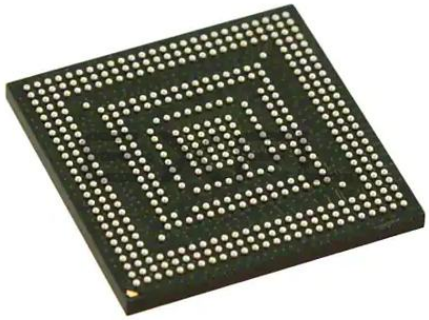

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31vkn5cr2

Table 16. DDR (Double Data Rate) I/O DC Electrical Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low-level output current	I_{OL}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 3.6 7.2 10.8 14.4	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	NVCC	NVCC+0.3	V
Low-Level DC input voltage	V_{IL}	—	–0.3	0	0.3*NVCC	V
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.2 AC Electrical Characteristics

Figure 5 depicts the load circuit for outputs. Figure 6 depicts the output transition time waveform. The range of operating conditions appears in Table 17 for slow general I/O, Table 18 for fast general I/O, and Table 19 for DDR I/O (unless otherwise noted).

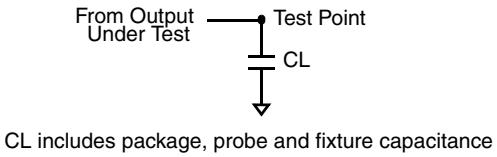

Figure 5. Load Circuit for Output

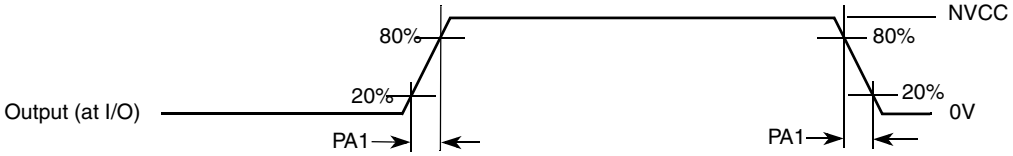

Figure 6. Output Transition Time Waveform

Table 17. AC Electrical Characteristics of Slow[1] General I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.92 1.5	1.95 2.98	3.17 4.75	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	1.52 2.75	—	4.81 8.42	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	2.79 5.39	—	8.56 16.43	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

Table 18. AC Electrical Characteristics of Fast[1] General I/O [2]

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.68 1.34	1.33 2.6	2.07 4.06	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.91 1.79	1.77 3.47	2.74 5.41	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.36 2.68	2.64 5.19	4.12 8.11	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

Table 19. AC Electrical Characteristics of DDR I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (DDR Drive)[1]	tpr	25 pF 50 pF	0.51 0.97	0.82 1.58	1.28 2.46	ns
	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.67 1.29	1.08 2.1	1.69 3.27	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.99 1.93	1.61 3.13	2.51 4.89	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.96 3.82	3.19 6.24	4.99 9.73	ns

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 20 shows clock amplifier electrical characteristics.

Table 20. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1]– 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

4.3.5.2 PIO Mode Timing

Figure 11 shows timing for PIO read, and Table 25 lists the timing parameters for PIO read.

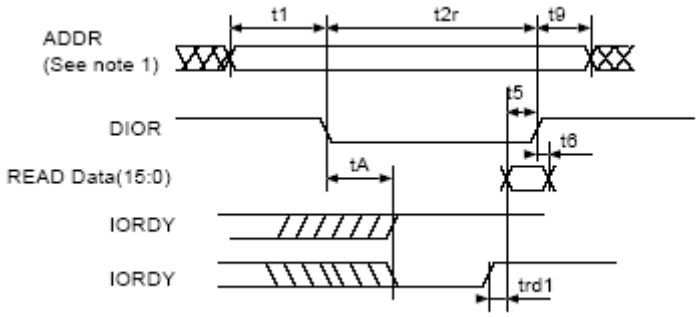

Figure 11. PIO Read Timing Diagram

Table 25. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 12 shows timing for PIO write, and Table 26 lists the timing parameters for PIO write.

Table 33. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 28, Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

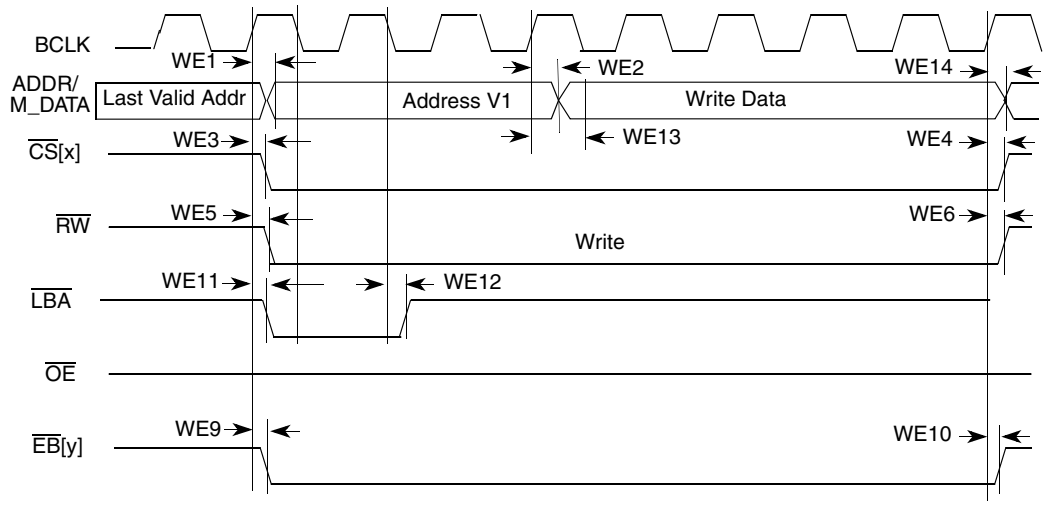

Figure 32. Muxed A/D Mode Timing Diagram for Asynchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

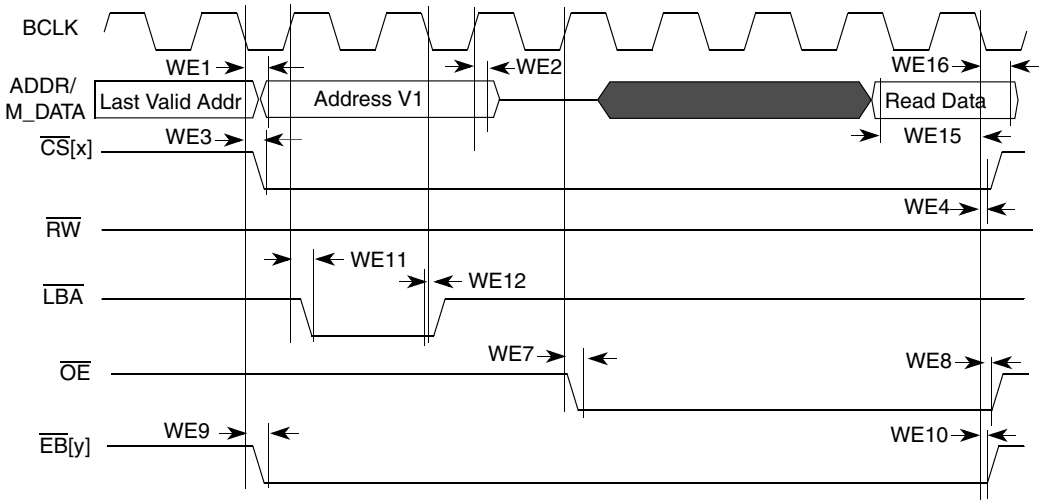

Figure 33. Muxed A/D Mode Timing Diagram for Asynchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

4.3.9.3 ESDCTL Electrical Specifications

Figure 34, Figure 35, Figure 36, Figure 37, Figure 38, and Figure 39 depict the timings pertaining to the ESDCTL module, which interfaces Mobile DDR or SDR SDRAM. Table 34, Table 35, Table 36, Table 37, Table 38, and Table 39 list the timing parameters.

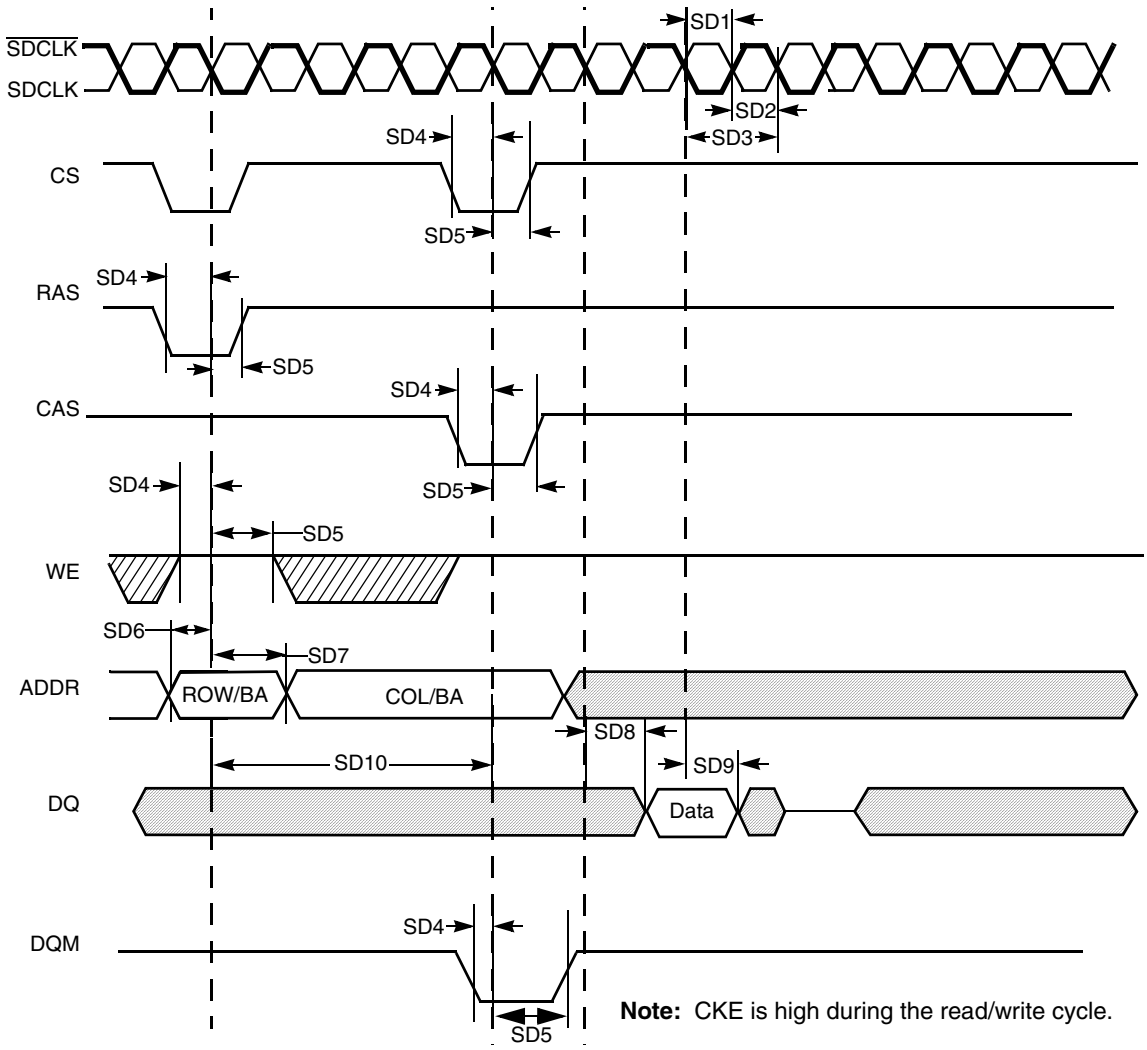

Figure 34. SDRAM Read Cycle Timing Diagram

Table 34. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

Table 46. Supported Display Components[1]

Type	Vendor	Model
TFT displays (memory-less)	Sharp (HR-TFT Super Mobile LCD family)	LQ035Q7 DB02, LM019LC1Sxx
	Samsung (QCIF and QVGA TFT modules for mobile phones)	LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2]
	Toshiba (LTM series)	LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2]
	NEC	NL6448BC20-08E, NL8060BC31-27
Display controllers	Epson	S1D15xxx series, S1D19xxx series, S1D13713, S1D13715
	Solomon Systech	SSD1301 (OLED), SSD1828 (LDCD)
	Hitachi	HD66766, HD66772
	ATI	W2300
Smart display modules	Epson	L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2]
	Hitachi	120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller
	Densitron Europe LTD	All displays with MPU 80/68K series interface and serial peripheral interface
	Sharp	LM019LC1Sxx
	Sony	ACX506AKM
Digital video encoders (for TV)	Analog Devices	ADV7174/7179
	Crystal (Cirrus Logic)	CS49xx series
	Focus	FS453/4

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

2 These display components not validated at time of publication.

4.3.15.2 Synchronous Interfaces

4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 46 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

Table 49. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) * Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY * Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY * Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY * Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY * Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY * Tdpcp	ns

4.3.15.4 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.3.15.2.2, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.3.15.4.1 Interface to a TV Encoder, Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 51 depicts the interface timing,

- The frequency of the clock DISPB_D3_CLK is 27 MHz (within 10%).
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

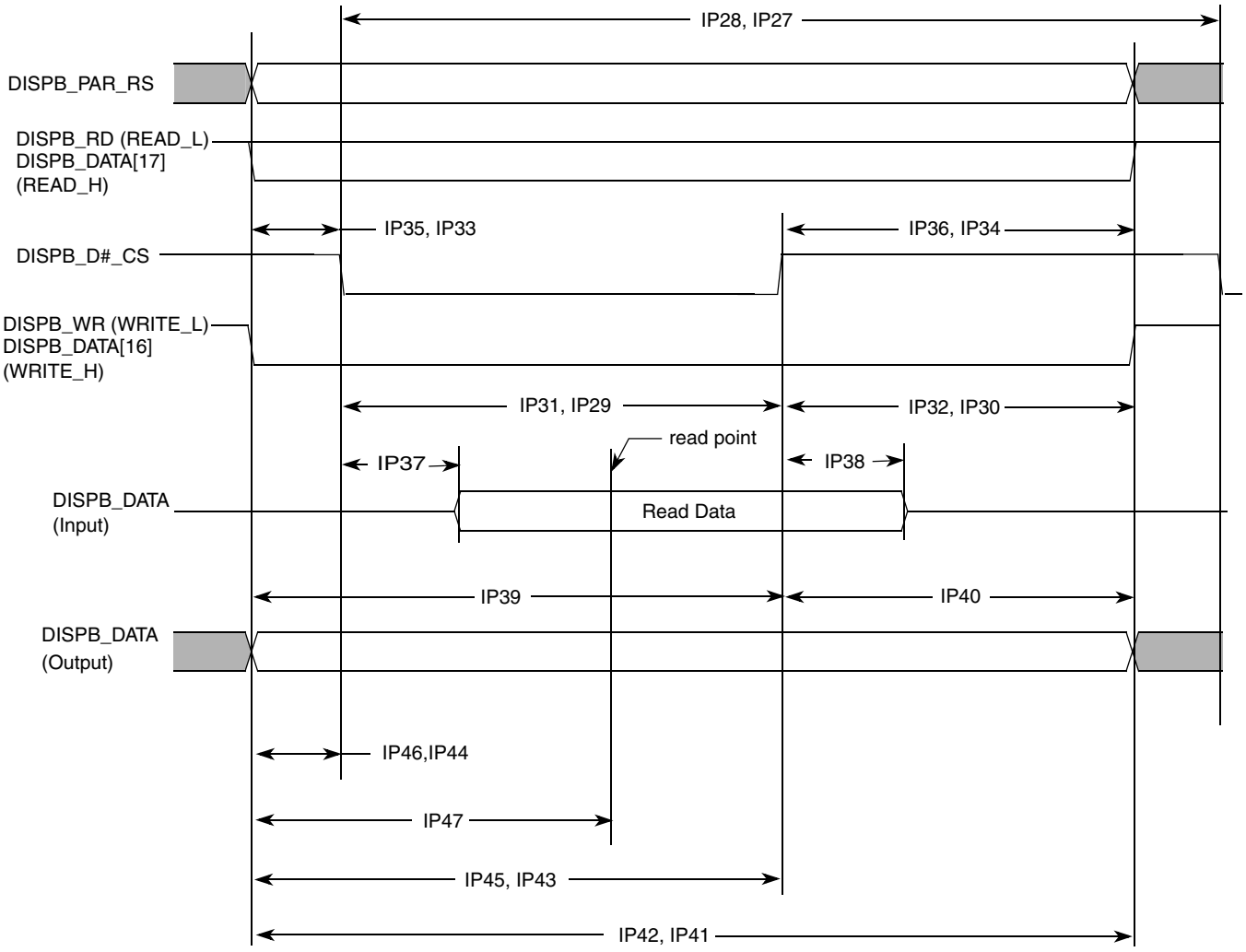

Figure 57. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

Table 50. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP36	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]–Tdicur–1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns
IP39	Write data setup time	Tds	Tdicdw–1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr–1.5	Tdicpr	Tdicpr+1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw–1.5	Tdicpw	Tdicpw+1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr–1.5	Tdicdr	Tdicdr+1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw–1.5	Tdicdw	Tdicdw+1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

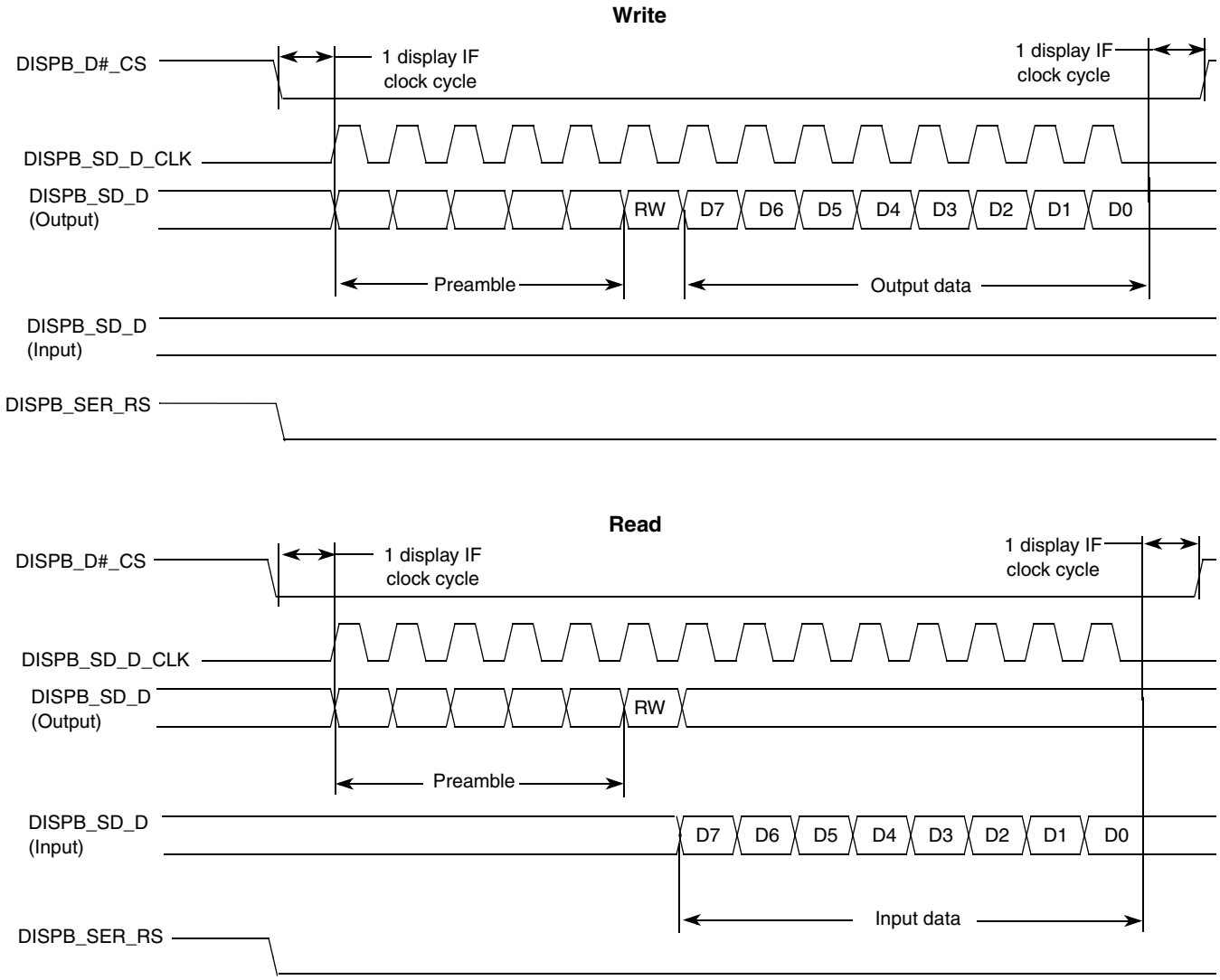

Figure 63. 5-Wire Serial Interface (Type 1) Timing Diagram

4.3.15.5.4 Serial Interfaces, Electrical Characteristics

Figure 65 depicts timing of the serial interface. Table 51 lists the timing parameters at display access level.

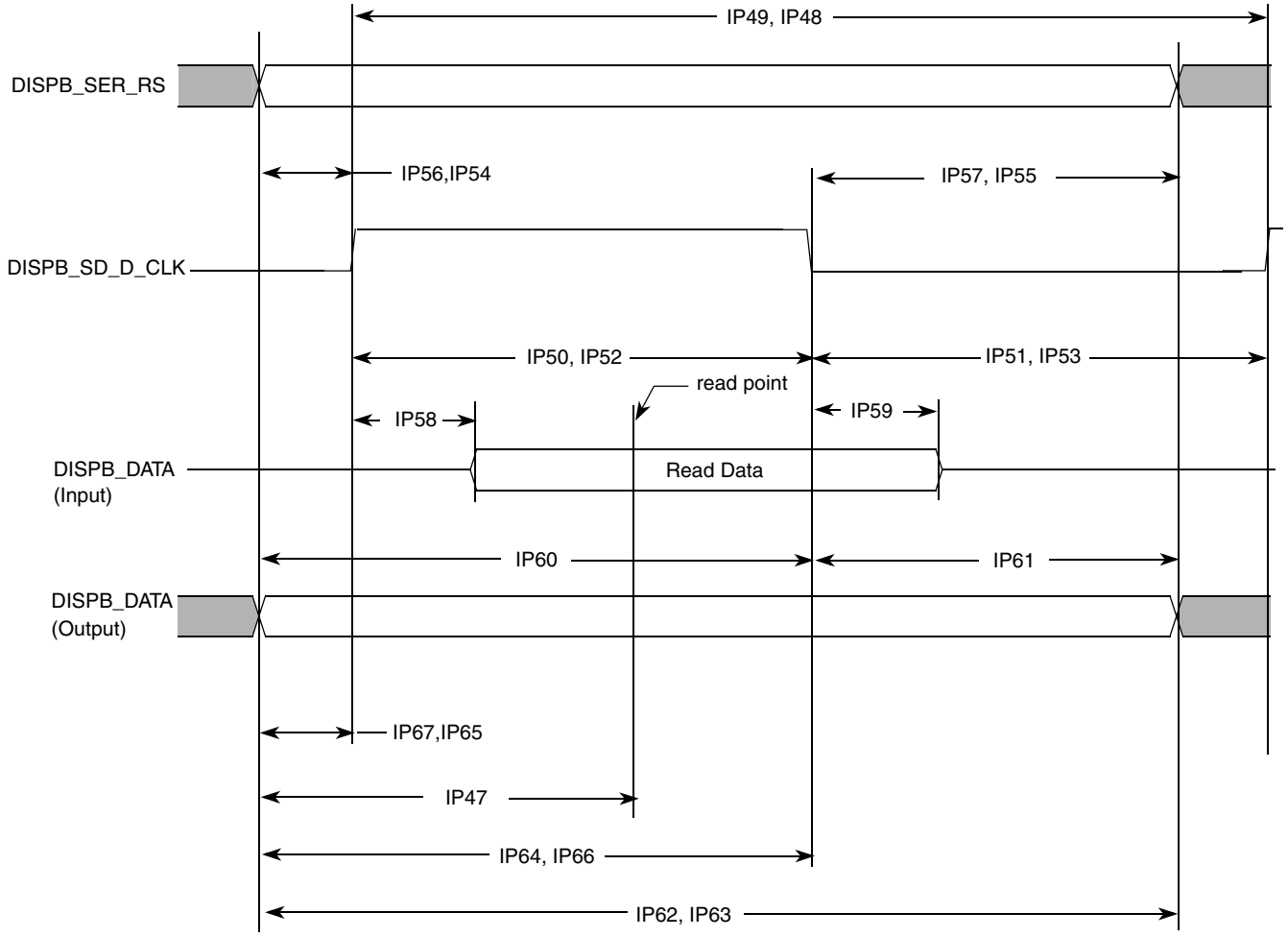

Figure 65. Asynchronous Serial Interface Timing Diagram

Table 51. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns

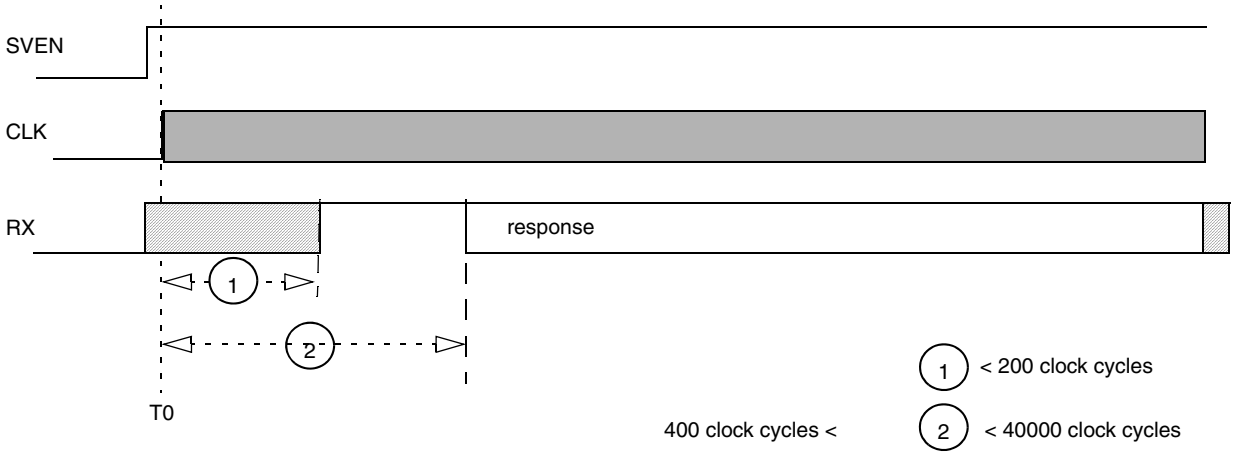

Figure 74. Internal-Reset Card Reset Sequence

4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 75):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

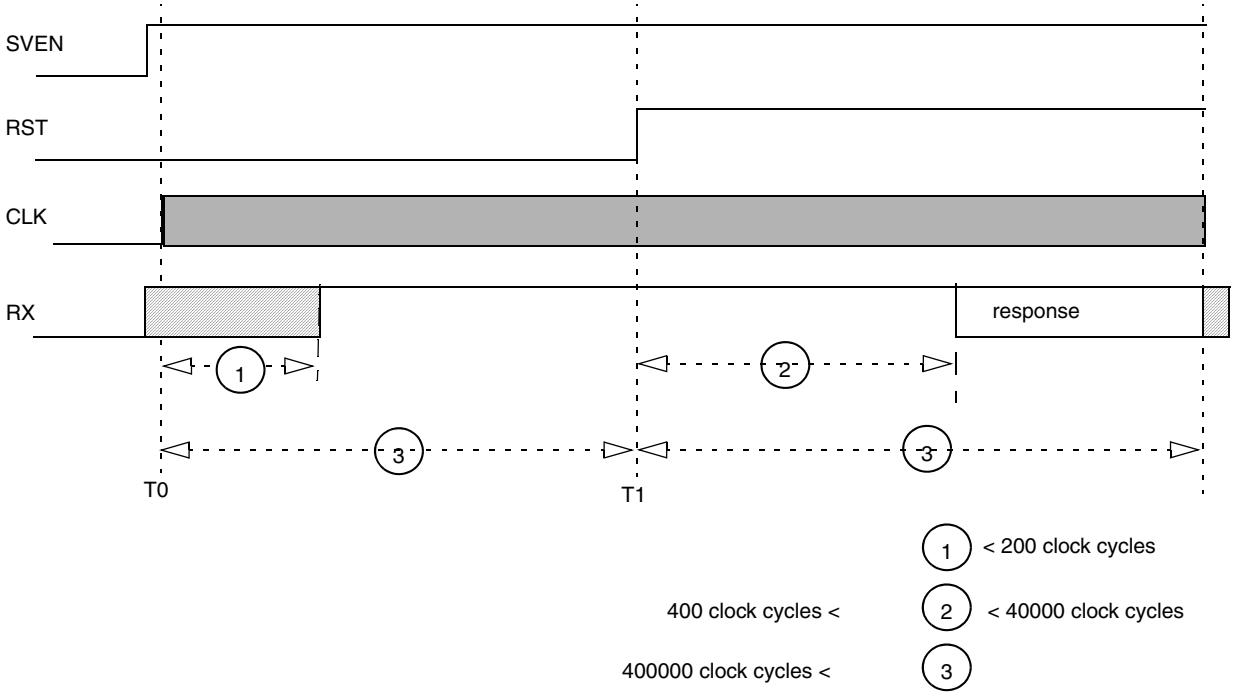

Figure 75. Active-Low-Reset Card Reset Sequence

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 77 depicts the SJC test clock input timing. Figure 78 depicts the SJC boundary scan timing, Figure 79 depicts the SJC test access port, Figure 80 depicts the SJC TRST timing, and Table 59 lists the SJC timing parameters.

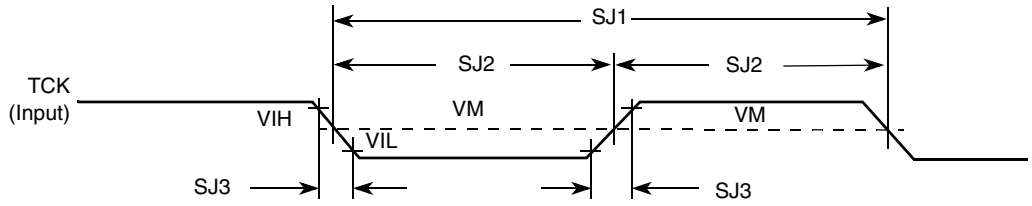

Figure 77. Test Clock Input Timing Diagram

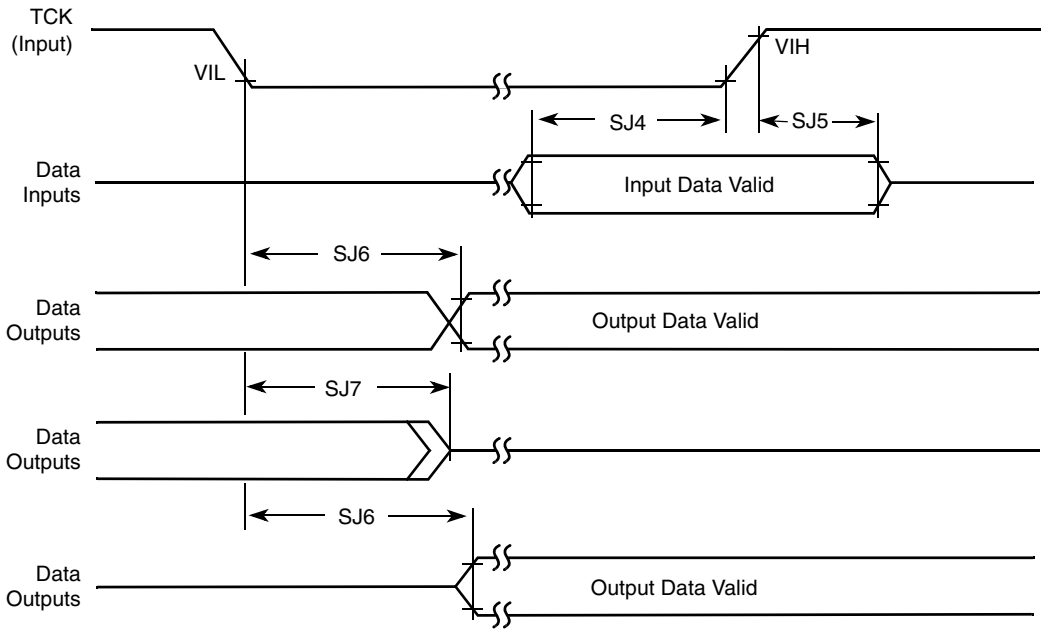

Figure 78. Boundary Scan (JTAG) Timing Diagram

Table 62. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 63. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 85 depicts the USB ULPI timing diagram, and Table 64 lists the timing parameters.

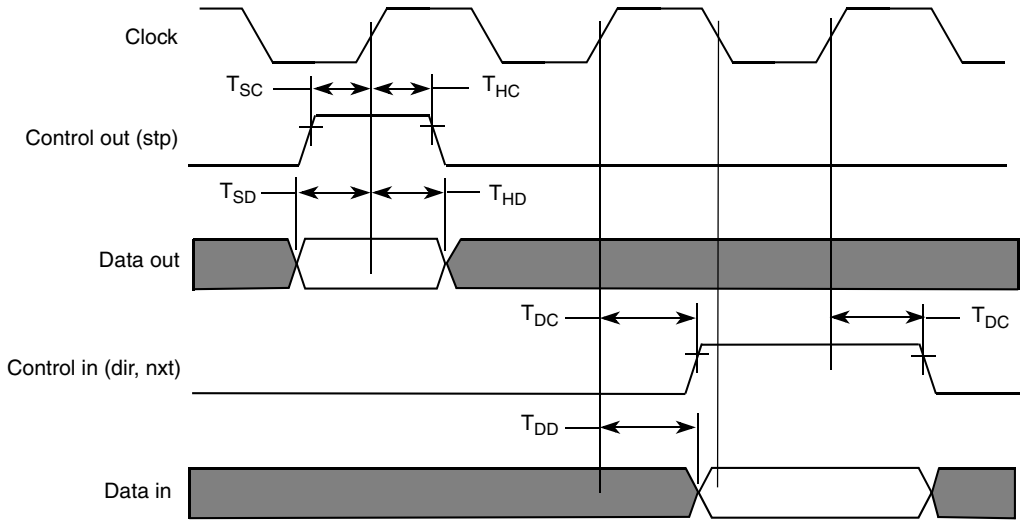

Figure 85. USB ULPI Interface Timing Diagram

Table 64. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 66 shows the device connection list for signals only, alpha-sorted by signal identification.

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	AD6
A1	AF5
A10	AF18
A11	AC3
A12	AD3
A13	AD4
A14	AF17
A15	AF16
A16	AF15
A17	AF14
A18	AF13
A19	AF12
A2	AB5
A20	AF11
A21	AF10
A22	AF9
A23	AF8
A24	AF7
A25	AF6
A3	AE4
A4	AA3
A5	AF4
A6	AB3
A7	AE3
A8	AD5
A9	AF3
ATA_CS0	J6
ATA_CS1	F2
ATA_DIOR	E2
ATA_DIOW	H6
ATA_DMACK	F1
$\overline{\text{ATA\_RESET}}$	H3
BATT_LINE	F7
BCLK	AB26
BOOT_MODE0	F20
BOOT_MODE1	C21
BOOT_MODE2	D24
BOOT_MODE3	C22
BOOT_MODE4	D26
CAPTURE	A22
CAS	AD20
CE_CONTROL	A14
CKIH	F24

Signal ID	Ball Location
CKIL	H21
CLKO	C23
CLKSS	G26
COMPARE	G18
CONTRAST	R24
CS0	AE23
CS1	AF23
CS2	AE21
CS3	AD22
CS4	AF24
CS5	AF22
CSI_D10	M24
CSI_D11	L26
CSI_D12	M21
CSI_D13	M25
CSI_D14	M20
CSI_D15	M26
CSI_D4	L21
CSI_D5	K25
CSI_D6	L24
CSI_D7	K26
CSI_D8	L20
CSI_D9	L25
CSI_HSYNC	K20
CSI_MCLK	K24
CSI_PIXCLK	J26
CSI_VSYNC	J25
CSPI1_MISO	P7
CSPI1_MOSI	P2
CSPI1_SCLK	N2
CSPI1_SPI_RDY	N3
CSPI1_SS0	P3
CSPI1_SS1	P1
CSPI1_SS2	P6
CSPI2_MISO	A4
CSPI2_MOSI	E3
CSPI2_SCLK	C7
CSPI2_SPI_RDY	B6
CSPI2_SS0	B5
CSPI2_SS1	C6
CSPI2_SS2	A5
CSPI3_MISO	G3
CSPI3_MOSI	D2

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
EB1	W21
ECB	Y21
FPSHIFT	M23
GPIO1_0	C19
GPIO1_1	G17
GPIO1_2	B20
LD7	T20
LD8	R17
LD9	U23
M_GRANT	U18
M_REQUEST	T17
MA10	Y2
MCUPG	See VPG0
NFALE	T2
$\overline{\text{NFCE}}$	R4
NFCLE	T1
NFRB	R3
$\overline{\text{NFRE}}$	T4
$\overline{\text{NFWE}}$	T3
$\overline{\text{NFWP}}$	P6
OE	T18
PAR_RS	P22
PC_BVD1	G2
PC_BVD2	H4
$\overline{\text{PC\_CD1}}$	J3
$\overline{\text{PC\_CD2}}$	H1
PC_POE	J6
PC_PWRON	K6
PC_READY	H2
PC_RST	F1
$\overline{\text{PC\_RW}}$	G3
PC_VS1	H3
PC_VS2	G1
$\overline{\text{PC\_WAIT}}$	J4
$\overline{\text{POR}}$	F21
POWER_FAIL	F20
PWMO	F2
RAS	AA19
READ	N18
$\overline{\text{RESET\_IN}}$	F22
RI_DCE1	D10
RI_DTE1	B11
RTCK	D15
RTS1	B9
RTS2	B12
RW	V18

Signal ID	Ball Location
LD17	W23
LD2	R21
LD3	R20
LD4	T23
LD5	T22
LD6	T21
SCK6	R2
SCLK0	B19
SD_D_CLK	M21
SD_D_I	M20
SD_D_IO	M18
SD0	AC18
SD1	AA17
SD1_CLK	K2
SD1_CMD	K3
SD1_DATA0	K4
SD1_DATA1	J1
SD1_DATA2	J2
SD1_DATA3	L6
SD10	AB14
SD11	AC14
SD12	AA13
SD13	AB13
SD14	AC13
SD15	AA12
SD16	AC12
SD17	AA11
SD18	AB11
SD19	AC11
SD2	AB17
SD20	AA10
SD21	AB10
SD22	AC10
SD23	AC9
SD24	AA9
SD25	AC8
SD26	AB8
SD27	AC7
SD28	AA8
SD29	AB7
SD3	AC17
SD30	AA7
SD31	AC6
SD4	AA16
SD5	AC16
SD6	AA15

Table 69. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
RXD1	C9
RXD2	A12
SCK3	P1
SCK4	G6
SCK5	D4
SDCKE0	Y17
SDCKE1	V16
SDCLK	AC20
$\overline{\text{SDCLK}}$	AC19
SDQS0	AB16
SDQS1	AB12
SDQS2	AB9
SDQS3	AB6
SDWE	AB20
SER_RS	P23
SFS3	P2
SFS4	D3
SFS5	G7
SFS6	P4
SIMPD0	B18
SJC_MOD	C17
SRST0	C18
SRX0	A19
SRXD3	N3
SRXD4	C3
SRXD5	C4
SRXD6	R1
STX0	F16
STXD3	N4
STXD4	B3
STXD5	D1
STXD6	P3
SVEN0	D17
TCK	F14
TDI	A18
TDO	B17
TMS	C16

Signal ID	Ball Location
SD7	AB15
SD8	AC15
SD9	AA14
SDBA0	AA6
SDBA1	Y7
TRSTB	F15
TXD1	D9
TXD2	F11
USB_BYP	C8
USB_OC	B8
USB_PWR	A8
USBH2_CLK	L1
USBH2_DATA0	M6
USBH2_DATA1	K1
USBH2_DIR	L2
USBH2_NXT	L4
USBH2_STP	L3
USBOTG_CLK	D8
USBOTG_DATA0	G8
USBOTG_DATA1	C7
USBOTG_DATA2	A6
USBOTG_DATA3	F8
USBOTG_DATA4	D7
USBOTG_DATA5	B6
USBOTG_DATA6	A5
USBOTG_DATA7	C6
USBOTG_DIR	A7
USBOTG_NXT	B7
USBOTG_STP	F9
VPG0	G21
VPG1	G22
VSTBY	H18
VSYNC0	L22
VSYNC3	N20
WATCHDOG_RST	B21
WRITE	N22

6 Product Differences

The locations that provide the differences between silicon Revision 2.0, 1.2, and previous versions are given in Table 72. The differences between the MCIMX31/MCIMX31L and the MCIMX31C/MCIMX31LC are outlined in Table 73.

Table 72. Silicon Differentiation by Location within the Data Sheet

Item	Location	Silicon 1.2 and Previous	Silicon 2.0
Ordering Information	Section 1.2, “Ordering Information	Table 1	Table 1
Feature Differences	Table 1.2.1, "Feature Differences Between Mask Sets," on page 3	N/A	Table 1.2.1
Operating Ranges	Table 4.1, "Chip-Level Conditions," on page 10	Table 8, "Operating Ranges," on page 13	Table 8, and Table 9, "Specific Operating Ranges for Silicon Revision 2.0," on page 14
Power-up Sequences	Section 4.2.1, “Powering Up	Figure 2, "Power-Up Sequence for Silicon Revisions 1.2 and Previous," on page 20	Figure 3, "Option 1 Power-Up Sequence (Silicon Revision 2.0)," on page 21
Power-down Sequences	Section 4.2.2, “Powering Down	—	—

Table 73. Product Differentiation

Item	Location	MCIMX31/MCIMX31L	MCIMX31C/MCIMX31LC
Device ordering information	Table 1, "Ordering Information," on page 3	See Table 1.	See Table 1.
Thermal simulation values	Table 6, "Thermal Resistance Data—14 × 14 mm Package," on page 11 and Table 7, "Thermal Resistance Data—19 × 19 mm Package," on page 11	See Table 6 and Table 7.	See Table 7.
Core overdrive operating voltages	Table 8, "Operating Ranges," on page 13	Capability to operate in overdrive voltages.	Not capable of overdrive operating voltages.
Fuse_VDD	Table 8, "Operating Ranges," on page 13 and Table 9, "Specific Operating Ranges for Silicon Revision 2.0," on page 14	Fusebox read Supply Voltage 1.65 min, 1.95 max.	In read mode, FUSE_VDD should be floated.
Ambient operating temperature range	Table 13, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0," on page 17, and Table 14, "Current Consumption for 0×C to 70×C, for Silicon Revision 2.0," on page 18	0°C min, 70°C max –40°C min, 85°C max	–40°C min, 85°C max
Current consumption values	Table 13, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0," on page 17	Typical value changes for State Retention, Doze, and Wait. See Table.	Typical value changes for State Retention, Doze, and Wait. See Table.
DPLL maximum output freq range	Table 31, "DPLL Specifications," on page 37	MPLL and SPLL = 532 MHz	MPLL and SPLL = 400 MHz