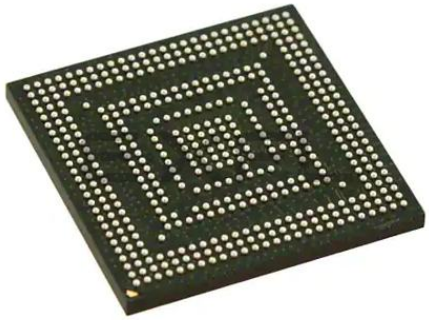

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31vkn5r2

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
Fusebox	Fusebox	ROM	The Fusebox is a ROM that is factory configured by Freescale.	4.3.12/55 See also Table 11
GPIO	General Purpose I/O Module	Pins	The GPIO provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose signals that can be configured as either inputs or outputs.	—
GPT	General Purpose Timer	Timer Peripheral	The GPT is a multipurpose module used to measure intervals or generate periodic output.	—
GPU	Graphics Processing Unit	Multimedia Peripheral	The GPU provides hardware acceleration for 2D and 3D graphics algorithms.	—
I^2C	Inter IC Communication	Connectivity Peripheral	The I^2C provides serial interface for controlling the Sensor Interface and other external devices. Data rates of up to 100 Kbits/s are supported.	4.3.13/56
IIM	IC Identification Module	ID	The IIM provides an interface for reading device identification.	—
IPU	Image Processing Unit	Multimedia Peripheral	The IPU processes video and graphics functions in the MCIMX31 and interfaces to video, still image sensors, and displays.	4.3.14/57, 4.3.15/59
KPP	Keypad Port	Connectivity Peripheral	The KPP is used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix.	—
MPEG-4	MPEG-4 Video Encoder	Multimedia Peripherals	The MPEG-4 encoder accelerates video compression, following the MPEG-4 standard	—
MSHC	Memory Stick Host Controller	Connectivity Peripheral	The MSHC is placed in between the AIPS and the customer memory stick to support data transfer from the MCIMX31 to the customer memory stick.	4.3.16/84
PADIO	Pads I/O	Buffers and Drivers	The PADIO serves as the interface between the internal modules and the device's external connections.	4.3.1/22
PCMCIA	PCM	Connectivity Peripheral	The PCMCIA Host Adapter provides the control logic for PCMCIA socket interfaces.	4.3.17/86
PWM	Pulse-Width Modulator	Timer Peripheral	The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones.	4.3.18/88
RNGA	Random Number Generator Accelerator	Security	The RNGA module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism.	—
RTC	Real Time Clock	Timer Peripheral	The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050.	—
RTIC	Run-Time Integrity Checkers	Security	The RTIC ensures the integrity of the peripheral memory contents and assists with boot authentication.	—

4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. MCIMX31 Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, “Absolute Maximum Ratings”	on page 10
Table 7, “Thermal Resistance Data—19 × 19 mm Package”	on page 11
Table 8, “Operating Ranges”	on page 13
Table 9, “Specific Operating Ranges for Silicon Revision 2.0”	on page 14
Table 10, “Interface Frequency”	on page 14
Section 4.1.1, “Supply Current Specifications”	on page 16
Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions”	on page 19

CAUTION

Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 8, "Operating Ranges," on page 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.65	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.3	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	°C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	1500	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	500	
Offset voltage allowed in run mode between core supplies.	V_{core_offset} [1]	—	15	mV

[1] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 6 provides the thermal resistance data for the 14 × 14 mm, 0.5 mm pitch package.

Table 6. Thermal Resistance Data—14 × 14 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	56	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	30	°C/W	1, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	26	°C/W	1, 3
Junction to Board	—	$R_{\theta JB}$	17	°C/W	1, 4
Junction to Case	—	$R_{\theta JC}$	10	°C/W	1, 5
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 6

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 7 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

Table 7. Thermal Resistance Data—19 × 19 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	29	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	25	°C/W	1, 2, 3
Junction to Board	—	$R_{\theta JB}$	19	°C/W	1, 3
Junction to Case (Top)	—	$R_{\theta JCtop}$	10	°C/W	1, 4
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 5

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31 (worst-case scenario)

4.2.1 Powering Up

The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power up sequence. Power up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 shows the power-up sequence for silicon Revisions 1.2 and previous. Figure 3 and Figure 4 show the power-up sequence for silicon Revision 2.0.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

4.3.5.2 PIO Mode Timing

Figure 11 shows timing for PIO read, and Table 25 lists the timing parameters for PIO read.

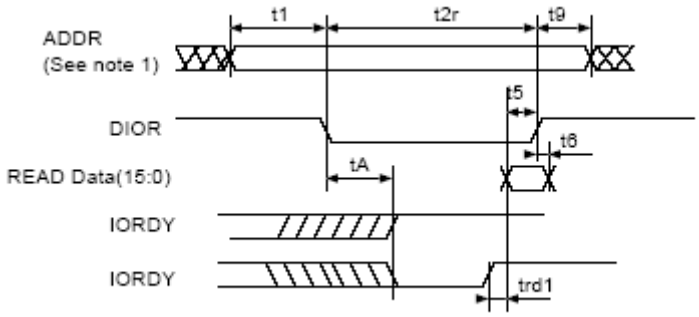


Figure 11. PIO Read Timing Diagram

Table 25. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 12 shows timing for PIO write, and Table 26 lists the timing parameters for PIO write.

Table 31. DPLL Specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Phase lock time	—	—	100	µs	In addition to the frequency
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ < 50 kHz
Maximum allowed PLL supply voltage ripple	—	—	20	mV	50 kHz < $F_{modulation}$ < 300 kHz
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ > 300 kHz
PLL output clock phase jitter	—	—	5.2	ns	Measured on CLKO pin
PLL output clock period jitter	—	—	420	ps	Measured on CLKO pin

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 23, Figure 24, Figure 25, and Figure 26 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 32 lists the timing parameters.

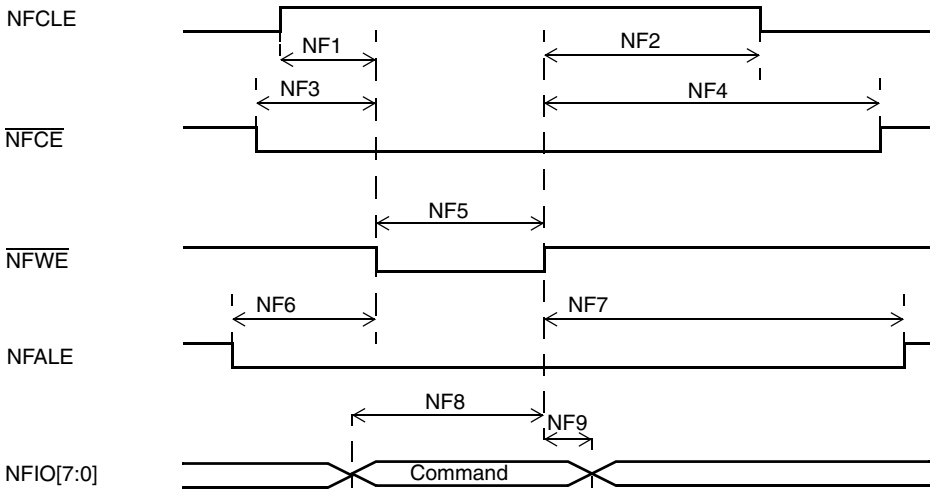


Figure 23. Command Latch Cycle Timing Diagram

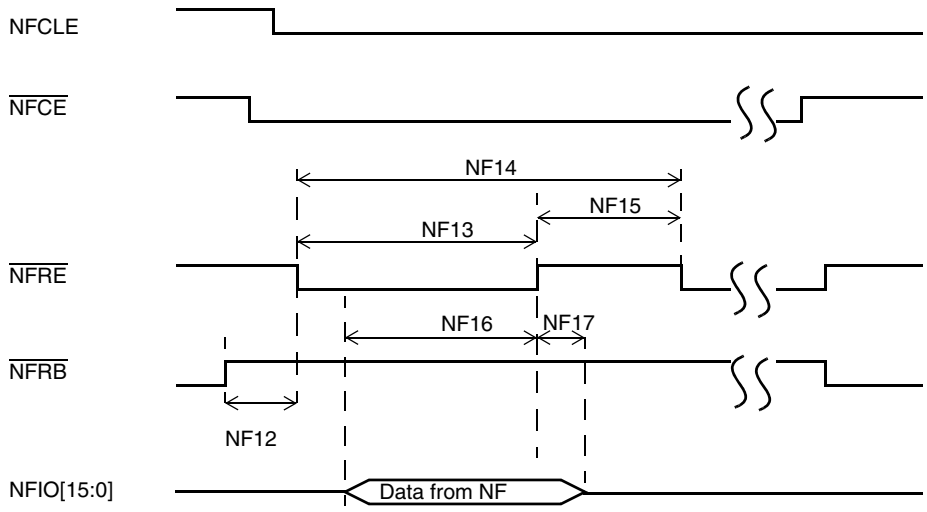


Figure 26. Read Data Latch Cycle Timing Diagram

Table 32. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min	Max	Min	Max	
NF1	NFCLE Setup Time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE Hold Time	tCLH	T–2.0 ns	—	28	—	ns
NF3	$\overline{\text{NFCE}}$ Setup Time	tCS	T–1.0 ns	—	29	—	ns
NF4	$\overline{\text{NFCE}}$ Hold Time	tCH	T–2.0 ns	—	28	—	ns
NF5	$\overline{\text{NF\_WP}}$ Pulse Width	tWP	T–1.5 ns		28.5		ns
NF6	NFALE Setup Time	tALS	T	—	30	—	ns
NF7	NFALE Hold Time	tALH	T–3.0 ns	—	27	—	ns
NF8	Data Setup Time	tDS	T	—	30	—	ns
NF9	Data Hold Time	tDH	T–5.0 ns	—	25	—	ns
NF10	Write Cycle Time	tWC	2T		60		ns
NF11	$\overline{\text{NFWE}}$ Hold Time	tWH	T–2.5 ns		27.5		ns
NF12	Ready to $\overline{\text{NFRE}}$ Low	tRR	6T	—	180	—	ns
NF13	$\overline{\text{NFRE}}$ Pulse Width	tRP	1.5T	—	45	—	ns
NF14	READ Cycle Time	tRC	2T	—	60	—	ns
NF15	$\overline{\text{NFRE}}$ High Hold Time	tREH	0.5T–2.5 ns		12.5	—	ns
NF16	Data Setup on READ	tDSR	N/A		10	—	ns
NF17	Data Hold on READ	tDHR	N/A		0	—	ns

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification on Table 31, "DPLL Specifications," on page 37.

Table 34. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD9	Data out hold time[1]	tOH	1.8	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 38 and Table 39.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 34 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.14.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 43.

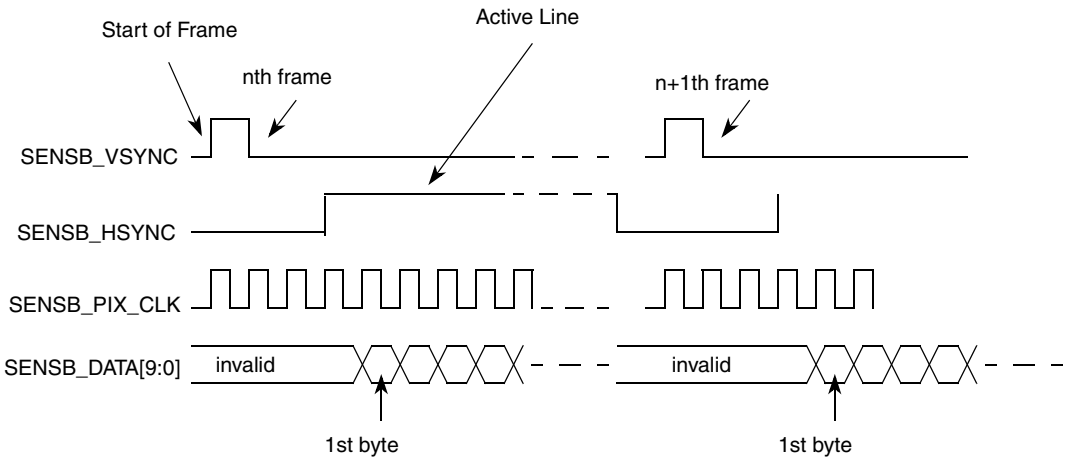


Figure 43. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.3.14.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.3.14.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 44. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

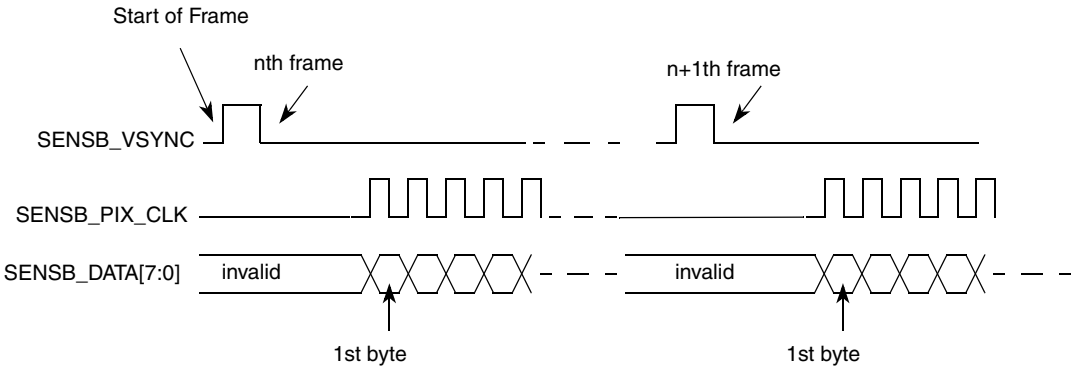


Figure 44. Non-Gated Clock Mode Timing Diagram

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

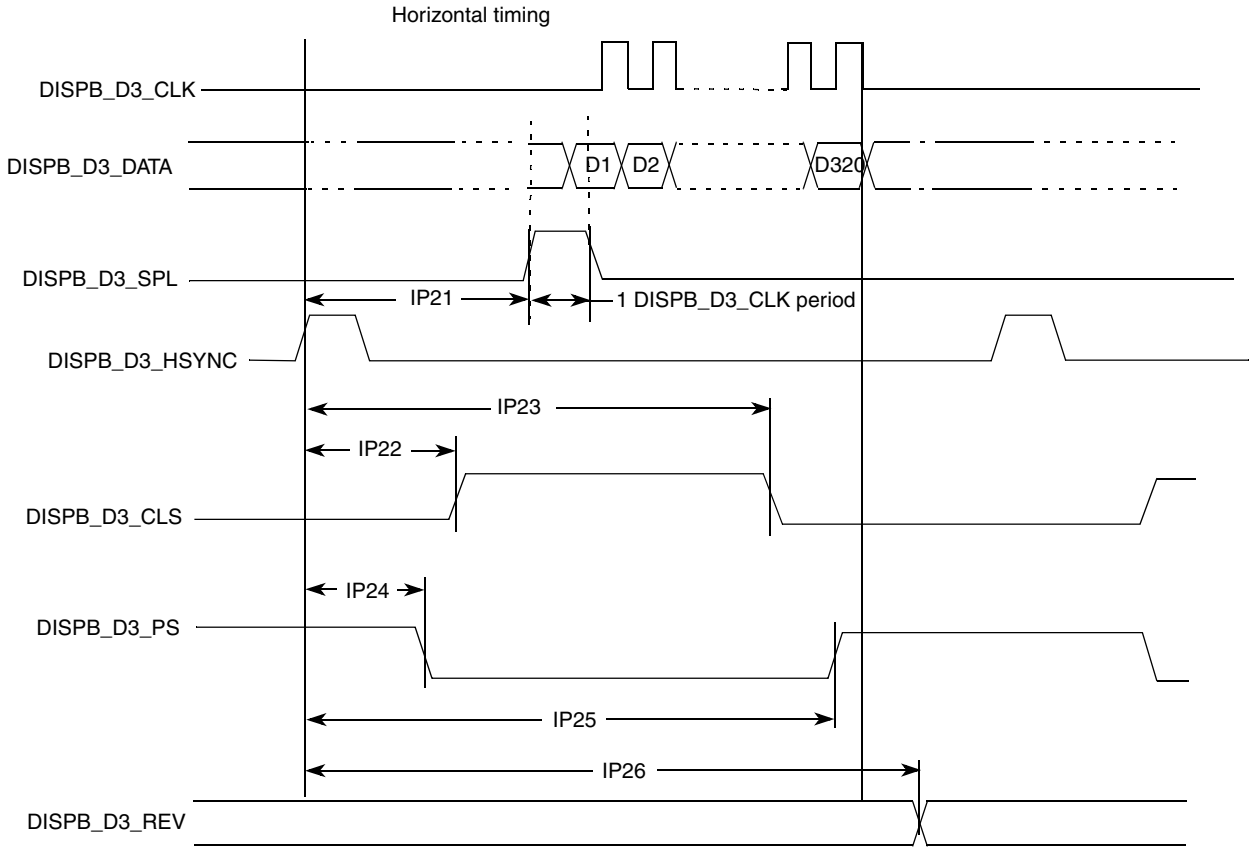
3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.3.15.3 Interface to Sharp HR-TFT Panels

Figure 50 depicts the Sharp HR-TFT panel interface timing, and Table 49 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics." The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW+1=320 pixel/line, FH+1=240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 50. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

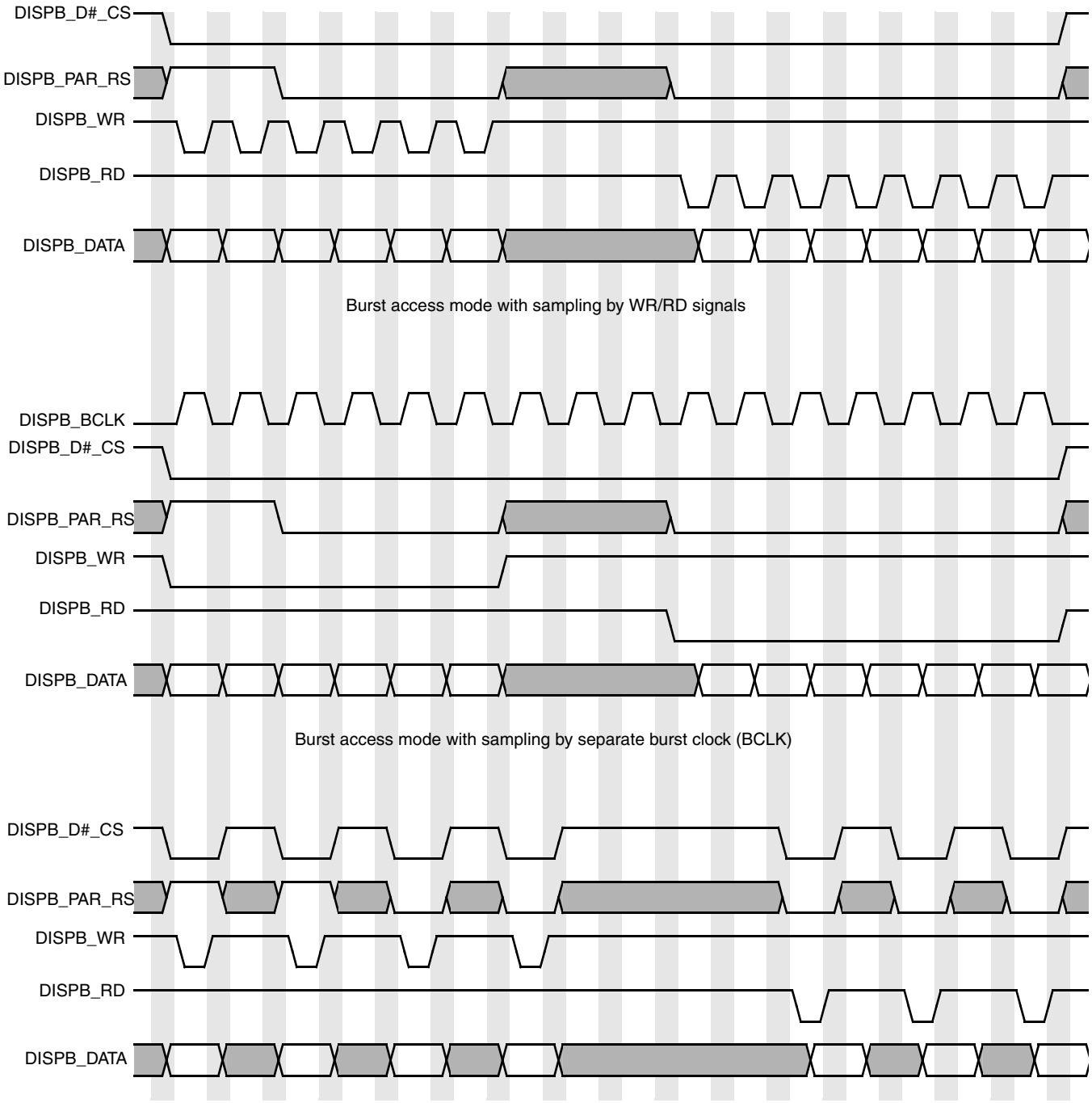


Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

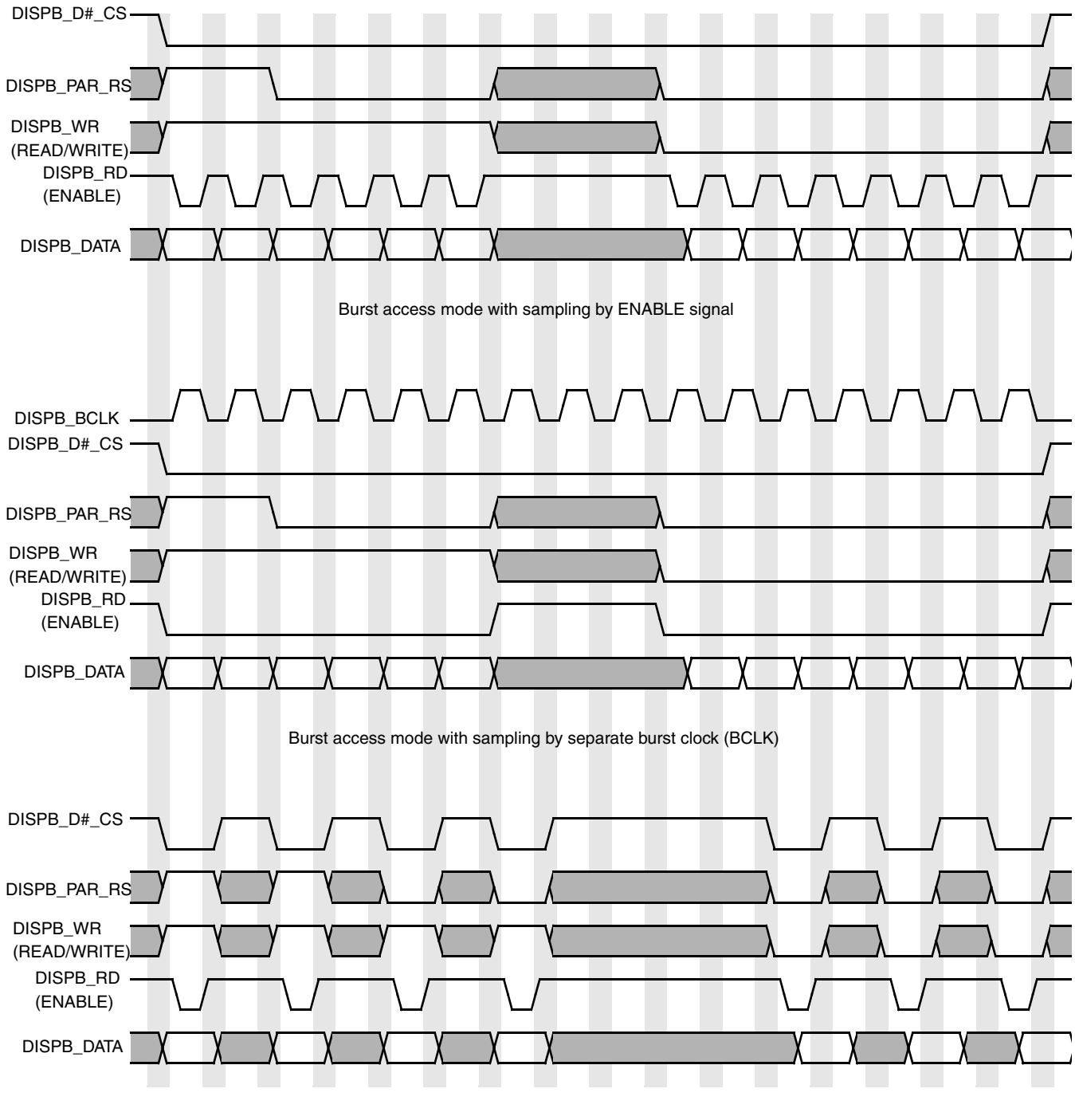


Figure 55. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to four display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the DI_DISP0_TIME_CONF_3, DI_DISP1_TIME_CONF_3, DI_DISP2_TIME_CONF_3 Registers. Figure 56 shows timing of the parallel interface with read wait states.

Figure 64 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

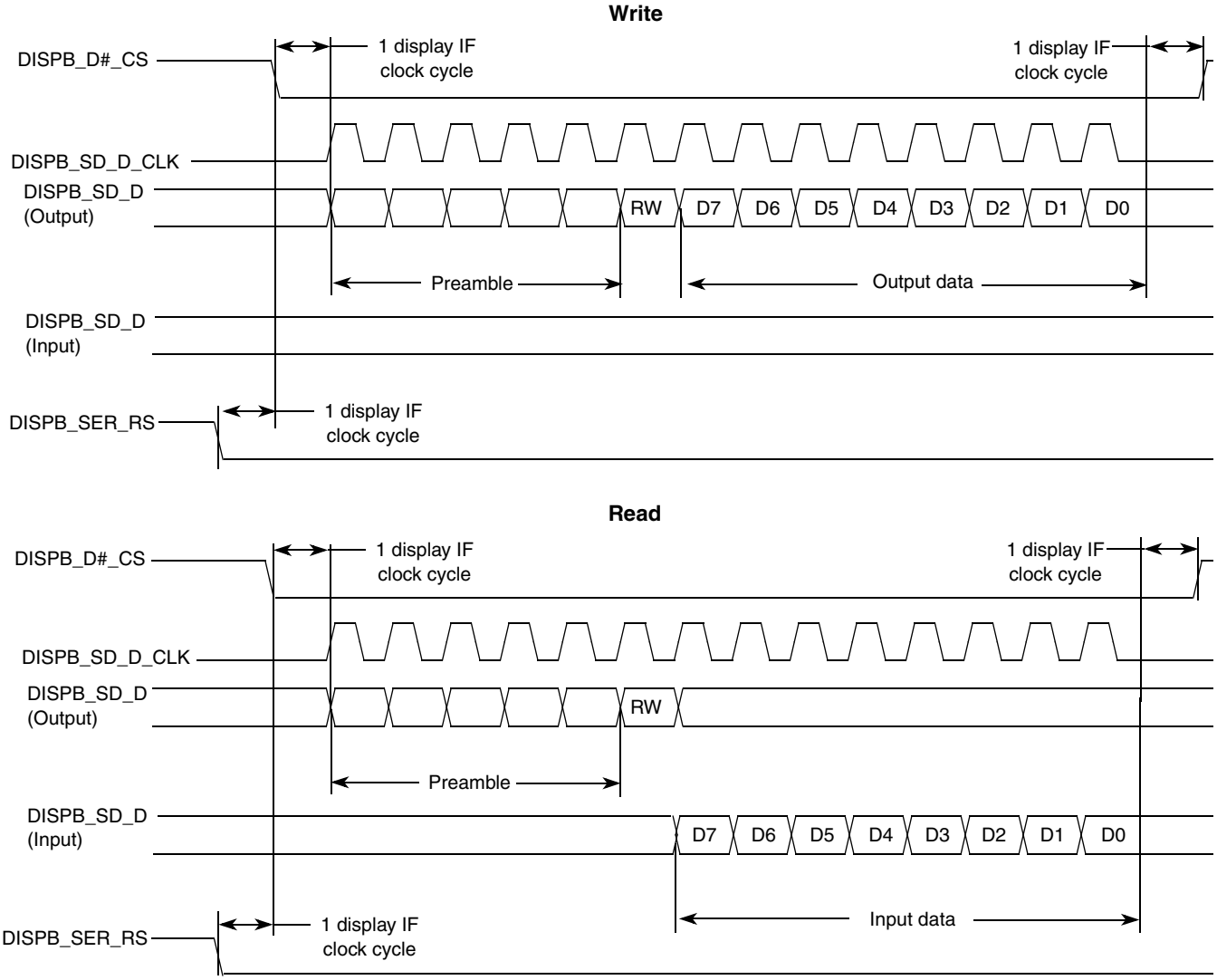


Figure 64. 5-Wire Serial Interface (Type 2) Timing Diagram

Table 51. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]–Tdicur–1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns
IP60	Write data setup time	Tds	Tdicdw–1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr–1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw–1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr–1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw–1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point:

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

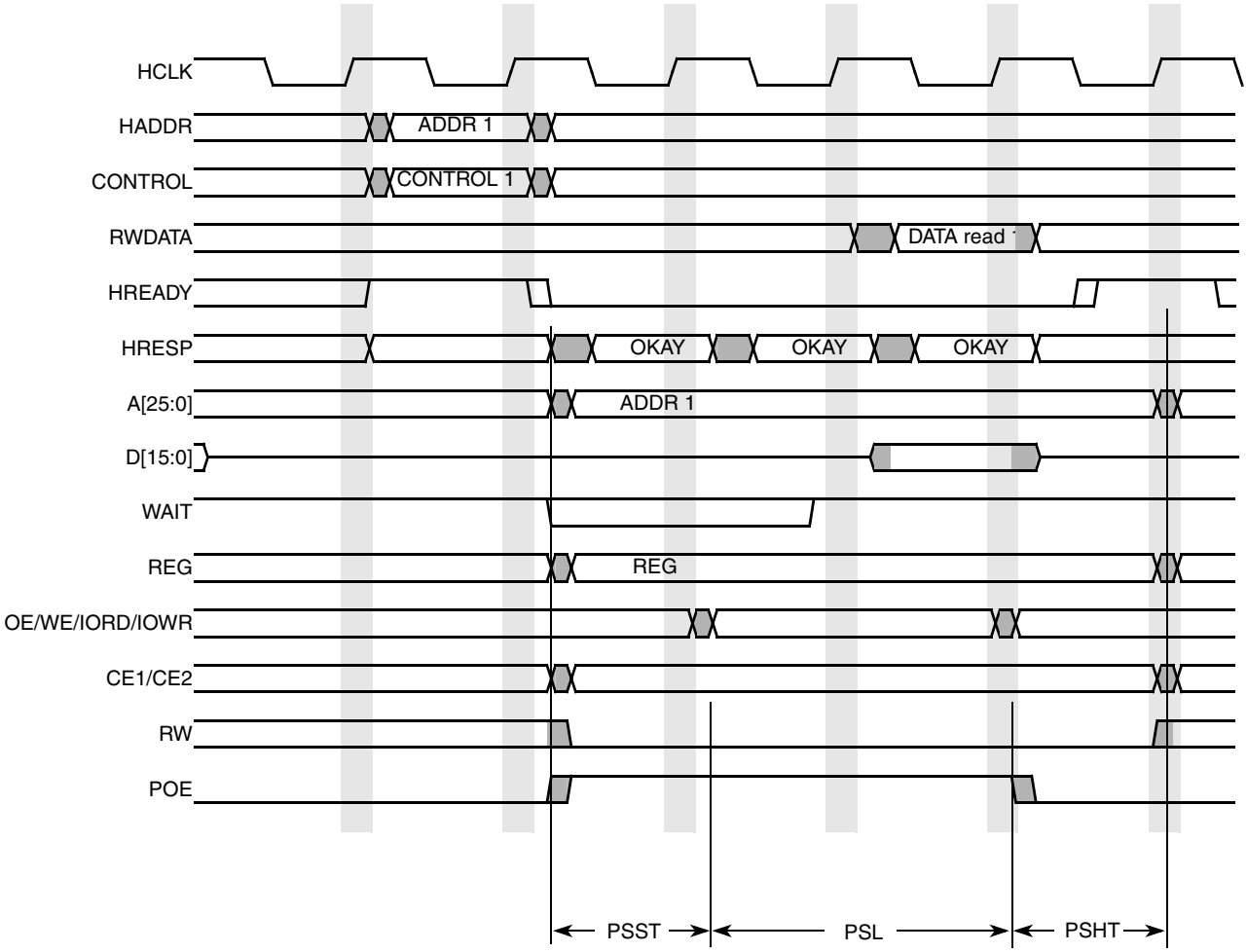


Figure 70. Read Accesses Timing Diagram—PSHT=1, PSST=1

Table 54. PCMCIA Write and Read Timing Parameters

Symbol	Parameter	Min	Max	Unit
PSHT	PCMCIA strobe hold time	0	63	clock
PSST	PCMCIA strobe set up time	1	63	clock
PSL	PCMCIA strobe length	1	128	clock

4.3.18 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Table 62. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 63. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 85 depicts the USB ULPI timing diagram, and Table 64 lists the timing parameters.

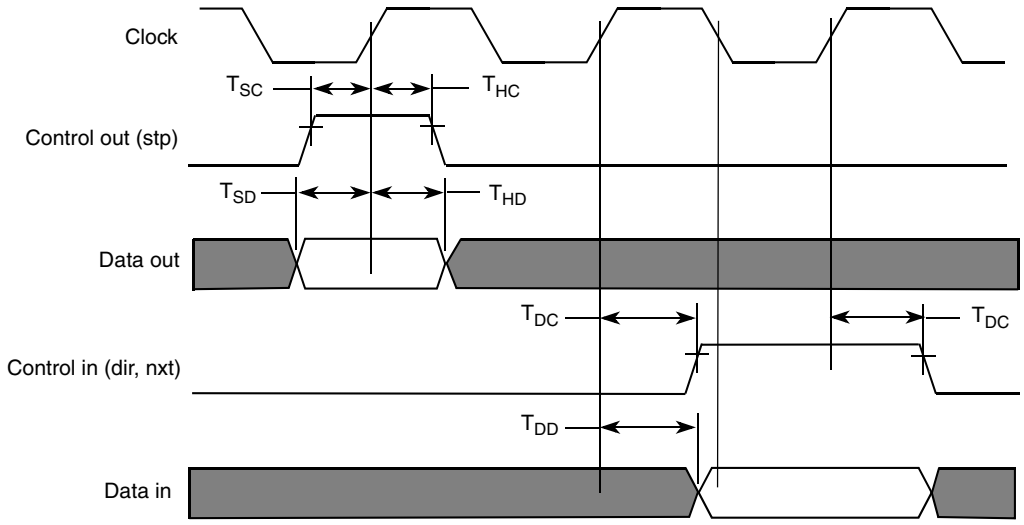


Figure 85. USB ULPI Interface Timing Diagram

Table 64. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 66 shows the device connection list for signals only, alpha-sorted by signal identification.

Table 66. 14 x 14 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	AD6
A1	AF5
A10	AF18
A11	AC3
A12	AD3
A13	AD4
A14	AF17
A15	AF16
A16	AF15
A17	AF14
A18	AF13
A19	AF12
A2	AB5
A20	AF11
A21	AF10
A22	AF9
A23	AF8
A24	AF7
A25	AF6
A3	AE4
A4	AA3
A5	AF4
A6	AB3
A7	AE3
A8	AD5
A9	AF3
ATA_CS0	J6
ATA_CS1	F2
ATA_DIOR	E2
ATA_DIOW	H6
ATA_DMACK	F1
$\overline{\text{ATA\_RESET}}$	H3
BATT_LINE	F7
BCLK	AB26
BOOT_MODE0	F20
BOOT_MODE1	C21
BOOT_MODE2	D24
BOOT_MODE3	C22
BOOT_MODE4	D26
CAPTURE	A22
CAS	AD20
CE_CONTROL	A14
CKIH	F24

Signal ID	Ball Location
CKIL	H21
CLKO	C23
CLKSS	G26
COMPARE	G18
CONTRAST	R24
CS0	AE23
CS1	AF23
CS2	AE21
CS3	AD22
CS4	AF24
CS5	AF22
CSI_D10	M24
CSI_D11	L26
CSI_D12	M21
CSI_D13	M25
CSI_D14	M20
CSI_D15	M26
CSI_D4	L21
CSI_D5	K25
CSI_D6	L24
CSI_D7	K26
CSI_D8	L20
CSI_D9	L25
CSI_HSYNC	K20
CSI_MCLK	K24
CSI_PIXCLK	J26
CSI_VSYNC	J25
CSPI1_MISO	P7
CSPI1_MOSI	P2
CSPI1_SCLK	N2
CSPI1_SPI_RDY	N3
CSPI1_SS0	P3
CSPI1_SS1	P1
CSPI1_SS2	P6
CSPI2_MISO	A4
CSPI2_MOSI	E3
CSPI2_SCLK	C7
CSPI2_SPI_RDY	B6
CSPI2_SS0	B5
CSPI2_SS1	C6
CSPI2_SS2	A5
CSPI3_MISO	G3
CSPI3_MOSI	D2

Table 71. Ball Map—19 x 19 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	GND	CSPI2_SS1	USBOTG_DATA6	USBOTG_DATA2	USBOTG_DIR	USB_PWR	CTS1	DTR_DTE1	DSR_DTE1	RXD2	KEY_ROW0	KEY_ROW3	KEY_COL0	KEY_COL5	KEY_COL7	TDI	SRX0	COMPARE	GND	GND	GND	A
B	GND	GND	STXD4	CSPI2_MISO	CSPI2_SCLK	USBOTG_DATA5	USBOTG_NXT	USB_OC	RTS1	DSR_DCE1	RI_DTE1	RTS2	KEY_ROW1	KEY_ROW6	KEY_COL1	KEY_COL6	TDO	SIMPD0	SCLK0	GPIO1_2	WATCHDOG_RST	GND	GND	B
C	GND	GND	SRXD4	SRXD5	CSPI2_SS0	USBOTG_DATA7	USBOTG_DATA1	USB_BYP	RXD1	DCD_DCE1	DTR_DCE2	CTS2	KEY_ROW2	KEY_ROW7	KEY_COL3	TMS	SJC_MOD	SRST0	GPIO1_0	CLKO	BOOT_MODE1	GND	GND	C
D	STXD5	CSPI3_MISO	SFS4	SCK5	CSPI2_MOSI	CSPI2_SPI_RDY	USBOTG_DATA4	USBOTG_CLK	TXD1	RI_DCE1	DCD_DTE1	CE_CONTROL	KEY_ROW5	KEY_COL2	RTCK	$\overline{DE}$	SVEN0	CAPTURE	GPIO1_5	BOOT_MODE2	GPIO1_4	GND	GND	D
E	ATA_CS0	ATA_DMACK	ATA_DIOR	CSPI3_MOSI																BOOT_MODE4	CKIL	DVFS0	DVFS1	E
F	PC_RST	PWMO	$\overline{ATA\_RESET}$	CSPI3_SPI_RDY		BATT_LINE	CSPI2_SS2	USBOTG_DATA3	USBOTG_STP	DTR_DCE1	TXD2	KEY_ROW4	KEY_COL4	TCK	TRSTB	STX0	BOOT_MODE0	BOOT_MODE3		POWER_FAIL	$\overline{POR}$	$\overline{RESET\_IN}$	CKIH	F
G	PC_VS2	PC_BVD1	$\overline{PC\_RW}$	ATA_CS1		SCK4	SFS5	USBOTG_DATA0	NVCC5	NVCC5	NVCC6	NVCC6	NVCC6	NVCC9	NVCC1	NVCC1	GPIO1_1	GPIO1_6		GPIO1_3	VPG0	VPG1	GPIO3_0	G
H	$\overline{PC\_CD2}$	PC_READY	PC_VS1	PC_BVD2		ATA_DIOW	CSPI3_SCLK	NVCC5	NVCC5	NVCC8	NVCC8	NVCC6	QVCC	NVCC4	NVCC7	NVCC1	CLKSS	VSTBY		CSI_MCLK	CSI_VSYNC	CSI_HSYNC	CSI_PIXCLK	H
J	SD1_DATA1	SD1_DATA2	$\overline{PC\_CD1}$	$\overline{PC\_WAIT}$		PC_POE	IOIS16	QVCC1	QVCC1	QVCC1	NVCC8	GND	GND	QVCC	NVCC4	NVCC7	NVCC1	I2C_CLK		CSI_D4	CSI_D5	CSI_D7	CSI_D8	J
K	USBH2_DATA1	SD1_CLK	SD1_CMD	SD1_DATA0		PC_PWRON	NVCC3	NVCC3	QVCC1	GND	GND	GND	GND	GND	NVCC4	NVCC7	GPIO3_1	I2C_DAT		CSI_D9	CSI_D10	CSI_D11	CSI_D12	K
L	USBH2_CLK	USBH2_DIR	USBH2_STP	USBH2_NXT		SD1_DATA3	NVCC3	NVCC3	QVCC4	GND	GND	GND	GND	GND	QVCC	NVCC7	CSI_D6	CSI_D14		CSI_D13	CSI_D15	VSYNC0	HSYNC	L
M	CSPI1_SPI_RDY	CSPI1_SS0	CSPI1_SS2	CSPI1_SCLK		USBH2_DATA0	QVCC4	QVCC4	GND	GND	GND	GND	GND	GND	QVCC	NVCC7	DRDY0	SD_D_IO		SD_D_I	SD_D_CLK	LCS0	FPSHIFT	M
N	CSPI1_MOSI	CSPI1_MISO	SRXD3	STXD3		CSPI1_SS1	NC[1]	QVCC4	QVCC	GND	GND	GND	GND	GND	QVCC	NVCC2	D3_SPL	READ		VSYNC3	CONTRAST	WRITE	LCS1	N
P	SCK3	SFS3	STXD6	SFS6		$\overline{NFWP}$	NC[1]	NVCC10	QVCC	GND	GND	GND	GND	GND	QVCC	NVCC2	UGND	UVCC		D3_CLS	D3_REV	PAR_RS	SER_RS	P
R	SRXD6	SCK6	NFRB	$\overline{NFCE}$		D13	NVCC10	NVCC10	NVCC10	QVCC	QVCC	GND	QVCC	QVCC	NVCC2	NVCC2	LD8	LD11		LD3	LD2	LD1	LD0	R
T	NFCLE	NFALE	$\overline{NFWE}$	$\overline{NFRE}$		D8	D4	IOQVDD	NVCC10	NVCC22	NVCC21	NVCC21	NVCC21	NVCC2	FUSE_VDD	FVCC	M_REQUEST	OE		LD7	LD6	LD5	LD4	T
U	D15	D14	D12	D11		D0	NVCC22	NVCC22	NVCC22	NVCC22	NVCC21	SVCC	SGND	MGND	MVCC	FGND	CS0	M_GRANT		LD12	NC	LD10	LD9	U
V	D10	D9	D6	D3		NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	A22	A20	A18	A16	A10	SDCKE1	LBA	RW		LD16	LD15	LD14	LD13	V
W	D7	D5	D2	D1																BCLK	EB1	EB0	LD17	W
Y	GND	MA10	A13	A8	A4	A0	SDBA1	A25	A24	A23	A21	A19	A17	A15	A14	DQM1	SDCKE0	CS2	CS3	CS4	ECB	CS1	GND	Y
AA	GND	GND	A12	A7	A3	SDBA0	SD30	SD28	SD24	SD20	SD17	SD15	SD12	SD9	SD6	SD4	SD1	DQM2	RAS	CAS	CS5	GND	GND	AA
AB	GND	GND	A11	A6	A2	SDQS3	SD29	SD26	SDQS2	SD21	SD18	SDQS1	SD13	SD10	SD7	SDQS0	SD2	DQM3	DQM0	SDWE	GND	GND	GND	AB
AC	GND	GND	A9	A5	A1	SD31	SD27	SD25	SD23	SD22	SD19	SD16	SD14	SD11	SD8	SD5	SD3	SD0	$\overline{SDCLK}$	SDCLK	GND	GND	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
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+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
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Document Number: MCIMX31
Rev. 4.1
11/2008

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