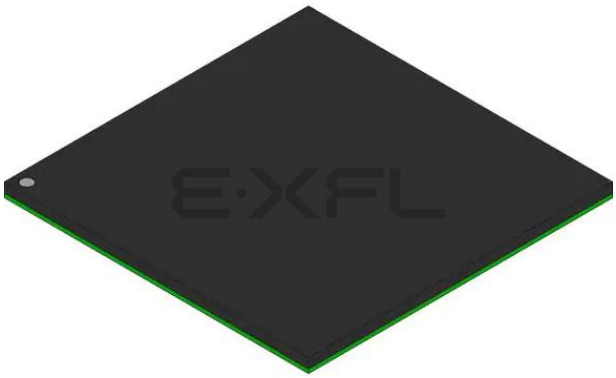

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	272-LFBGA
Supplier Device Package	272-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g2dvk05aa

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
QSPI	QSPI	Y	Y	Y	Y
SDIO	uSDHC1	Y	Y	Y	Y
	uSDHC2	Y	Y	Y	Y
UART	UART1	Y	Y	Y	Y
	UART2	Y	Y	Y	Y
	UART3	Y	Y	Y	Y
	UART4	Y	Y	Y	Y
	UART5	NA	Y	Y	Y
	UART6	NA	Y	Y	Y
	UART7	NA	Y	Y	Y
	UART8	NA	Y	Y	Y
ISO7816-3	SIM1	NA	Y	Y	Y
	SIM2	NA	Y	Y	Y
I2C	I2C1	Y	Y	Y	Y
	I2C2	Y	Y	Y	Y
	I2C3	NA	Y	Y	Y
	I2C4	NA	Y	Y	Y
SPI	ECSPI1	Y	Y	Y	Y
	ECSPI2	Y	Y	Y	Y
	ECSPI3	NA	Y	Y	Y
	ECSPI4	NA	Y	Y	Y
I2S/SAI	SAI1	Y	Y	Y	Y
	SAI2	NA	Y	Y	Y
	SAI3	NA	Y	Y	Y

- Four I^2C
- Two 10/100 Ethernet Controller (IEEE1588 compliant)
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- One Quad SPI
- Two Flexible Controller Area Network (FlexCAN)
- Three Watchdog timers (WDOG)
- Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total
- Touch Screen Controller (TSC)

The i.MX 6UltraLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme
- Two smart card interfaces compatible with EVM Standard 4.3

The i.MX 6UltraLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6UltraLite processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for imagine resize, rotation, overlay, and CSC[1]. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. CSU is configured during boot and by eFUSEs and determine the security level operation mode as well as the TZ policy.

1. G2 and G3 only

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6UltraLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

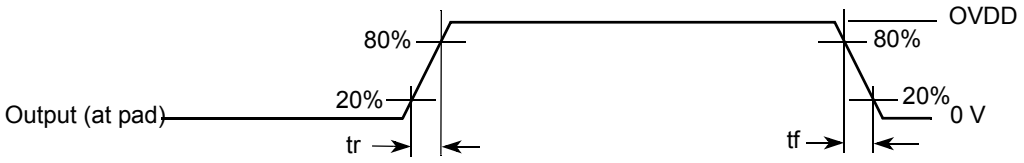

Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode
	8 Bit				16 Bit		16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	Reserved	Reserved	EIM_DATA [07:00]	Reserved	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	Reserved	Reserved	EIM_DATA [15:08]	Reserved	EIM_AD [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

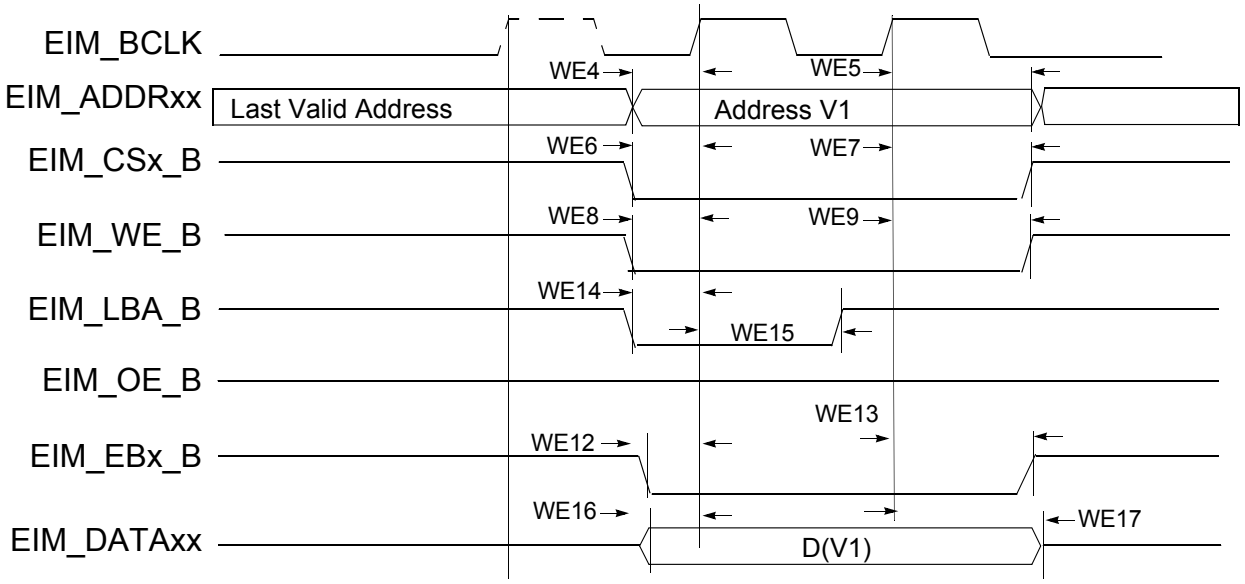

Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

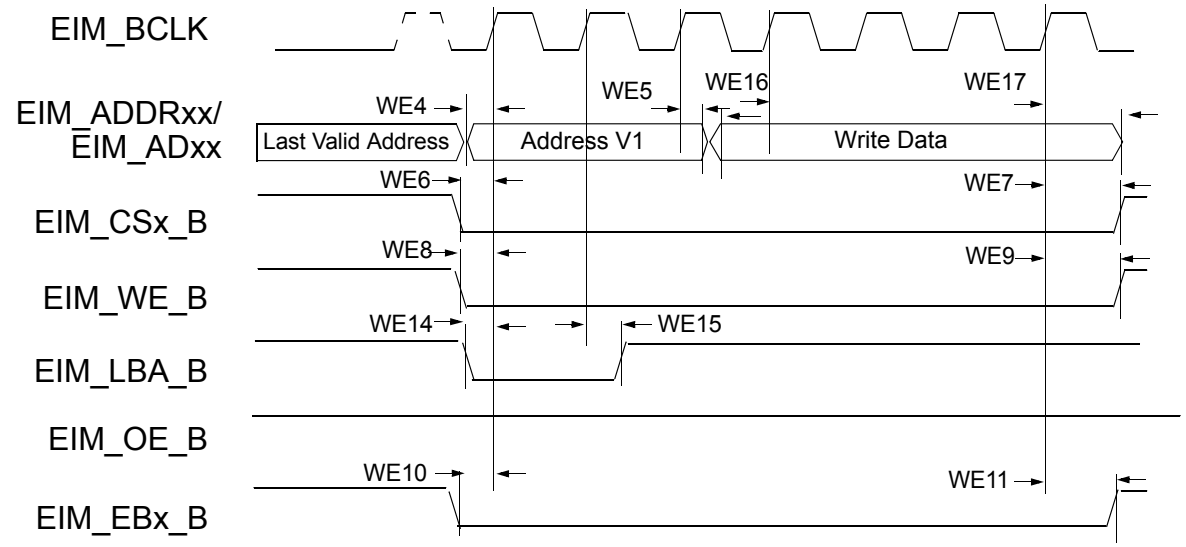

Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

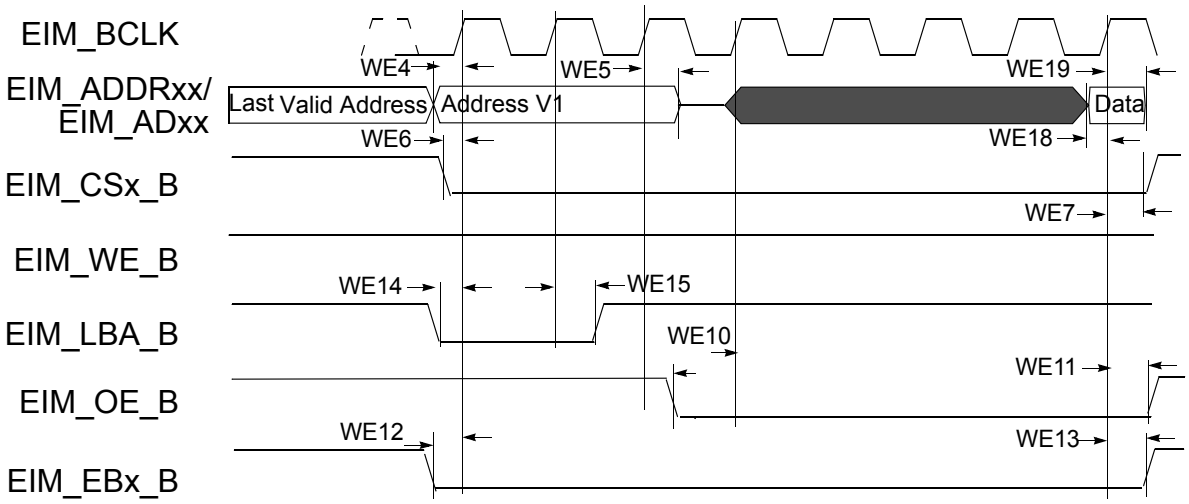

Figure 14. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 15 through Figure 19, and Table 40 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 15 through Figure 18 as RWSC, OEN and CSN is configured differently. See the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for the EIM programming model.

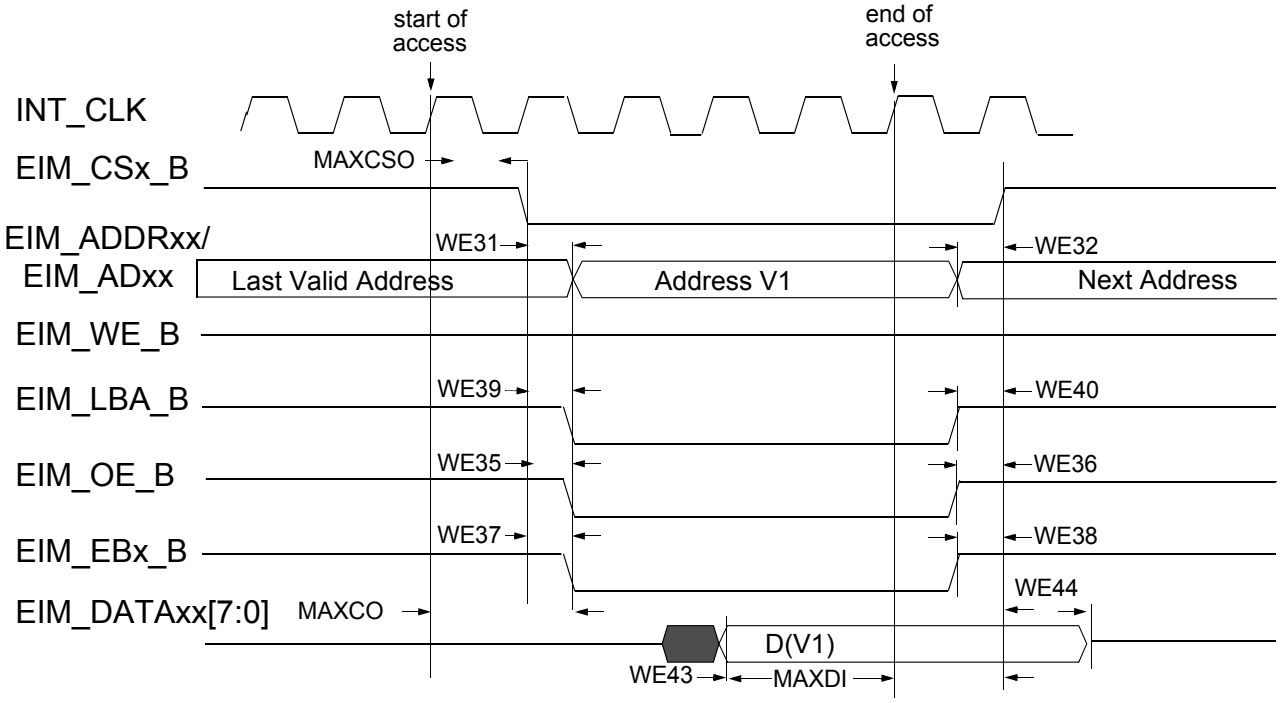

Figure 15. Asynchronous Memory Read Access (RWSC = 5)

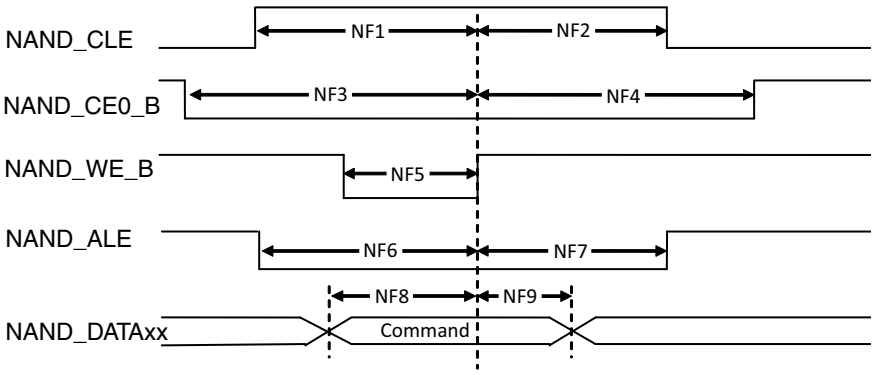

Figure 27. Command Latch Cycle Timing Diagram

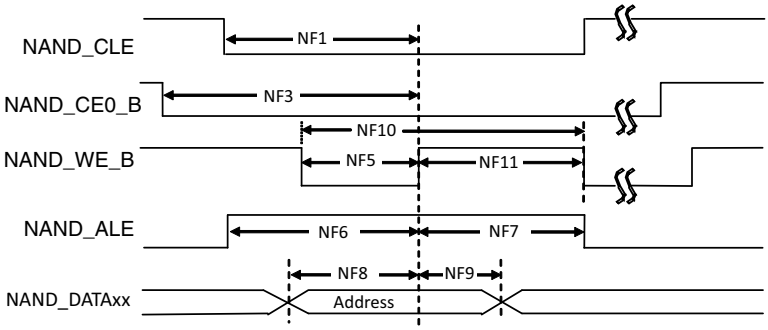

Figure 28. Address Latch Cycle Timing Diagram

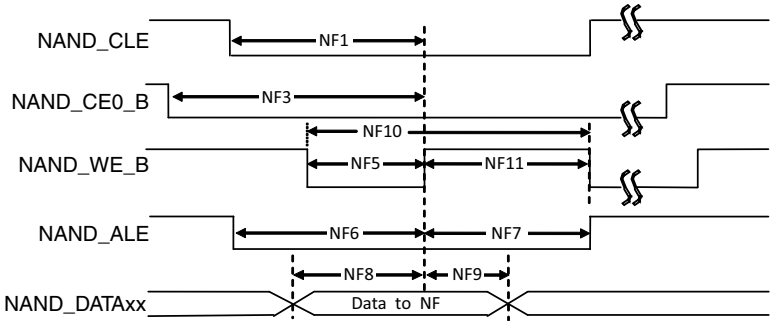

Figure 29. Write Data Latch Cycle Timing Diagram

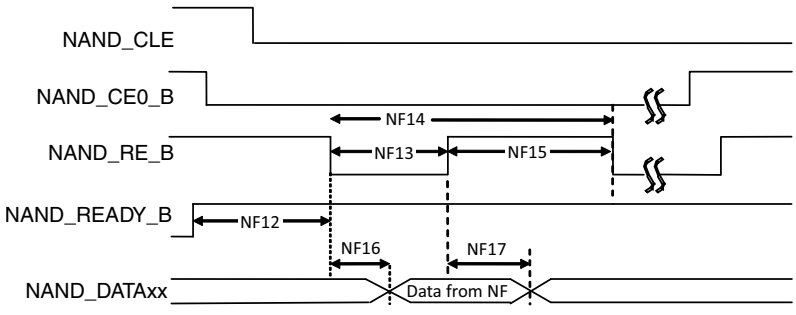

Figure 30. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

4.11.3.3 SDR50/SDR104 AC Timing

Figure 45 depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

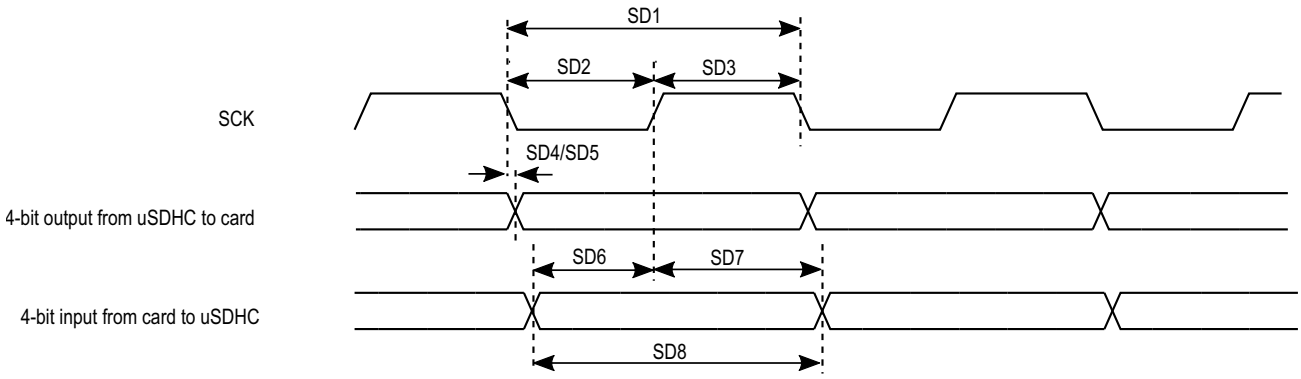

Figure 45. SDR50/SDR104 Timing

Table 56. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46*t_{CLK}	0.54*t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46*t_{CLK}	0.54*t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5*t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.11.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 53 depicts the timing of the PWM, and Table 64 lists the PWM timing parameters.

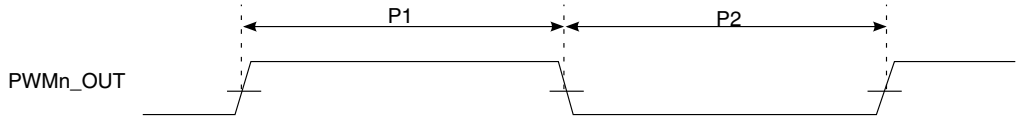

Figure 53. PWM Timing

Table 64. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.11.8 LCD Controller (LCDIF) Timing Parameters

Figure 54 shows the LCDIF timing and Table 65 lists the timing parameters.

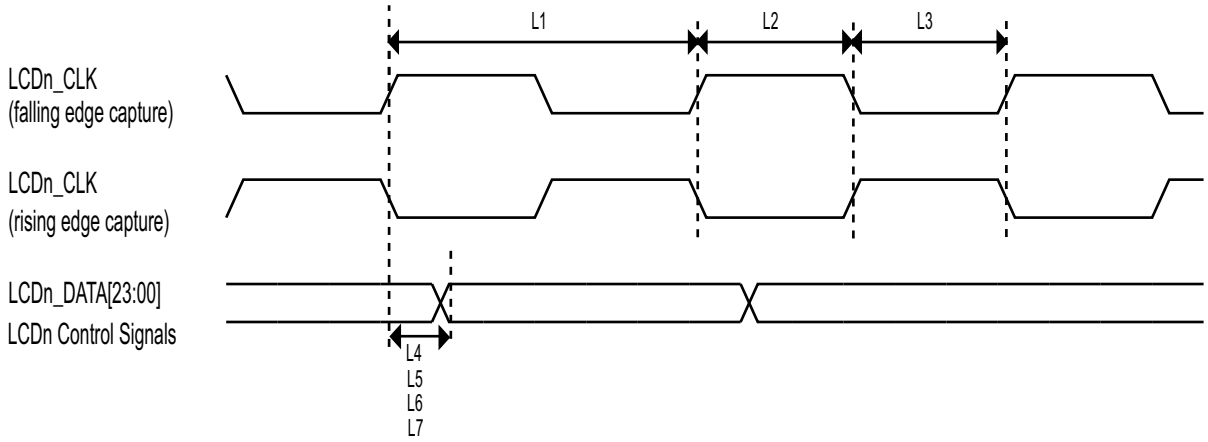

Figure 54. LCD Timing

4.11.13.1.2 UART Receiver

Figure 70 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

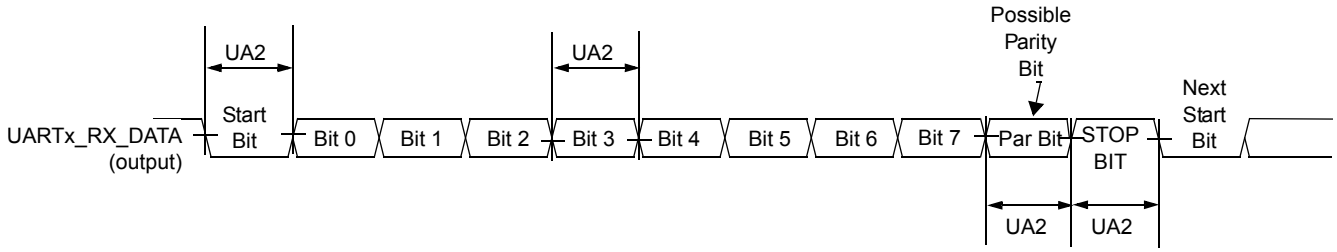

Figure 70. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.13.1.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 71 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

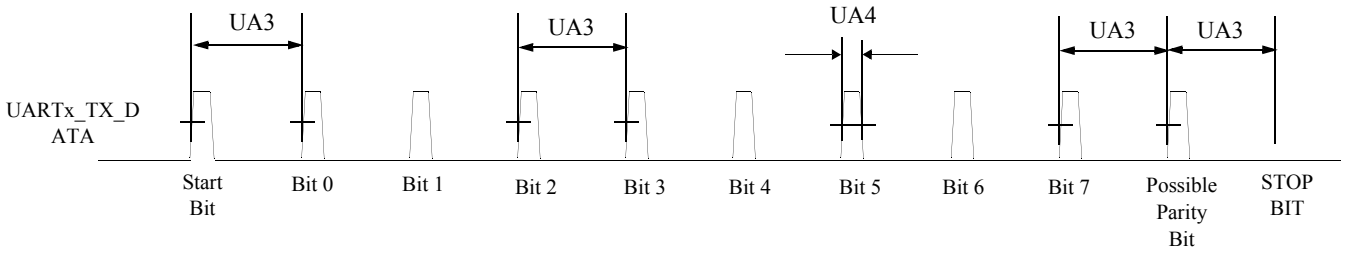

Figure 71. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 72 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

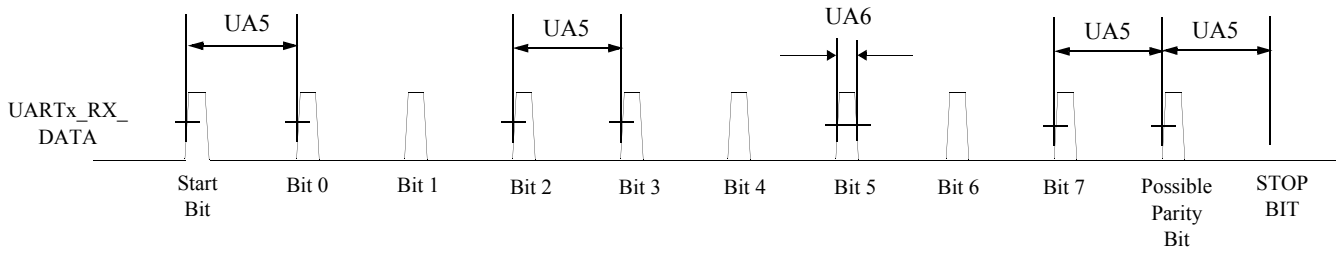

Figure 72. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.14 USB PHY Parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs

— Applies to: Universal Serial Bus Specification, Revision 2.0

- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  — Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  — Revision 1.2, December 7, 2010
  — Portable device only

4.12 A/D Converter

4.12.1 12-bit ADC Electrical Characteristics

4.12.1.1 12-bit ADC Operating Conditions

Table 80. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDAD)[2]	ΔVDDAD	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔVSSAD	-100	0	100	mV	—
Ref Voltage High	—	V_{REFH}	1.13	V_{DDAD}	V_{DDAD}	V	—
Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	—	5	7	kohms	—
	ADLPC=0, ADHSC=0		—	12.5	15	kohms	—
	ADLPC=1, ADHSC=0		—	25	30	kohms	—
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	—	—	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

[1] Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 81. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = (V_{REFH} - V_{REFL})/2 N	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		
[P:][C:] Integral Non-Linearity	12 bit mode	INL	—	2.6	—	LSB	—
	10bit mode		—	0.8	—		
	8 bit mode		—	0.3	—		
Zero-Scale Error	12 bit mode	E_{ZS}	—	-0.3	—	LSB	—
	10bit mode		—	-0.15	—		
	8 bit mode		—	-0.15	—		
Full-Scale Error	12 bit mode	E_{FS}	—	-2.5	—	LSB	—
	10bit mode		—	-0.6	—		
	8 bit mode		—	-0.3	—		
[L:] Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	—	Bits	—
[L:] Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	—

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm Package Information

6.1.1 14x14 mm, 0.8 mm Pitch, Ball Matrix

Figure 74 shows the top, bottom, and side views of the 14x14 mm BGA package.

Table 95. 14x14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

6.2.2 9x9 mm Supplies Contact Assignments and Functional Contact Assignments

Table 97 shows the device connection list for ground, sense, and reference contact signals.

Table 97. 9x9 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	N13	—
DRAM_VREF	T1	—
GPANAIO	T11	—
NGND_KEL0	M10	—
NVCC_CSI	E5	—
NVCC_DRAM	G5, L5, M5, N6	—
NVCC_DRAM_2P5	K6	—
NVCC_ENET	G13	—
NVCC_GPIO	M13	—
NVCC_LCD	E13	—
NVCC_NAND	E11	—
NVCC_PLL	T13	—
NVCC_SD1	E7	—
NVCC_UART	L13	—
VDD_ARM_CAP	G9, G10, G11, H9, H10, H11	—
VDD_HIGH_CAP	U11	—
VDD_HIGH_IN	U15	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G7, G8, H7, H8, J7, J8, K7, K8, L7, L8	—
VDD_SOC_IN	J9, J10, J11, K9, K10, K11, L9, L10, L11	—
VDD_USB_CAP	N11	—
VDDA_ADC_3P3	T17	—
VSS	A2, A7, A12, A17, B1, C15, F1, F3, F8, F10, F17, H6, H12, J3, J15, K12, M1, M3, M8, M17, R3, R9, R12, R15, U1, U6, U13, U17	—

6.2.3 9x9 mm, 0.5 mm Pitch, Ball Map

Table 99 shows the 9x9 mm, 0.5 mm pitch ball map for the i.MX 6UltraLite.

Table 99. 9x9 mm, 0.5 mm Pitch, Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A		VSS	CSI_DATA06	SD1_DATA1	SD1_DATA0	NAND_DATA05	VSS	NAND_WEB	NAND_DATA01	LCD_ENABLE	LCD_DATA04	VSS	LCD_DATA09	LCD_DATA13	LCD_DATA16	LCD_DATA15	VSS	A
B	VSS	CSI_DATA02	CSI_DATA05	SD1_DATA3	SD1_DATA2	NAND_CE1_B	NAND_CLE	NAND_DATA07	NAND_DATA06	LCD_HSYNC	LCD_DATA03	LCD_DATA01	LCD_DATA08	LCD_DATA14	LCD_DATA18	LCD_DATA22	LCD_DATA20	B
C	CSI_MCLK	CSI_DATA07	CSI_DATA00	CSI_DATA04	SD1_CLK	SD1_CMD	NAND_DATA03	NAND_DATA04	NAND_DATA02	LCD_VSYNC	LCD_CLK	LCD_DATA07	LCD_DATA11	LCD_DATA12	VSS	LCD_DATA21	LCD_DATA23	C
D	CSI_DATA03	CSI_HSYNC	CSI_VSYNC	CSI_DATA01	CSI_PIXCLK	NAND_WP_B	NAND_DATA00	NAND_ALE	NAND_RE_B	LCD_DATA02	LCD_DATA00	LCD_DATA05	LCD_DATA06	LCD_DATA10	LCD_DATA17	ENET2_RX_EN	ENET2_RX_DATA1	D
E	DRAM_ODT1	DRAM_ADDR15	DRAM_ADDR14	DRAM_ADDR06	NVCC_CSI	NAND_DQS	NVCC_SD1	NAND_CE0_B	NAND_READY_B	LCD_RESET	NVCC_NAND	LCD_DATA19	NVCC_LCD	ENET2_TX_DATA0	ENET2_TX_EN	ENET1_TX_DATA0	ENET2_RX_DATA0	E
F	VSS	DRAM_RESET	VSS	DRAM_SDWE_B	DRAM_SDBA1			VSS		VSS			ENET1_TX_DATA1	ENET2_TX_DATA1	ENET1_TX_EN	ENET1_RX_DATA1	VSS	F
G	DRAM_ADDR00	DRAM_ADDR01	DRAM_SDBA2	DRAM_CAS_B	NVCC_DRAM		VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP		NVCC_ENET	ENET1_RX_ER	ENET1_TX_CLK	ENET1_RX_EN	ENET1_RX_DATA0	G

7 Revision History

Table 101 provides a revision history for this data sheet.

Table 101. i.MX 6UltraLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
0	08/2015	• Initial release
0.1	01/2015	• Updated Table 1 Ordering Information • Added Table 2 Detailed peripherals information
0.2	02/2015	• Updated Figure 2 i.MX 6UltraLite System Block Diagram • Updated Table 39 EIM Bus Timing Parameters and Table 40 EIM Asynchronous Timing Parameters Relative to Chip Select • Updated Table 96 14x14 mm Functional contact Assignments and Table 99 9x9 mm Functional contact Assignments • Updated Figure 71 UART IrDA Mode Transmit Timing Diagram and Figure 72 UART IrDA Mode Transmit Timing Diagram • Added Table 100 GPIO behaviors during reset
0.3	03/2016	• Updated Figure 1 Part Number Nomenclature—i.MX 6UltraLite • Updated Table 1 Ordering Information • Updated Table 3 i.MX 6UltraLite Modules List
1	04/2016	• Updated Table 3 i.MX 6UltraLite Module list for BCH descriptions • Updated Table 4 Special Signal Considerations • Added a note for Table 9 14x14 MM Package Thermal Resistance • UpdatedTable 15 Low Power Mode Current and Power Consumption • Added a note for Table 23 XTALI and RTC_XTALI DC Parameters • Updated Table 38 EIM Internal Module Multiplexing • Updated Table 56 SDR50/SDR104 Interface Timing Specification • Updated Table 95 14x14 mm Functional Contact Assignments and footnote • Updated Section 4.1.1, “Absolute Maximum Ratings • Updated Section 4.6.3, “DDR I/O DC Parameters • Added Section 4.11.8, “LCD Controller (LCDIF) Timing Parameters • Updated Section 4.11.9, “QUAD SPI (QSPI) Timing Parameters