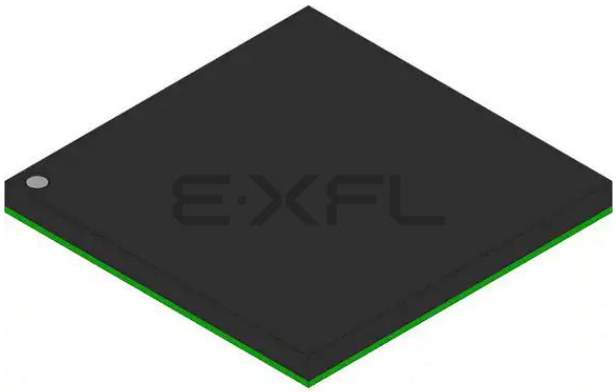

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g2dvm05aa

- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Smart appliances

The features of the i.MX 6UltraLite processor include[1]:

- Single-core ARM Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of each device is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The device supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—Multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- Ethernet interfaces—10/100 Mbps Ethernet controllers.
- Human-machine interface—Support digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, multiple expansion card port (high-speed MMC/SDIO host and other), 12-bit ADC module, CAN port, smart card interface compatible with EMV Standard v4.3, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6UltraLite Security Reference Manual* (IMX6ULSRM).
- Integrated power management—The processor integrates linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6UltraLite features, see Section 1.2, “Features”.

1. The actual feature set depends on the part numbers as described in the Table 1 and Table 2.

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
QSPI	QSPI	Y	Y	Y	Y
SDIO	uSDHC1	Y	Y	Y	Y
	uSDHC2	Y	Y	Y	Y
UART	UART1	Y	Y	Y	Y
	UART2	Y	Y	Y	Y
	UART3	Y	Y	Y	Y
	UART4	Y	Y	Y	Y
	UART5	NA	Y	Y	Y
	UART6	NA	Y	Y	Y
	UART7	NA	Y	Y	Y
	UART8	NA	Y	Y	Y
ISO7816-3	SIM1	NA	Y	Y	Y
	SIM2	NA	Y	Y	Y
I2C	I2C1	Y	Y	Y	Y
	I2C2	Y	Y	Y	Y
	I2C3	NA	Y	Y	Y
	I2C4	NA	Y	Y	Y
SPI	ECSPI1	Y	Y	Y	Y
	ECSPI2	Y	Y	Y	Y
	ECSPI3	NA	Y	Y	Y
	ECSPI4	NA	Y	Y	Y
I2S/SAI	SAI1	Y	Y	Y	Y
	SAI2	NA	Y	Y	Y
	SAI3	NA	Y	Y	Y

4.3.1 Digital Regulators (LDO_ARM, LDO_SOC)

There are two digital LDO regulators ("Digital", because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 11 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 11 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

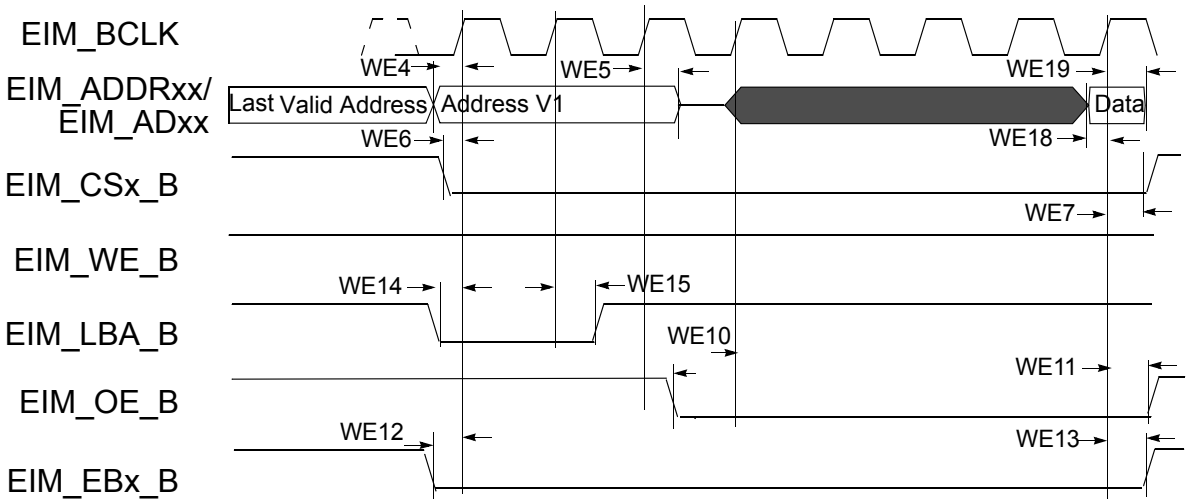


Figure 14. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 15 through Figure 19, and Table 40 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 15 through Figure 18 as RWSC, OEN and CSN is configured differently. See the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for the EIM programming model.

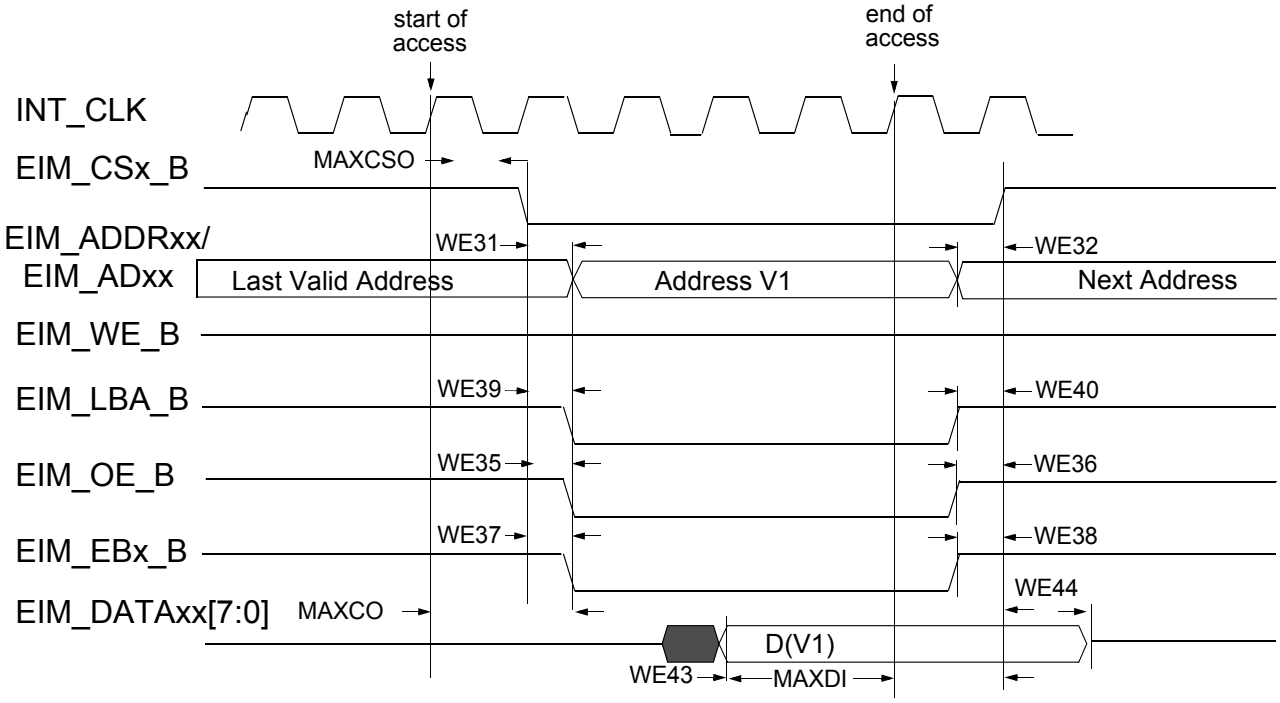


Figure 15. Asynchronous Memory Read Access (RWSC = 5)

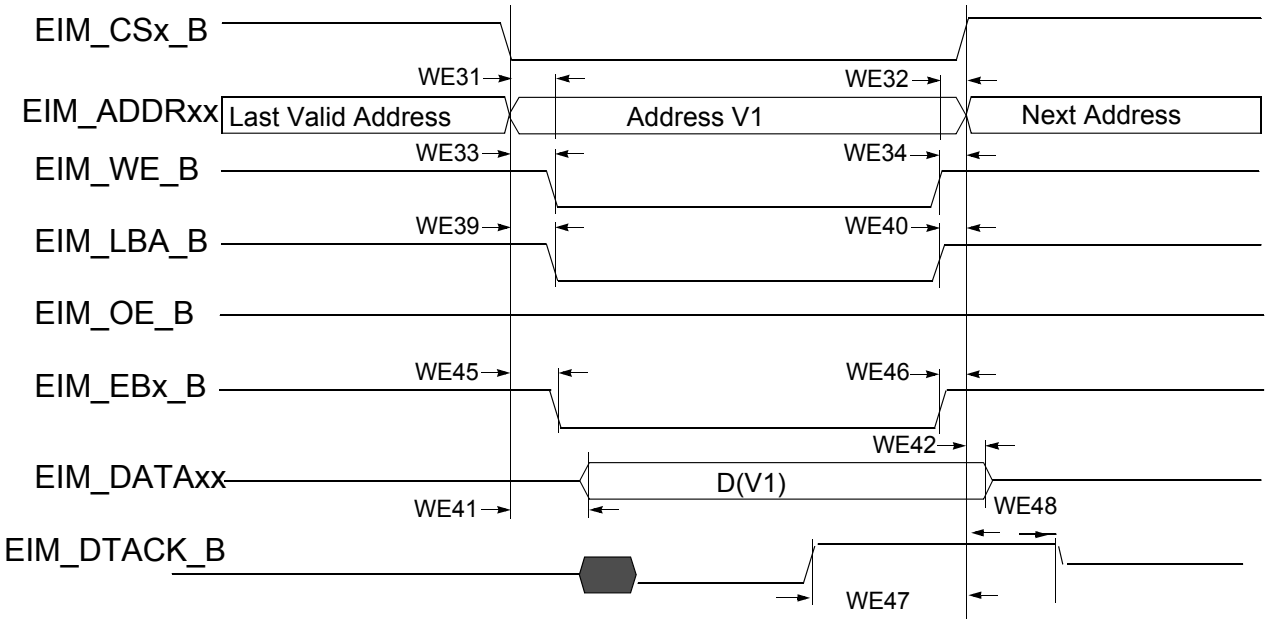


Figure 20. DTACK Mode Write Access (DAP=0)

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA x t	-3.5 - CSA x t	3.5 - CSA x t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7 - WE5 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE32A(muxed A/D	EIM_CSx_B valid to Address Invalid	t + WE4 - WE7 + (ADVN + ADVA + 1 - CSA) x t	t - 3.5 + (ADVN + ADVA + 1 - CSA) x t	t + 3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA) x t	-3.5 + (WEA - WCSA) x t	3.5 + (WEA - WCSA) x t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN) x t	-3.5 + (WEN - WCSN) x t	3.5 + (WEN - WCSN) x t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA) x t	-3.5 + (OEA - RCSA) x t	3.5 + (OEA - RCSA) x t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	-3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN) x t	-3.5 + (OEN - RCSN) x t	3.5 + (OEN - RCSN) x t	ns

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.10.3.2 Read and Write Timing

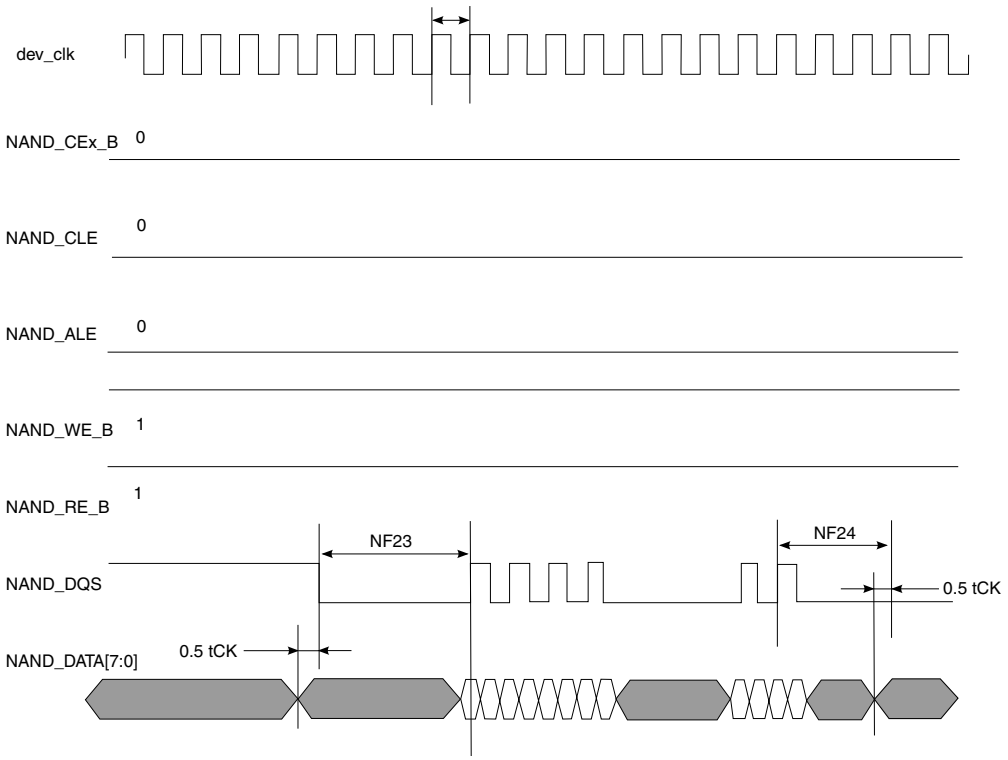


Figure 36. Samsung Toggle Mode Data Write Timing

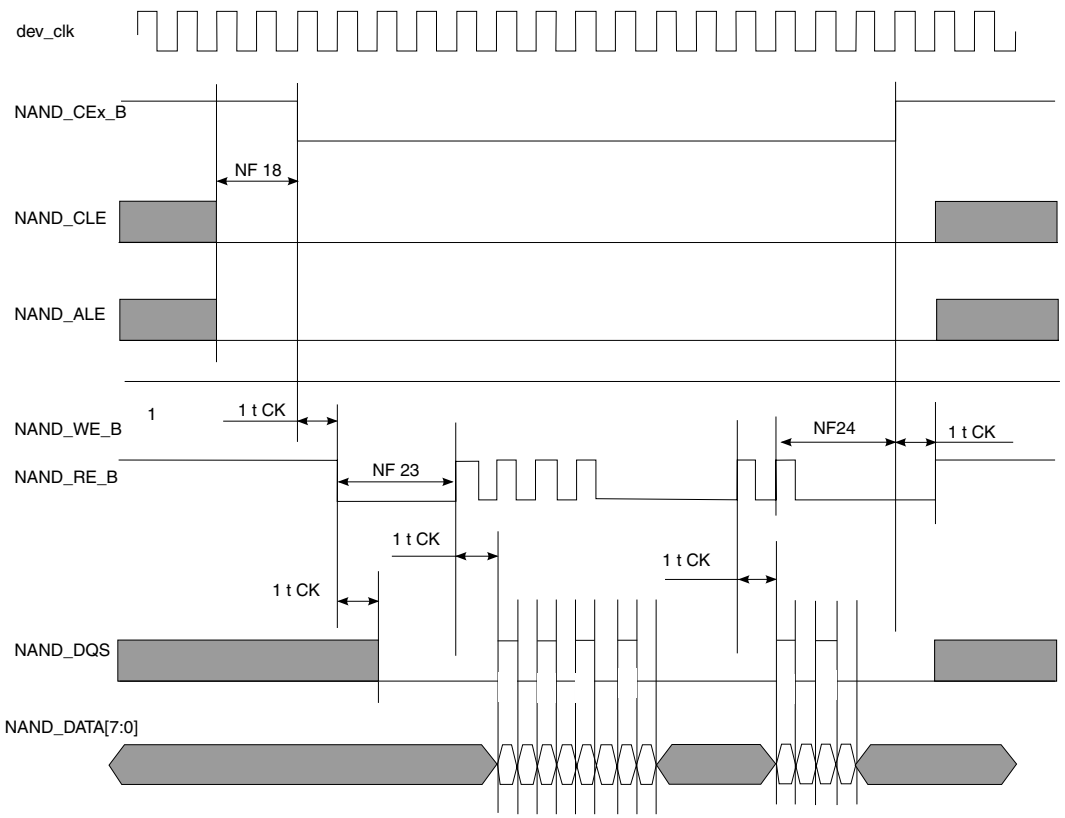


Figure 37. Samsung Toggle Mode Data Read Timing

Table 49. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see [3,2]]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see [2]]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see [2]]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see [2]]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see [2]]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see [4,2]]	—	ns
NF22	Clock period	tCK	—	—	ns
NF23	Preamble delay	tPRE	PRE_DELAY × T [see [5,2]]	—	ns
NF24	Postamble delay	tPOST	POST_DELAY × T +0.43 [see [2]]	—	ns

The following subsections describe the CSI timing in gated and ungated clock modes.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 41 depicts the timing of ECSPI in master mode. Table 52 lists the ECSPI master mode timing characteristics.

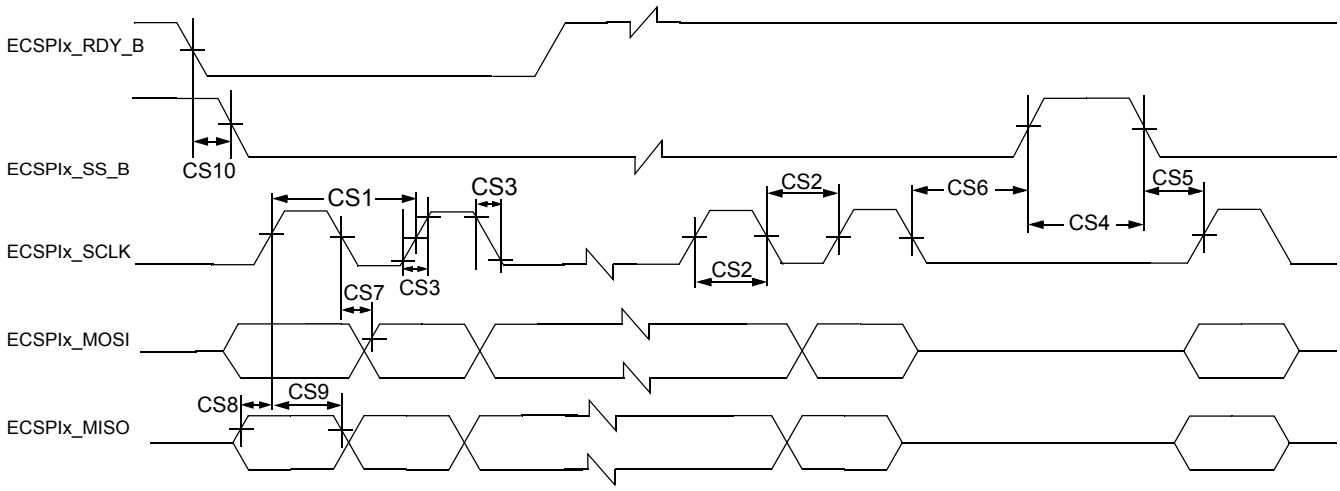


Figure 41. ECSPI Master Mode Timing Diagram

Table 52. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

Table 54. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.3.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 44 depicts the timing of eMMC4.4/4.41. Table 55 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

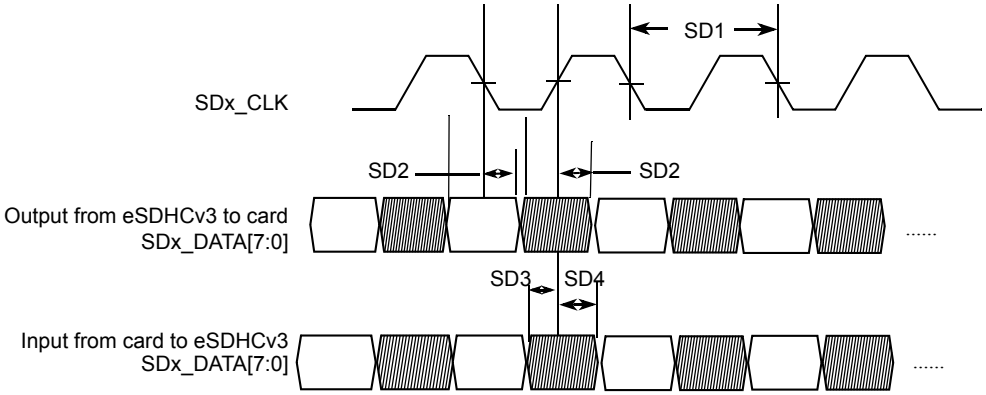


Figure 44. eMMC4.4/4.41 Timing

Table 55. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.11.3.3 SDR50/SDR104 AC Timing

Figure 45 depicts the timing of SDR50/SDR104, and Table 56 lists the SDR50/SDR104 timing characteristics.

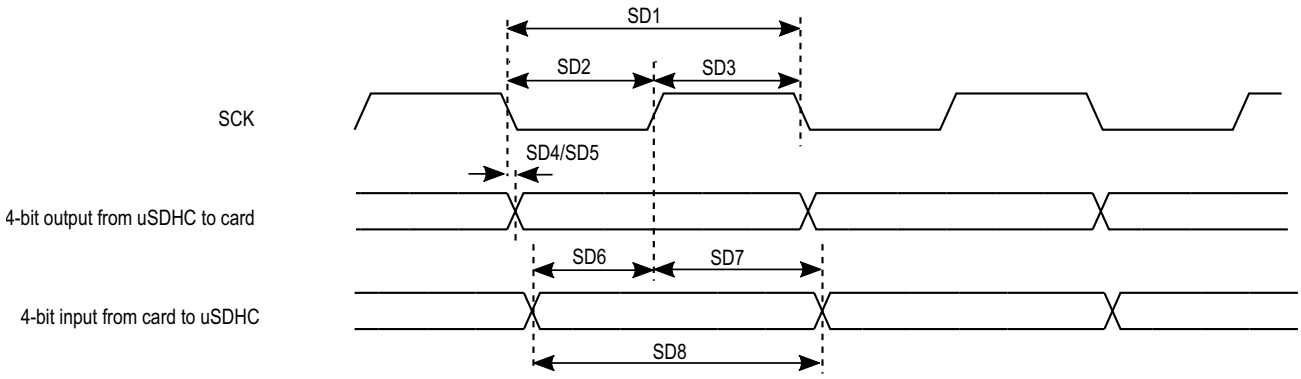


Figure 45. SDR50/SDR104 Timing

Table 56. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46*t_{CLK}	0.54*t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46*t_{CLK}	0.54*t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5*t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

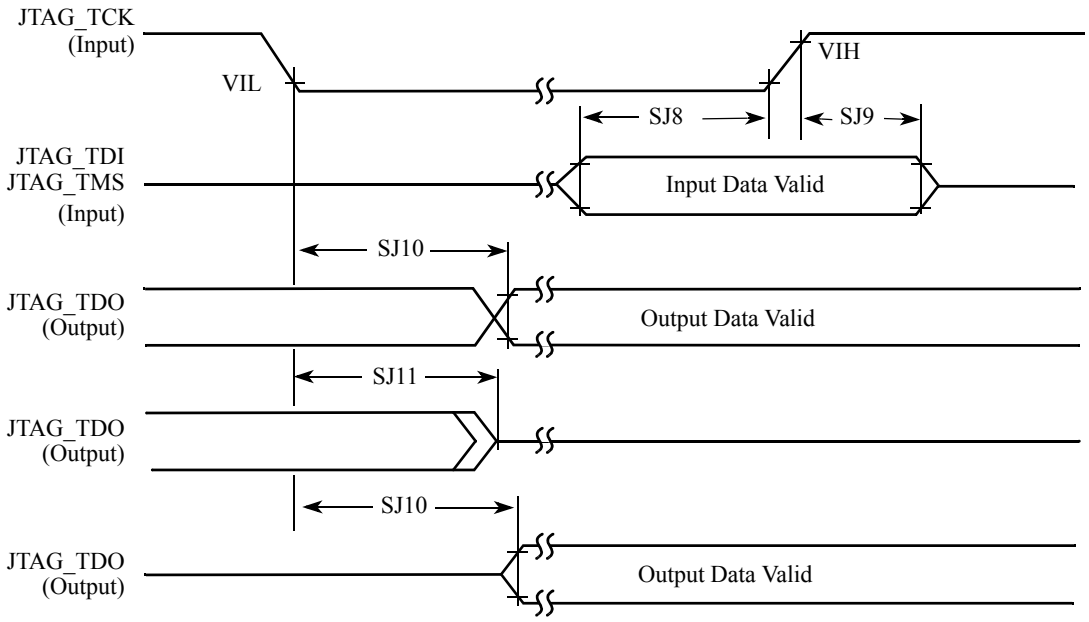


Figure 65. Test Access Port Timing Diagram

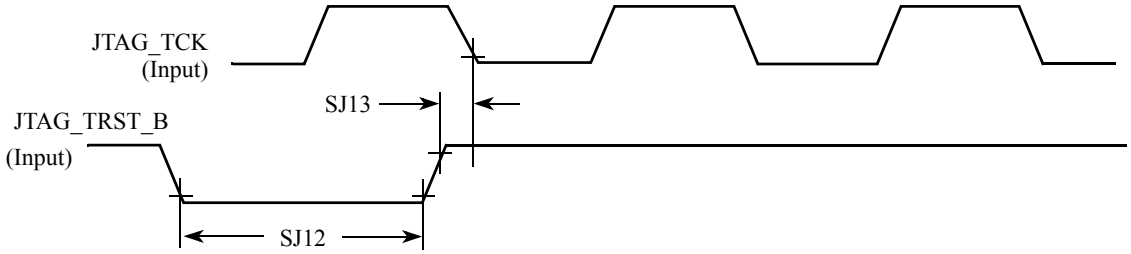


Figure 66. JTAG_TRST_B Timing Diagram

Table 74. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

4.11.13.1.2 UART Receiver

Figure 70 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

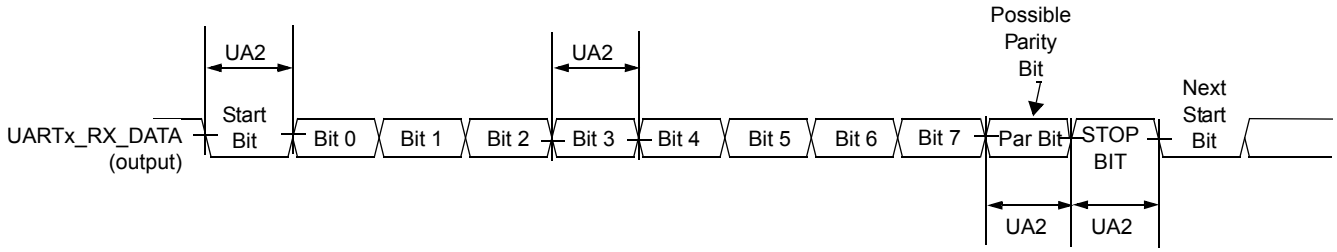


Figure 70. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.13.1.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 71 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

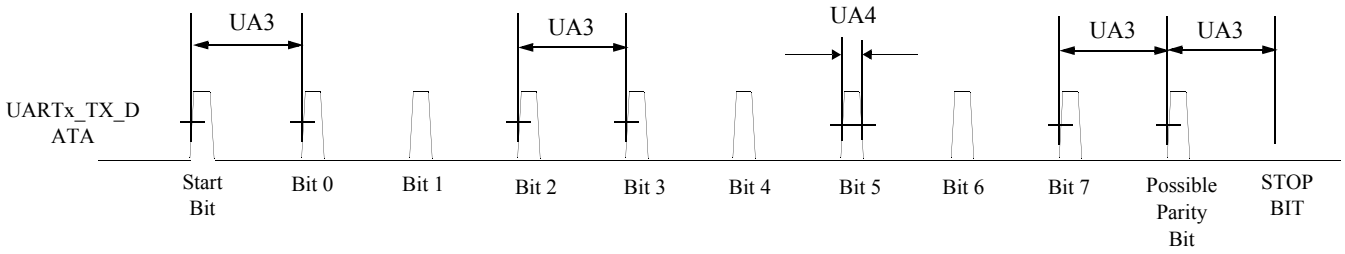


Figure 71. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 81. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp	—	2	—	cycles	—
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			

Table 82. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot Device Interface Allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 83. QSPI Boot trough QSPI

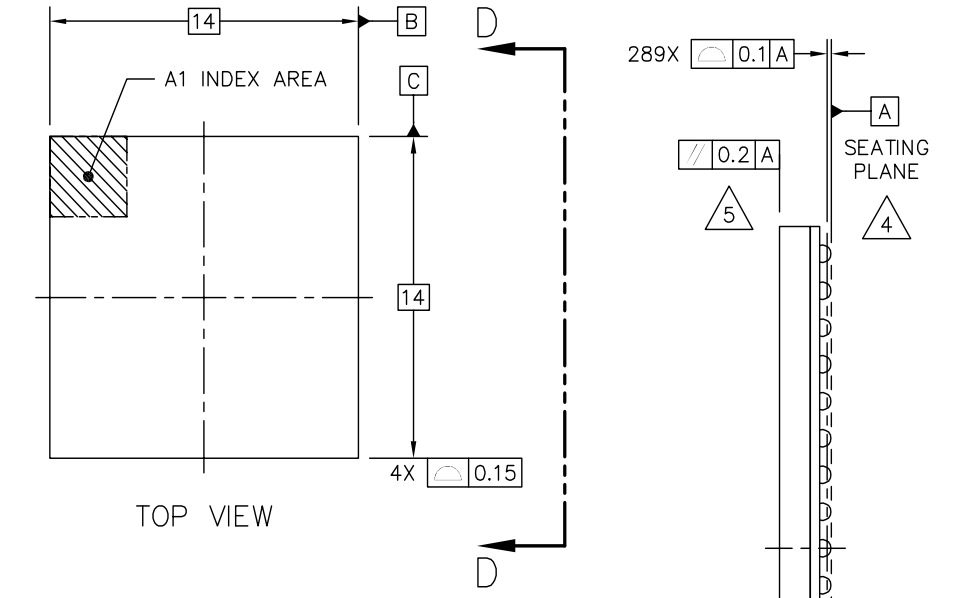
Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

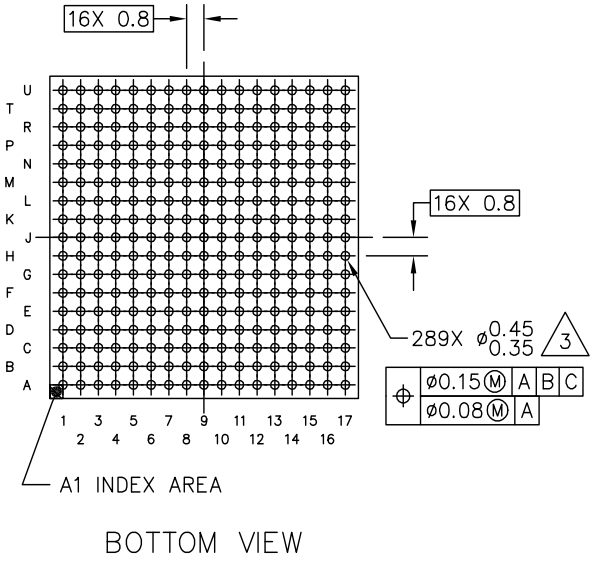
Table 91. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
NAND_ALE	weim.ADDR[17]	Alt 4		Yes	Yes
NAND_CE1_B	weim.ADDR[18]	Alt 4		Yes	Yes
SD1_CMD	weim.ADDR[19]	Alt 4		Yes	Yes
SD1_CLK	weim.ADDR[20]	Alt 4		Yes	Yes
SD1_DATA0	weim.ADDR[21]	Alt 4		Yes	Yes
SD1_DATA1	weim.ADDR[22]	Alt 4		Yes	Yes
SD1_DATA2	weim.ADDR[23]	Alt 4		Yes	Yes
SD1_DATA3	weim.ADDR[24]	Alt 4		Yes	Yes
ENET2_RXER	weim.ADDR[25]	Alt 4		Yes	Yes
ENET2_CRS_DV	weim.ADDR[26]	Alt 4		Yes	Yes
CSI_MCLK	weim.CS0_B	Alt 4	Yes		
LCD_DATA08	weim.DATA[0]	Alt 4		Yes	
LCD_DATA09	weim.DATA[1]	Alt 4		Yes	
LCD_DATA10	weim.DATA[2]	Alt 4		Yes	
LCD_DATA11	weim.DATA[3]	Alt 4		Yes	
LCD_DATA12	weim.DATA[4]	Alt 4		Yes	
LCD_DATA13	weim.DATA[5]	Alt 4		Yes	
LCD_DATA14	weim.DATA[6]	Alt 4		Yes	
LCD_DATA15	weim.DATA[7]	Alt 4		Yes	
LCD_DATA16	weim.DATA[8]	Alt 4		Yes	
LCD_DATA17	weim.DATA[9]	Alt 4		Yes	
LCD_DATA18	weim.DATA[10]	Alt 4		Yes	
LCD_DATA19	weim.DATA[11]	Alt 4		Yes	
LCD_DATA20	weim.DATA[12]	Alt 4		Yes	
LCD_DATA21	weim.DATA[13]	Alt 4		Yes	
LCD_DATA22	weim.DATA[14]	Alt 4		Yes	
LCD_DATA23	weim.DATA[15]	Alt 4		Yes	
NAND_RE_B	weim.EB_B[0]	Alt 4		Yes	Yes
NAND_WE_B	weim.EB_B[1]	Alt 4		Yes	Yes
CSI_HSYNC	weim.LBA_B	Alt 4	Yes		
CSI_PIXCLK	weim.OE	Alt 4	Yes		
CSI_VSYNC	weim.RW	Alt 4	Yes		

MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING





TITLE: MAPBGA, 14 X 14 X 1.18 PKG, 0.8 MM PITCH, 289 I/O	DOCUMENT NO: 98ASA00855D REV: O
	STANDARD: NON–JEDEC
	SHEET: 1 OF 3

Table 95 shows an alpha-sorted list of functional contact assignments for the 14x14 mm package.

Table 95. 14x14 mm Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	P16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	P17	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U9	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	—
CSI_DATA00	E4	NVCC_CSI	GPIO	ALT5	CSI_DATA00	Input	Keeper
CSI_DATA01	E3	NVCC_CSI	GPIO	ALT5	CSI_DATA01	Input	Keeper
CSI_DATA02	E2	NVCC_CSI	GPIO	ALT5	CSI_DATA02	Input	Keeper
CSI_DATA03	E1	NVCC_CSI	GPIO	ALT5	CSI_DATA03	Input	Keeper
CSI_DATA04	D4	NVCC_CSI	GPIO	ALT5	CSI_DATA04	Input	Keeper
CSI_DATA05	D3	NVCC_CSI	GPIO	ALT0	CSI_DATA05	Input	Keeper
CSI_DATA06	D2	NVCC_CSI	GPIO	ALT5	CSI_DATA06	Input	Keeper
CSI_DATA07	D1	NVCC_CSI	GPIO	ALT5	CSI_DATA07	Input	Keeper
CSI_HSYNC	F3	NVCC_CSI	GPIO	ALT5	CSI_HSYNC	Input	Keeper
CSI_MCLK	F5	NVCC_CSI	GPIO	ALT5	CSI_MCLK	Input	Keeper
CSI_PIXCLK	E5	NVCC_CSI	GPIO	ALT5	CSI_PIXCLK	Input	Keeper
CSI_VSYNC	F2	NVCC_CSI	GPIO	ALT5	CSI_VSYNC	Input	Keeper
DRAM_ADDR00	L5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	K1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	K4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	L1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 95. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 98. 9x9 mm Functional Contact Assignments (continued)

LCD_ENABLE	A10	NVCC_LCD	GPIO	ALT5	LCD_ENABLE	Input	Keeper
LCD_HSYNC	B10	NVCC_LCD	GPIO	ALT5	LCD_HSYNC	Input	Keeper
LCD_RESET	E10	NVCC_LCD	GPIO	ALT5	LCD_RESET	Input	Keeper
LCD_VSYNC	C10	NVCC_LCD	GPIO	ALT5	LCD_VSYNC	Input	Keeper
NAND_ALE	D8	NVCC_NAND	GPIO	ALT5	VDDSOC	Input	Keeper
NAND_CE0_B	E8	NVCC_NAND	GPIO	ALT5	NAND_CE0_B	Input	Keeper
NAND_CE1_B	B6	NVCC_NAND	GPIO	ALT5	NAND_CE1_B	Input	Keeper
NAND_CLE	B7	NVCC_NAND	GPIO	ALT5	NAND_CLE	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	NAND_DATA00	Input	Keeper
NAND_DATA01	A9	NVCC_NAND	GPIO	ALT5	NAND_DATA01	Input	Keeper
NAND_DATA02	C9	NVCC_NAND	GPIO	ALT5	NAND_DATA02	Input	Keeper
NAND_DATA03	C7	NVCC_NAND	GPIO	ALT5	NAND_DATA03	Input	Keeper
NAND_DATA04	C8	NVCC_NAND	GPIO	ALT5	NAND_DATA04	Input	Keeper
NAND_DATA05	A6	NVCC_NAND	GPIO	ALT5	NAND_DATA05	Input	Keeper
NAND_DATA06	B9	NVCC_NAND	GPIO	ALT5	NAND_DATA06	Input	Keeper
NAND_DATA07	B8	NVCC_NAND	GPIO	ALT5	NAND_DATA07	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	NAND_DQS	Input	Keeper
NAND_RE_B	D9	NVCC_NAND	GPIO	ALT5	NAND_RE_B	Input	Keeper
NAND_READY_B	E9	NVCC_NAND	GPIO	ALT5	NAND_READY_B	Input	Keeper
NAND_WE_B	A8	NVCC_NAND	GPIO	ALT5	NAND_WE_B	Input	Keeper
NAND_WP_B	D6	NVCC_NAND	GPIO	ALT5	NAND_WP_B	Input	Keeper
ONOFF	R6	VDD_SNVS_IN	GPIO	ALT0	ONOFF	Input	100 kΩ pull-up
POR_B	R10	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
RTC_XTALI	T12	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U12	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C5	NVCC_SD	GPIO	ALT5	SD1_CLK	Input	Keeper
SD1_CMD	C6	NVCC_SD	GPIO	ALT5	SD1_CMD	Input	Keeper
SD1_DATA0	A5	NVCC_SD	GPIO	ALT5	SD1_DATA0	Input	Keeper
SD1_DATA1	A4	NVCC_SD	GPIO	ALT5	SD1_DATA1	Input	Keeper
SD1_DATA2	B5	NVCC_SD	GPIO	ALT5	SD1_DATA2	Input	Keeper
SD1_DATA3	B4	NVCC_SD	GPIO	ALT5	SD1_DATA3	Input	Keeper
SNVS_PMIC_ON_REQ	T7	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up

Table 98. 9x9 mm Functional Contact Assignments (continued)

USB_OTG1_DN	R11	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	P11	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T9	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T10	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U10	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U9	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T14	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	U14	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0]. When the pad is configured as GPIO, the value is keeper out of reset.

[2] SNVS_TAMPER0 to SNVS_TAMPER9 is input floating in the following conditions.

—SNVS low power mode when configured as GPIO

—Tamper functions are not used when configured as TAMPER detection pins

It is required to connect external 1M Ohm pull-up or pull-down resistors to the pad to avoid the undesired leakage under two conditions above.