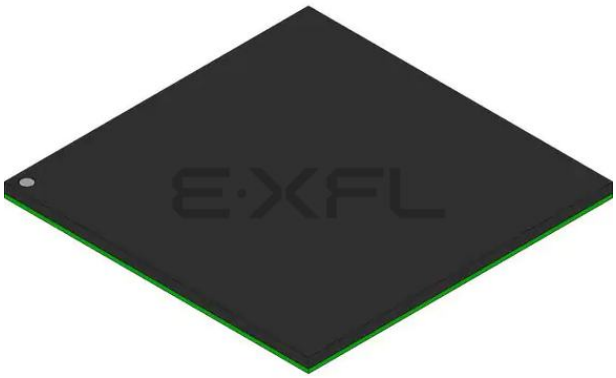

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	272-LFBGA
Supplier Device Package	272-MAPBGA (9x9)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g3dvk05aa

- Four I^2C
- Two 10/100 Ethernet Controller (IEEE1588 compliant)
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- One Quad SPI
- Two Flexible Controller Area Network (FlexCAN)
- Three Watchdog timers (WDOG)
- Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total
- Touch Screen Controller (TSC)

The i.MX 6UltraLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme
- Two smart card interfaces compatible with EVM Standard 4.3

The i.MX 6UltraLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6UltraLite processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for imagine resize, rotation, overlay, and CSC[1]. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. CSU is configured during boot and by eFUSEs and determine the security level operation mode as well as the TZ policy.

1. G2 and G3 only

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6UltraLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6UltraLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
System Counter	—	—	The system counter module is a programmable system counter which provides a shared time base to the Cortex A series cores as part of ARM's generic timer architecture. It is intended for use in application where the counter is always powered on and supports multiple, unrelated clocks.
TSC	Touch Screen	Touch Controller	With touch controller to support 4-wire and 5-wire resistive touch panel.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6 UART7 UART8	UART Interface	Connectivity Peripherals	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 4. Special Signal Considerations (continued)

Signal Name	Remarks
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 5. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6UltraLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for Freescale factory use. The user must tie this pin directly to GND.

Table 5. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

1 As per JEDEC JESD51-2 the intent of (thermal resistance) measurement is soley for a thermal performance comparison of one package to another in a standardized enviroment. This methodology is not meant to and will not predict the performance of a package in an application-specific enviroment.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

8 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.2.2 9x9 MM (VK) Package Thermal Resistance

Table 10 displays the 9x9 MM (VK) thermal resistance data.

Table 10. 9x9 MM (VK) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	65.6	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	36.2	°C/W	2,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	51.2	°C/W	2,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	31.8	°C/W	2,3
Junction to Board	—	$R_{\theta JB}$	17.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	14.5	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB_CSB}	11.1	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistances between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating Ranges

Table 11 provides the operating ranges of the i.MX 6UltraLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 11. Operating Ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode: LDO Enabled	VDD_SOC_IN	—	1.275	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
	VDD_ARM_CAP	A7 core at 528 MHz	1.15	—	1.3	V	Output voltage must be set to the following rules: • VDD_ARM_CAP <= VDD_SOC_CAP • VDD_SOC_CAP - VDD_ARM_CAP < 330 mV
		A7 core at 396 MHz	1.00	—	1.3		
		A7 core at 198 MHz	0.925	—	1.3		
	VDD_SOC_CAP	—	1.15	—	1.3	V	—
Run Mode: LDO Bypassed	VDD_SOC_IN	A7 core operation at 528 MHz or below	1.15	—	1.3	V	A7 core operation above 528 MHz is not supported when LDO is bypassed.
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.90	—	1.3	V	Refer to Table 15 Low Power Mode Current and Power Consumption on page 15
VDD_HIGH internal Regulator	VDD_HIGH_IN	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[2]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—
DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

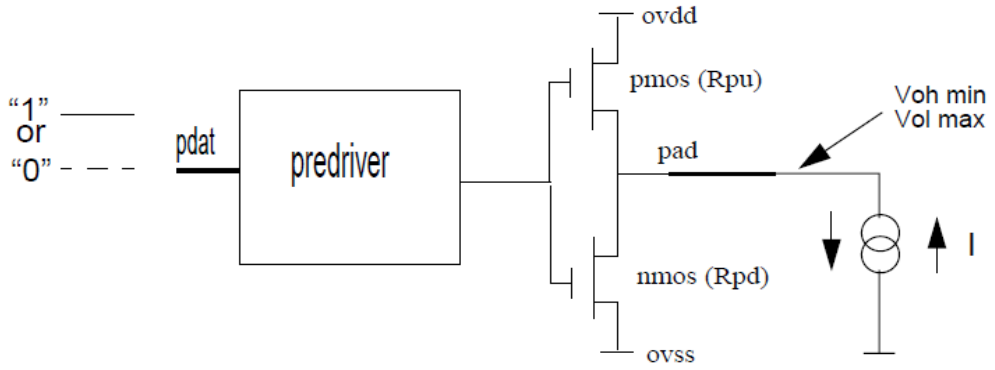

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 23 shows the DC parameters for the clock inputs.

Table 23. XTALI and RTC_XTALI DC Parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.2	V

1 The DC parameters are for external clock input only.

4.6.2 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 24 shows DC parameters for GPIO pads. The parameters in Table 24 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 24. Single Voltage GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15	–	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	–	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7*OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3*OVDD	V

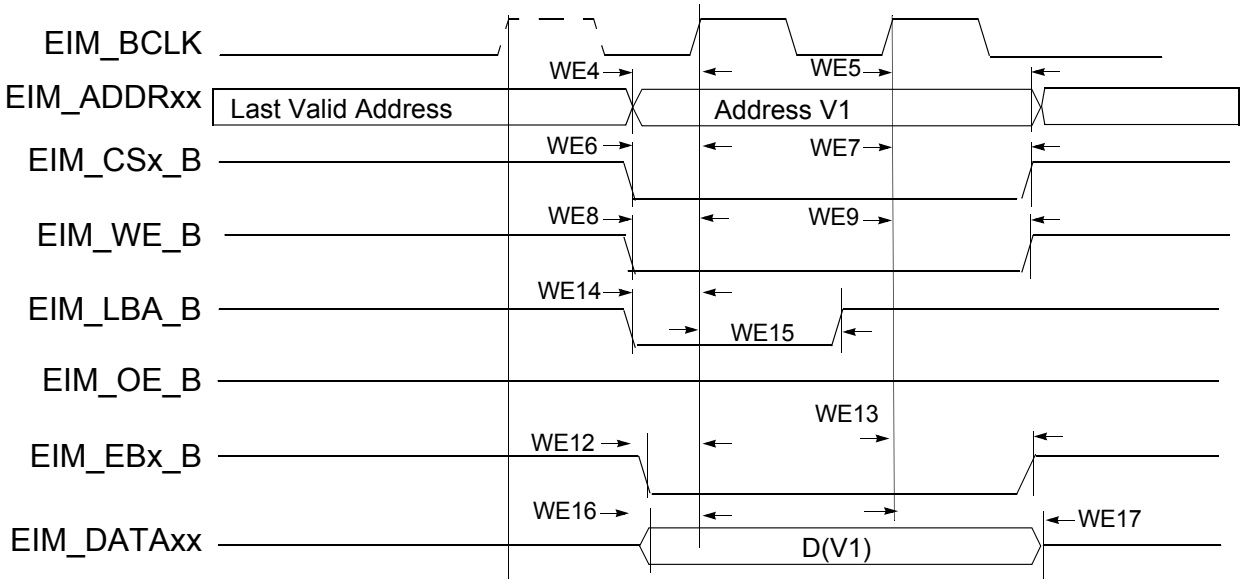

Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

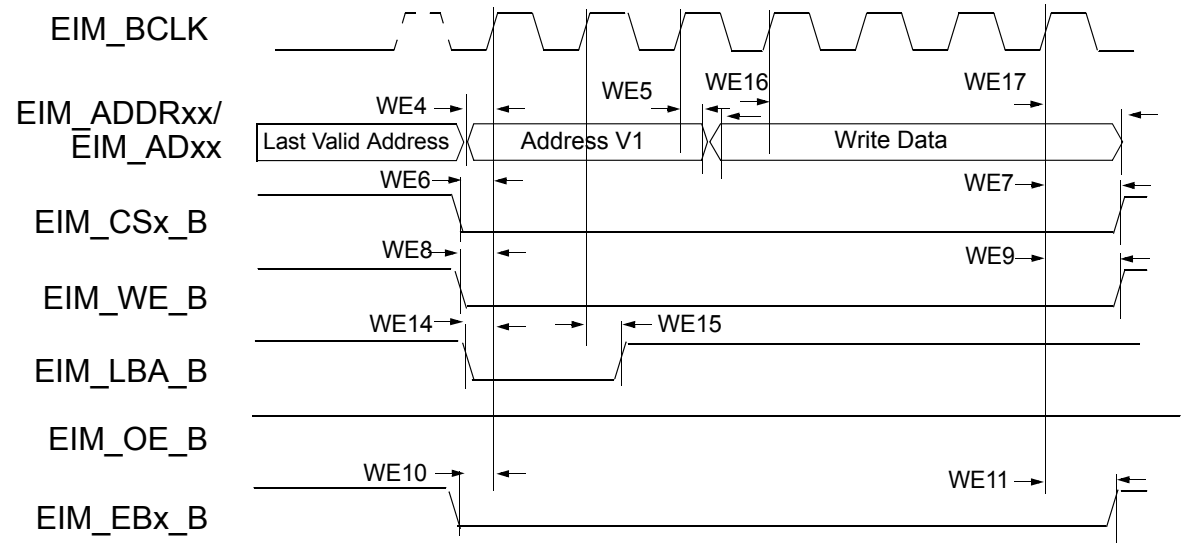

Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

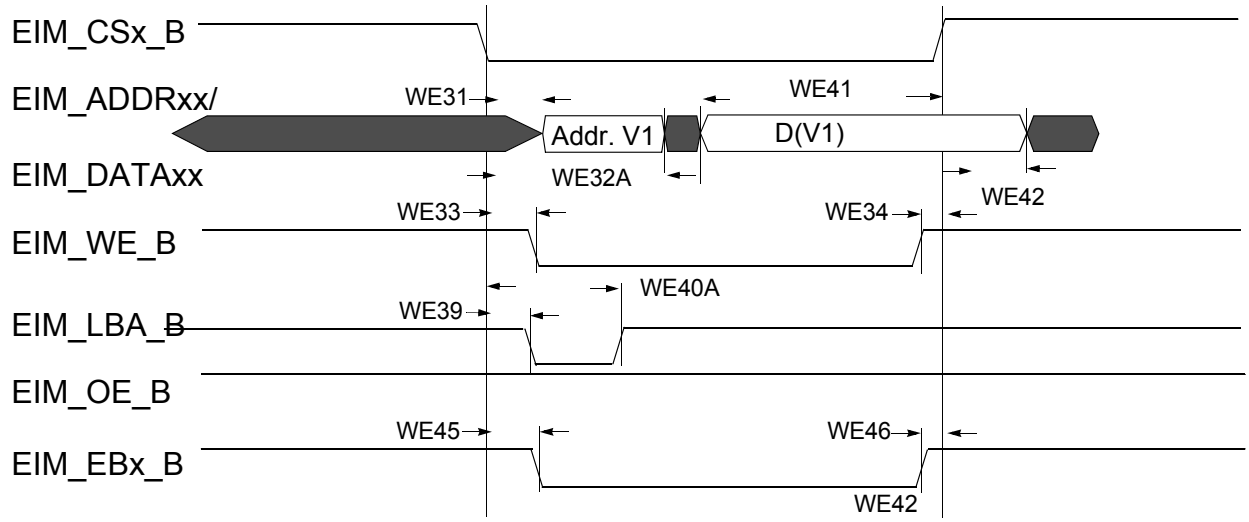

Figure 18. Asynchronous A/D Muxed Write Access

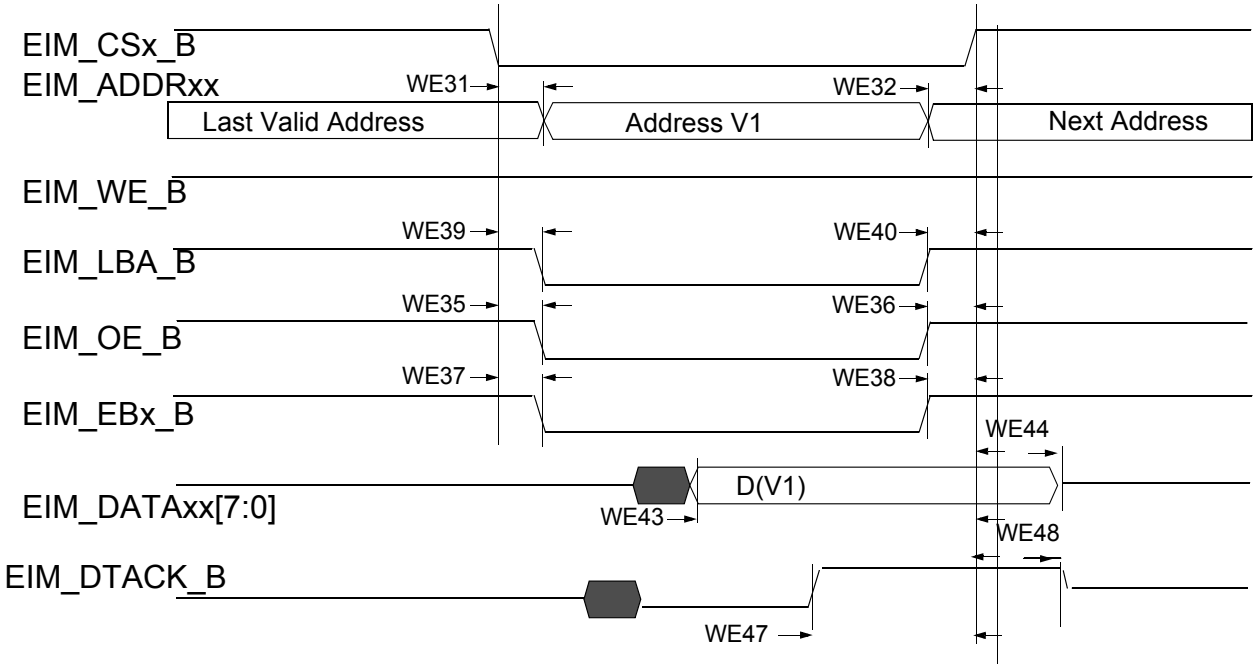

Figure 19. DTACK Mode Read Access (DAP=0)

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

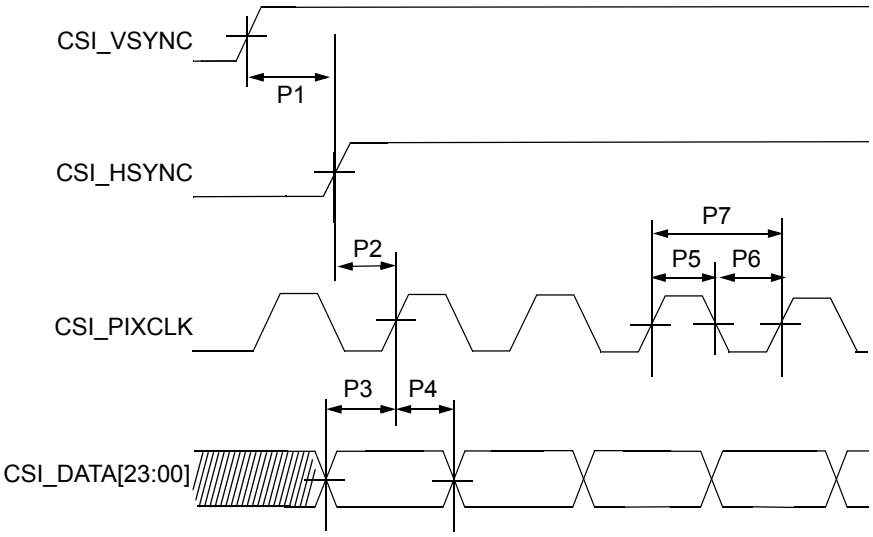

Figure 38. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

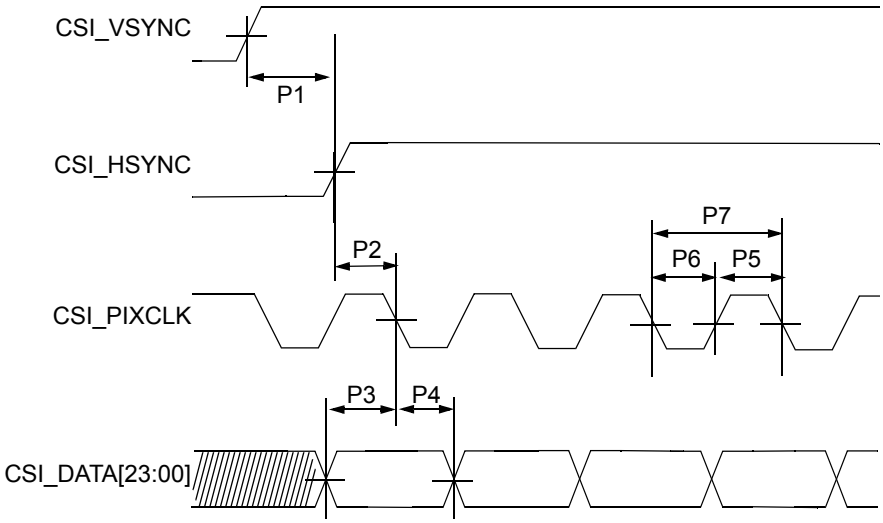

Figure 39. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 50. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

4.11.9.2 DDR Mode

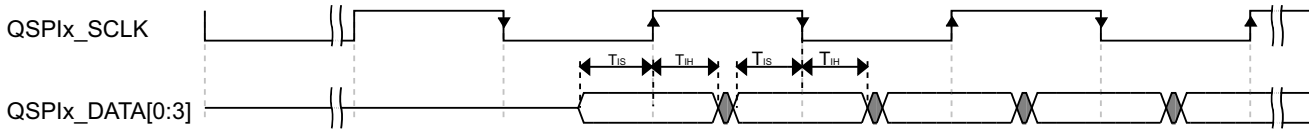

Figure 58. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 69. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

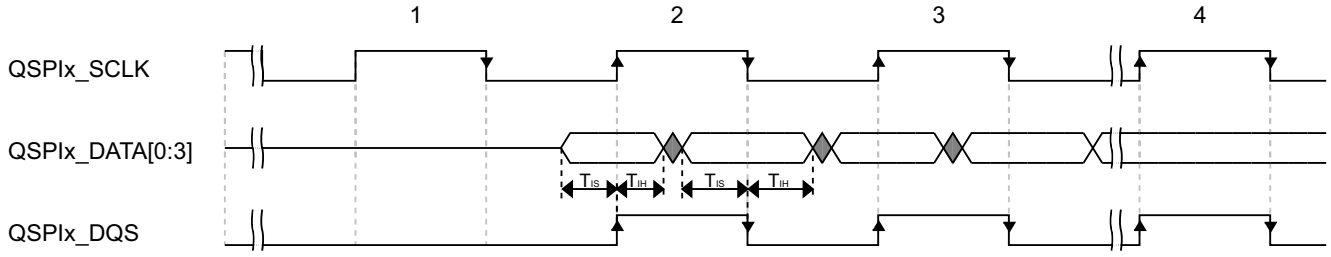

Figure 59. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 70. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

Table 72. Master Mode SAI Timing (continued)

Num	Characteristic	Min	Max	Unit
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

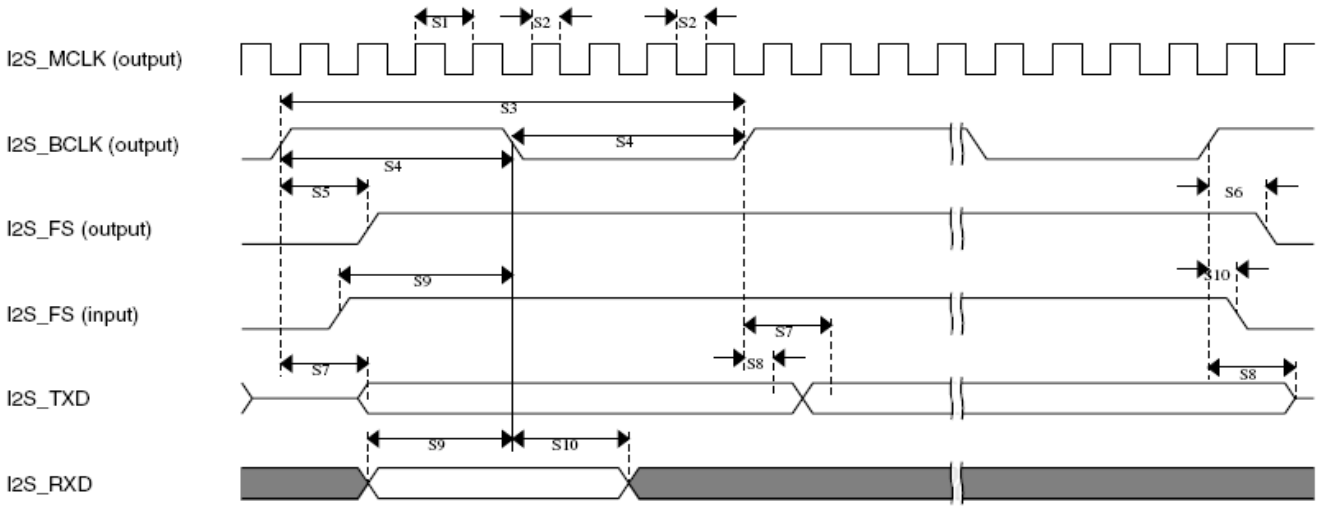

Figure 61. SAI Timing — Master Modes

Table 73. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 72 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

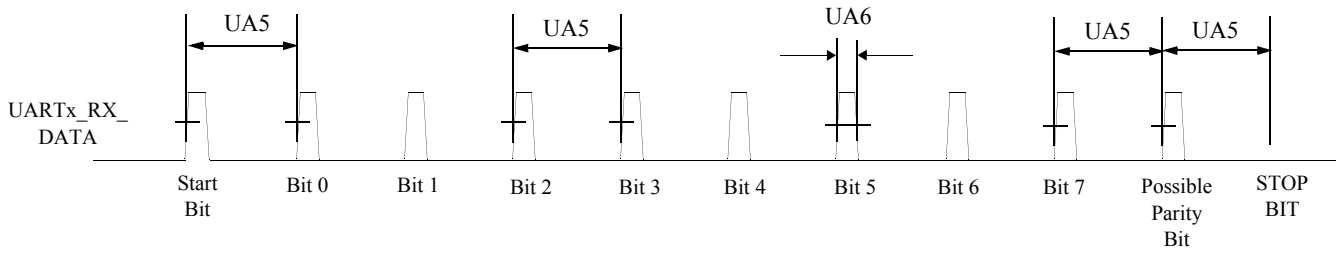

Figure 72. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.14 USB PHY Parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 82 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6UltraLite Fuse Map document and the System Boot chapter in *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

Table 82. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 82. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot Device Interface Allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 83. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

Table 90. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)
NAND_RE_B	usdhc2.CLK	Alt 1	Yes			
NAND_WE_B	usdhc2.CMD	Alt 1	Yes			
NAND_DATA00	usdhc2.DATA0	Alt 1	Yes			
NAND_DATA01	usdhc2.DATA1	Alt 1		Yes	Yes	
NAND_DATA02	usdhc2.DATA2	Alt 1		Yes	Yes	
NAND_DATA03	usdhc2.DATA3	Alt 1	Yes			
NAND_DATA04	usdhc2.DATA4	Alt 1			Yes	
NAND_DATA05	usdhc2.DATA5	Alt 1			Yes	
NAND_DATA06	usdhc2.DATA6	Alt 1			Yes	
NAND_DATA07	usdhc2.DATA7	Alt 1			Yes	
NAND_ALE	usdhc2.RESET_B	Alt 5				Yes
GPIO1_IO08	usdhc2.VSELECT	Alt 4				Yes

Table 91. NOR/OneNAND Boot through EIM

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
CSI_DATA00	weim.AD[0]	Alt 4	Yes		
CSI_DATA01	weim.AD[1]	Alt 4	Yes		
CSI_DATA02	weim.AD[2]	Alt 4	Yes		
CSI_DATA03	weim.AD[3]	Alt 4	Yes		
CSI_DATA04	weim.AD[4]	Alt 4	Yes		
CSI_DATA05	weim.AD[5]	Alt 4	Yes		
CSI_DATA06	weim.AD[6]	Alt 4	Yes		
CSI_DATA07	weim.AD[7]	Alt 4	Yes		
NAND_DATA00	weim.AD[8]	Alt 4	Yes		
NAND_DATA01	weim.AD[9]	Alt 4	Yes		
NAND_DATA02	weim.AD[10]	Alt 4	Yes		
NAND_DATA03	weim.AD[11]	Alt 4	Yes		
NAND_DATA04	weim.AD[12]	Alt 4	Yes		
NAND_DATA05	weim.AD[13]	Alt 4	Yes		
NAND_DATA06	weim.AD[14]	Alt 4	Yes		
NAND_DATA07	weim.AD[15]	Alt 4	Yes		
NAND_CLE	weim.ADDR[16]	Alt 4		Yes	Yes

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm Package Information

6.1.1 14x14 mm, 0.8 mm Pitch, Ball Matrix

Figure 74 shows the top, bottom, and side views of the 14x14 mm BGA package.

Table 95. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

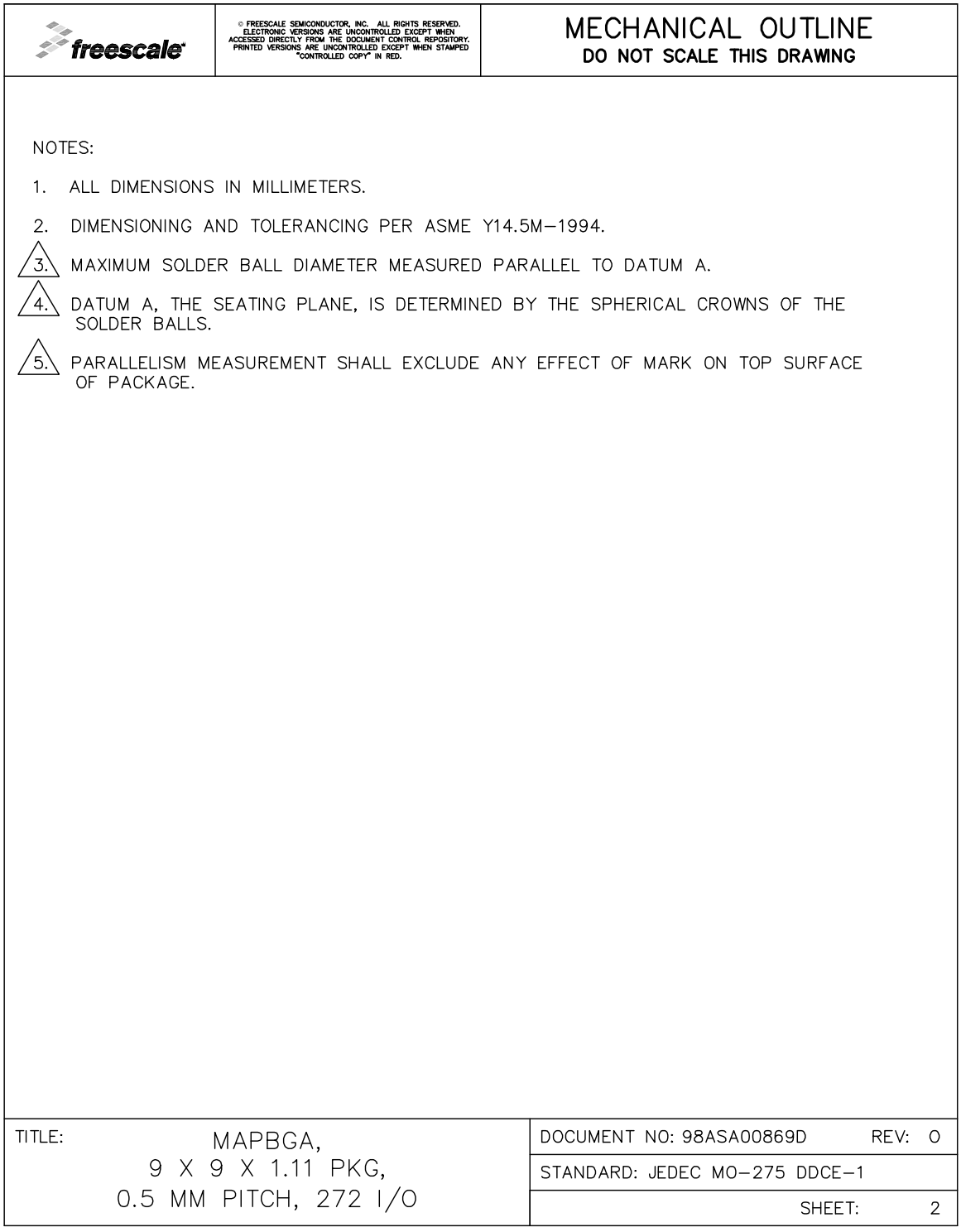

Figure 75. 9X9 mm BGA, Case x Package Top, Bottom, and Side Views

Table 98. 9x9 mm Functional Contact Assignments (continued)

DRAM_DATA09	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P4	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	N2	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	N1	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	P2	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	U4	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	R1	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	K2	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	E1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	L4	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	F2	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	H3	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	F5	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	G3	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	L2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	K1	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	K4	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	K3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	R5	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 98. 9x9 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P5	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	N4	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDQS1_P	N3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDWE_B	F4	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	T2	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	G17	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA0	Input	Keeper
ENET1_RX_DATA1	F16	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA1	Input	Keeper
ENET1_RX_EN	G16	NVCC_ENET	GPIO	ALT5	ENET1_RX_EN	Input	Keeper
ENET1_RX_ER	G14	NVCC_ENET	GPIO	ALT5	ENET1_RX_ER	Input	Keeper
ENET1_TX_CLK	G15	NVCC_ENET	GPIO	ALT5	ENET1_TX_CLK	Input	Keeper
ENET1_TX_DATA0	E16	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA0	Input	Keeper
ENET1_TX_DATA1	F13	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA1	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	ENET1_TX_EN	Input	Keeper
ENET2_RX_DATA0	E17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA0	Input	Keeper
ENET2_RX_DATA1	D17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA1	Input	Keeper
ENET2_RX_EN	D16	NVCC_ENET	GPIO	ALT5	ENET2_RX_EN	Input	Keeper
ENET2_RX_ER	H13	NVCC_ENET	GPIO	ALT5	ENET2_RX_ER	Input	Keeper
ENET2_TX_CLK	H14	NVCC_ENET	GPIO	ALT5	ENET2_TX_CLK	Input	Keeper
ENET2_TX_DATA0	E14	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA0	Input	Keeper
ENET2_TX_DATA1	F14	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA1	Input	Keeper
ENET2_TX_EN	E15	NVCC_ENET	GPIO	ALT5	ENET2_TX_EN	Input	Keeper
GPIO1_IO00	M14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	N16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	P15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	N15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	N14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	P14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	P16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper