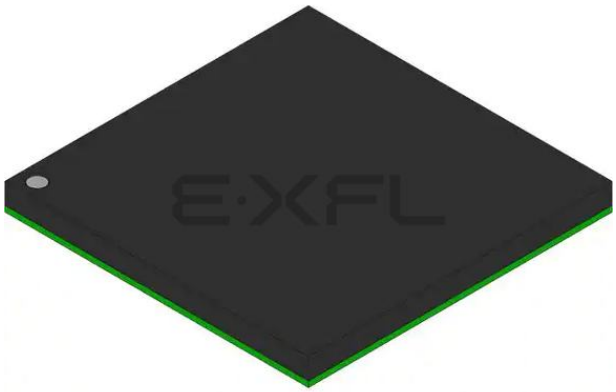

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g3dvm05aa

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.

See the i.MX 6UltraLite Power Consumption Measurement Application Note (AN5170) for more details on typical power consumption under various use case definitions.

Table 14. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_SOC_IN	528 MHz ARM clock based on Dhrystone test	500	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	500[2]	μA
USB_OTG1_VBUS USB_OTG2_VBUS	—	50[3]	mA
VDDA_ADC_3P3	100 Ohm maximum loading for touch panel	35	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(See[4])	—
NVCC_DRAM_2P5	—	50	mA
NVCC_GPIO	N=16	Use maximum IO Equation[5]	—
NVCC_UART	N=16	Use maximum IO equation[5]	—
NVCC_ENET	N=16	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_NAND	N=17	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_CSI	N=12	Use maximum IO equation[5]	—
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the *i.MX 6UltraLite Power Consumption Measurement Application Note* (AN5170) or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 15 shows the current core consumption (not including I/O) of i.MX 6UltraLite processors in selected low power modes.

Table 15. Low Power Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE: LDO Enabled	• LDO_ARM and LDO_SOC are set to 1.15 V • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLS are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.275 V)	7.7	mA
		VDD_HIGH_IN (3.0 V)	10.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	41.5	mW
SYSTEM IDLE: LDO Bypassed	• LDO_ARM and LDO_SOC are set to bypass mode • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.15 V)	7.5	mA
		VDD_HIGH_IN (3.0 V)	9.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	37.3	mW
LOW POWER IDLE: LDO Enabled	• LDO_SOC is set to 1.15 V, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.275 V)	3.2	mA
		VDD_HIGH_IN (3.0 V)	1.5	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	8.7	mW
LOW POWER IDLE: LDO Bypassed	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO-2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.15 V)	2.8	mA
		VDD_HIGH_IN (3.0 V)	0.4	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	4.57	mW
SUSPEND (DSM)	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are shut off • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • High-speed peripheral are powered off	VDD_SOC_IN (0.9 V)	0.44	mA
		VDD_HIGH_IN (3.0 V)	0.03	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	0.58	mW

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS, USB_OTG2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

NOTE

VDD_HIGH_IN should be turned off after VDD_SOC_IN is switched off.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

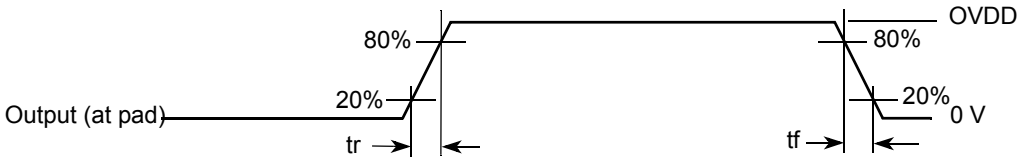

Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode
	8 Bit				16 Bit		16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	Reserved	Reserved	EIM_DATA [07:00]	Reserved	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	Reserved	Reserved	EIM_DATA [15:08]	Reserved	EIM_AD [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

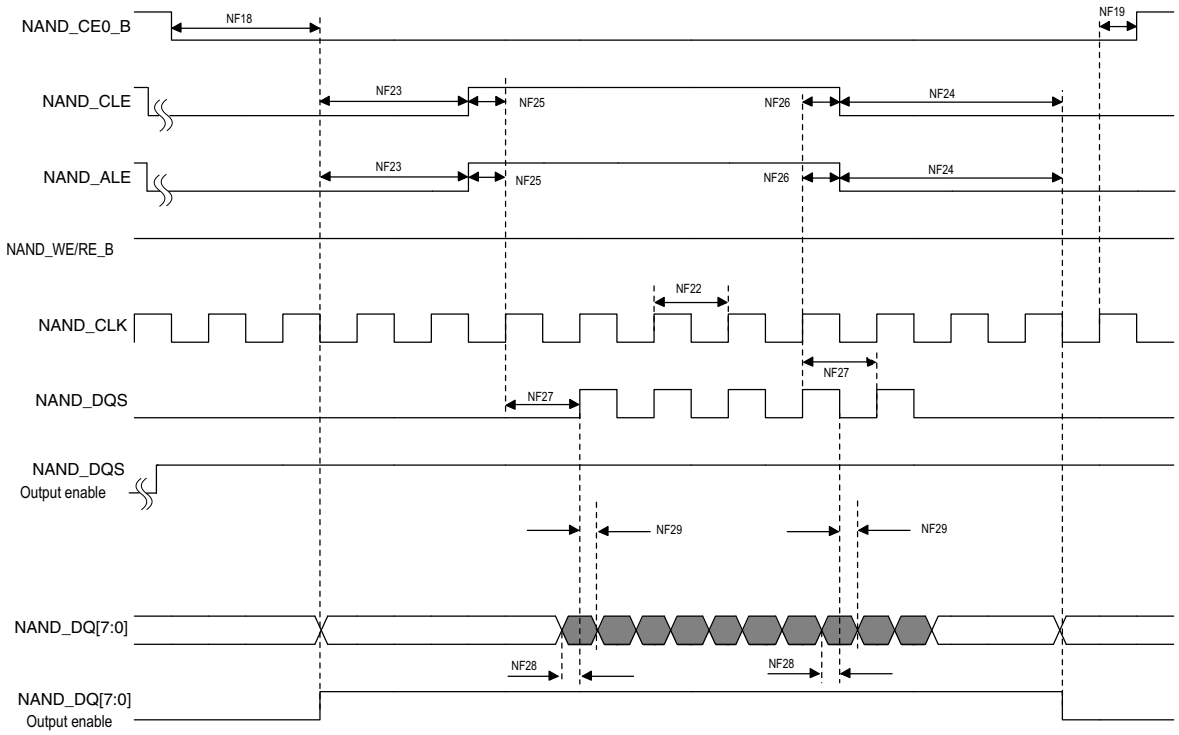

Figure 33. Source Synchronous Mode Data Write Timing Diagram

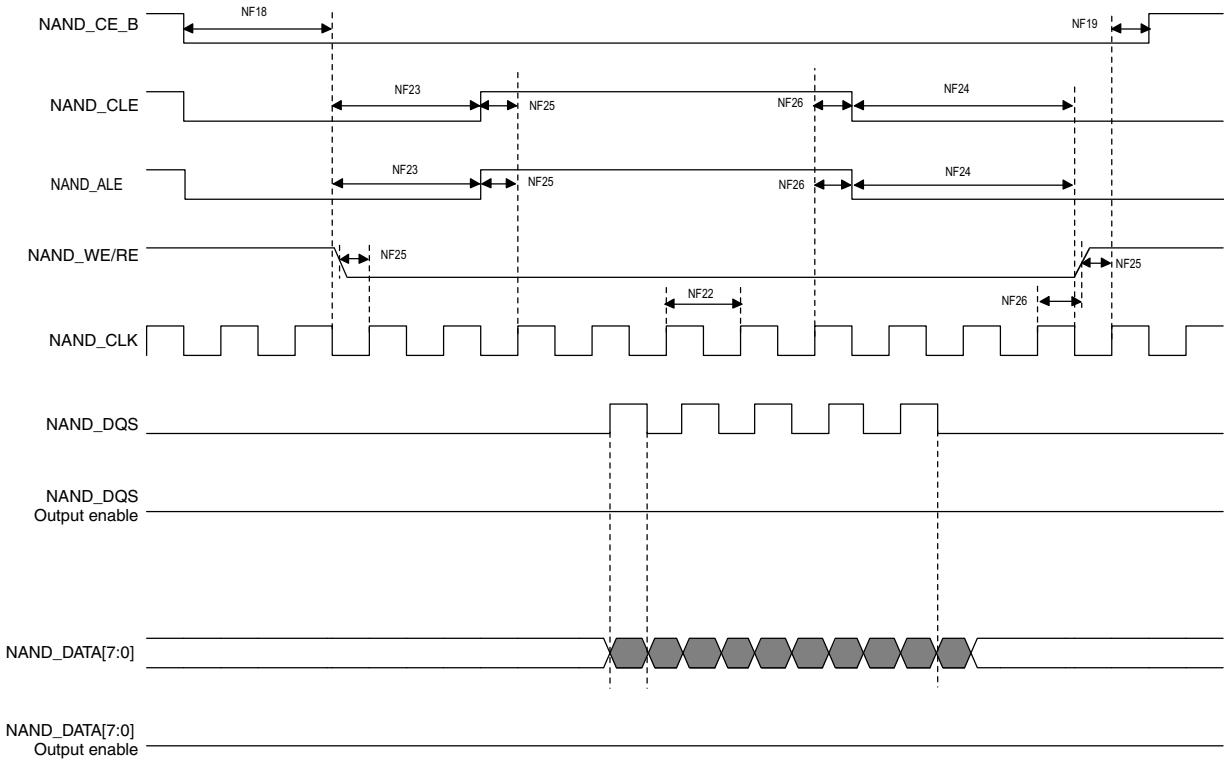

Figure 34. Source Synchronous Mode Data Read Timing Diagram

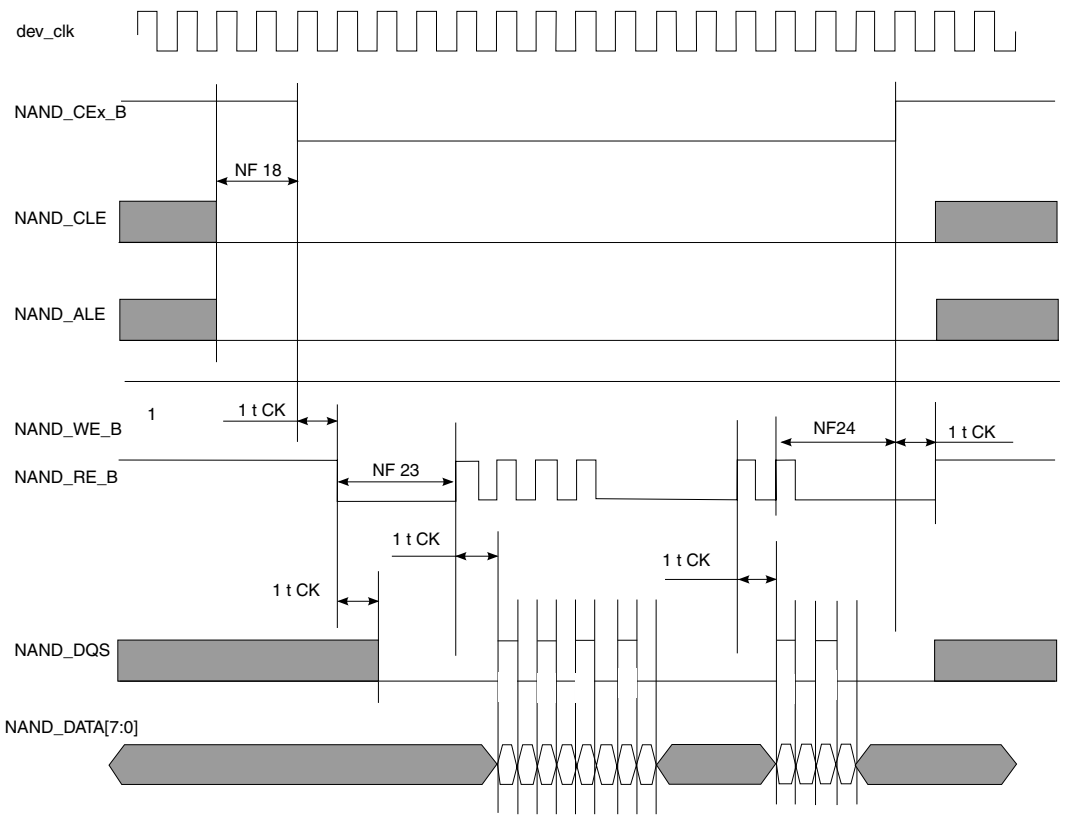

Figure 37. Samsung Toggle Mode Data Read Timing

Table 49. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see [3,2]]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see [2]]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see [2]]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see [2]]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see [2]]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see [4,2]]	—	ns
NF22	Clock period	tCK	—	—	ns
NF23	Preamble delay	tPRE	PRE_DELAY × T [see [5,2]]	—	ns
NF24	Postamble delay	tPOST	POST_DELAY × T +0.43 [see [2]]	—	ns

Table 50. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	133	MHz

4.11.1.0.2 Ungated Clock Mode Timing

Figure 40 shows the ungated clock mode timings of CSI, and Table 51 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

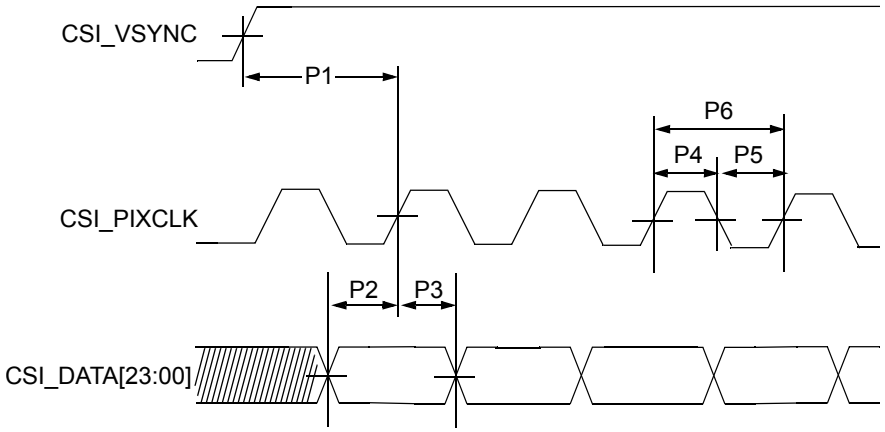

Figure 40. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 51. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	133	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 41 depicts the timing of ECSPI in master mode. Table 52 lists the ECSPI master mode timing characteristics.

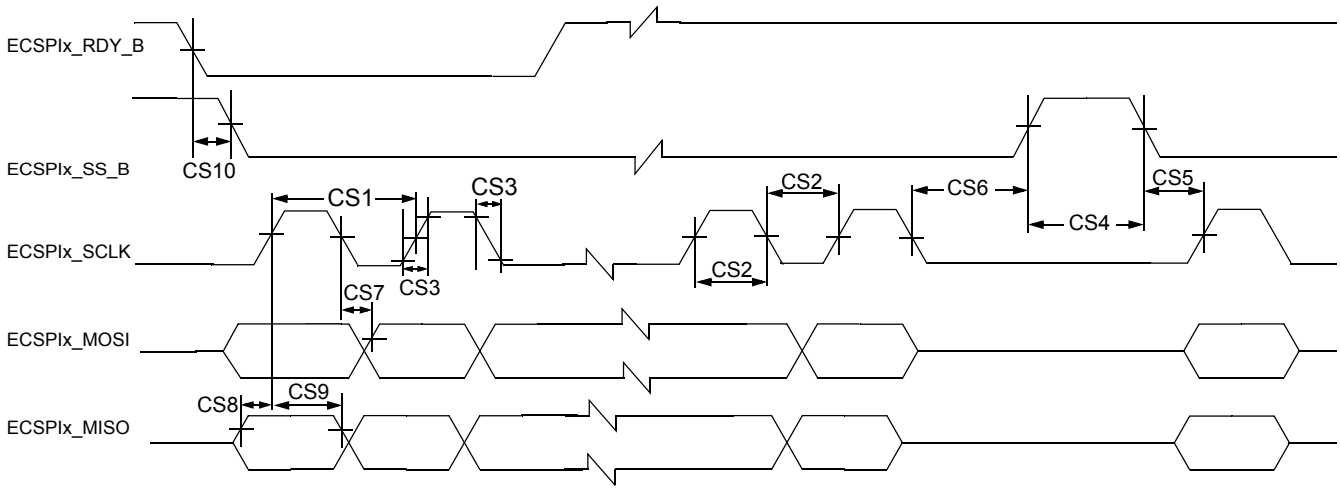

Figure 41. ECSPI Master Mode Timing Diagram

Table 52. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

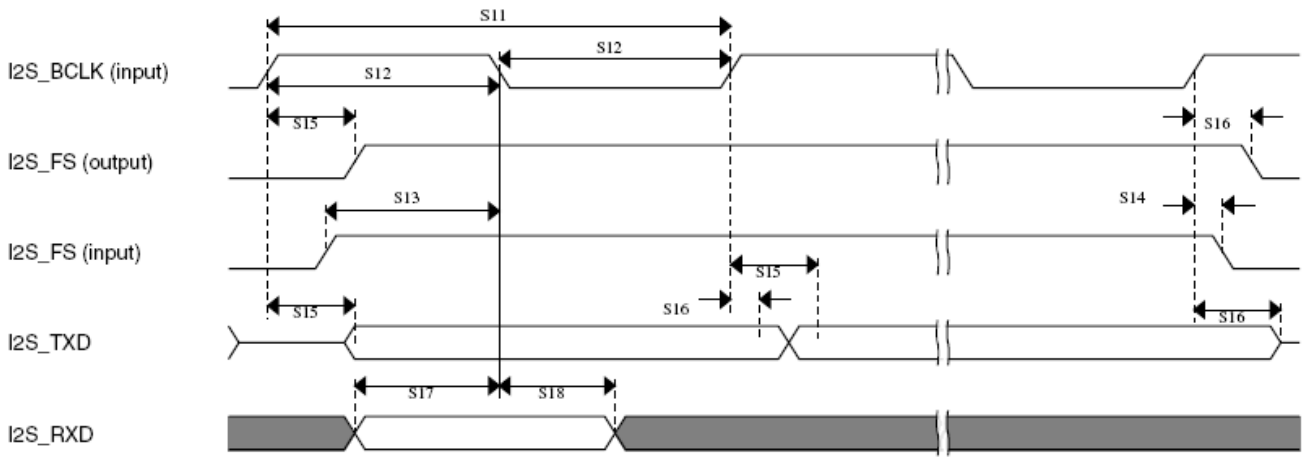

Figure 62. SAI Timing — Slave Modes

4.11.11 SCAN JTAG Controller (SJC) Timing Parameters

Figure 63 depicts the SJC test clock input timing. Figure 64 depicts the SJC boundary scan timing. Figure 65 depicts the SJC test access port. Signal parameters are listed in Table 74.

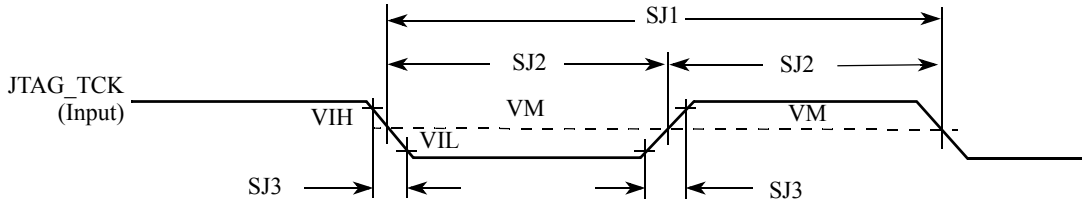

Figure 63. Test Clock Input Timing Diagram

Table 74. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.11.12 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 75 and Figure 67 and Figure 68 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 75. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

Table 81. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = (V_{REFH} - V_{REFL})/2 N	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		
[P:][C:] Integral Non-Linearity	12 bit mode	INL	—	2.6	—	LSB	—
	10bit mode		—	0.8	—		
	8 bit mode		—	0.3	—		
Zero-Scale Error	12 bit mode	E_{ZS}	—	-0.3	—	LSB	—
	10bit mode		—	-0.15	—		
	8 bit mode		—	-0.15	—		
Full-Scale Error	12 bit mode	E_{FS}	—	-2.5	—	LSB	—
	10bit mode		—	-0.6	—		
	8 bit mode		—	-0.3	—		
[L:] Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	—	Bits	—
[L:] Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	—

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

Table 91. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
NAND_ALE	weim.ADDR[17]	Alt 4		Yes	Yes
NAND_CE1_B	weim.ADDR[18]	Alt 4		Yes	Yes
SD1_CMD	weim.ADDR[19]	Alt 4		Yes	Yes
SD1_CLK	weim.ADDR[20]	Alt 4		Yes	Yes
SD1_DATA0	weim.ADDR[21]	Alt 4		Yes	Yes
SD1_DATA1	weim.ADDR[22]	Alt 4		Yes	Yes
SD1_DATA2	weim.ADDR[23]	Alt 4		Yes	Yes
SD1_DATA3	weim.ADDR[24]	Alt 4		Yes	Yes
ENET2_RXER	weim.ADDR[25]	Alt 4		Yes	Yes
ENET2_CRS_DV	weim.ADDR[26]	Alt 4		Yes	Yes
CSI_MCLK	weim.CS0_B	Alt 4	Yes		
LCD_DATA08	weim.DATA[0]	Alt 4		Yes	
LCD_DATA09	weim.DATA[1]	Alt 4		Yes	
LCD_DATA10	weim.DATA[2]	Alt 4		Yes	
LCD_DATA11	weim.DATA[3]	Alt 4		Yes	
LCD_DATA12	weim.DATA[4]	Alt 4		Yes	
LCD_DATA13	weim.DATA[5]	Alt 4		Yes	
LCD_DATA14	weim.DATA[6]	Alt 4		Yes	
LCD_DATA15	weim.DATA[7]	Alt 4		Yes	
LCD_DATA16	weim.DATA[8]	Alt 4		Yes	
LCD_DATA17	weim.DATA[9]	Alt 4		Yes	
LCD_DATA18	weim.DATA[10]	Alt 4		Yes	
LCD_DATA19	weim.DATA[11]	Alt 4		Yes	
LCD_DATA20	weim.DATA[12]	Alt 4		Yes	
LCD_DATA21	weim.DATA[13]	Alt 4		Yes	
LCD_DATA22	weim.DATA[14]	Alt 4		Yes	
LCD_DATA23	weim.DATA[15]	Alt 4		Yes	
NAND_RE_B	weim.EB_B[0]	Alt 4		Yes	Yes
NAND_WE_B	weim.EB_B[1]	Alt 4		Yes	Yes
CSI_HSYNC	weim.LBA_B	Alt 4	Yes		
CSI_PIXCLK	weim.OE	Alt 4	Yes		
CSI_VSYNC	weim.RW	Alt 4	Yes		

Table 95. 14x14 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	T2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDQS1_P	T1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDWE_B	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	N4	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	F16	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA0	Input	Keeper
ENET1_RX_DATA1	E17	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA1	Input	Keeper
ENET1_RX_EN	E16	NVCC_ENET	GPIO	ALT5	ENET1_RX_EN	Input	Keeper
ENET1_RX_ER	D15	NVCC_ENET	GPIO	ALT5	ENET1_RX_ER	Input	Keeper
ENET1_TX_CLK	F14	NVCC_ENET	GPIO	ALT5	ENET1_TX_CLK	Input	Keeper
ENET1_TX_DATA0	E15	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA0	Input	Keeper
ENET1_TX_DATA1	E14	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA1	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	ENET1_TX_EN	Input	Keeper
ENET2_RX_DATA0	C17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA0	Input	Keeper
ENET2_RX_DATA1	C16	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA1	Input	Keeper
ENET2_RX_EN	B17	NVCC_ENET	GPIO	ALT5	ENET2_RX_EN	Input	Keeper
ENET2_RX_ER	D16	NVCC_ENET	GPIO	ALT5	ENET2_RX_ER	Input	Keeper
ENET2_TX_CLK	D17	NVCC_ENET	GPIO	ALT5	ENET2_TX_CLK	Input	Keeper
ENET2_TX_DATA0	A15	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA0	Input	Keeper
ENET2_TX_DATA1	A16	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA1	Input	Keeper
ENET2_TX_EN	B15	NVCC_ENET	GPIO	ALT5	ENET2_TX_EN	Input	Keeper
GPIO1_IO00	K13	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	L15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	L14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	L17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	M17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	K17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	L16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper

Table 95. 14x14 mm Functional Contact Assignments (continued)

USB_OTG1_DN	T15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	U15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T12	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U12	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T16	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	T17	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0].

Table 96. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

N	M	L	K	J	H	G
DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1	DRAM_ADDR14
DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01	DRAM_ADDR06
VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13	VSS
DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07	DRAM_RESET
VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B	VSS
NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
TEST_MODE	VSS	VSS	VSS	VSS	VSS	VSS
SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP
VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS	VSS
VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART	UART5_RX_DATA
JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B	UART3_RTS_B
JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B	VSS
JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA	UART4_RX_DATA
GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA	UART4_TX_DATA
N	M	L	K	J	H	G

Table 98 shows an alpha-sorted list of functional contact assignments for the 9x9 mm package.

Table 98. 9x9 mm Functional Contact Assignments

Ball Name	9x9 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T8	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U8	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	U16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	T16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U7	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	—
CSI_DATA00	C3	NVCC_CSI	GPIO	ALT5	CSI_DATA00	Input	Keeper
CSI_DATA01	D4	NVCC_CSI	GPIO	ALT5	CSI_DATA01	Input	Keeper
CSI_DATA02	B2	NVCC_CSI	GPIO	ALT5	CSI_DATA02	Input	Keeper
CSI_DATA03	D1	NVCC_CSI	GPIO	ALT5	CSI_DATA03	Input	Keeper
CSI_DATA04	C4	NVCC_CSI	GPIO	ALT5	CSI_DATA04	Input	Keeper
CSI_DATA05	B3	NVCC_CSI	GPIO	ALT0	CSI_DATA05	Input	Keeper
CSI_DATA06	A3	NVCC_CSI	GPIO	ALT5	CSI_DATA06	Input	Keeper
CSI_DATA07	C2	NVCC_CSI	GPIO	ALT5	CSI_DATA07	Input	Keeper
CSI_HSYNC	D2	NVCC_CSI	GPIO	ALT5	CSI_HSYNC	Input	Keeper
CSI_MCLK	C1	NVCC_CSI	GPIO	ALT5	CSI_MCLK	Input	Keeper
CSI_PIXCLK	D5	NVCC_CSI	GPIO	ALT5	CSI_PIXCLK	Input	Keeper
CSI_VSYNC	D3	NVCC_CSI	GPIO	ALT5	CSI_VSYNC	Input	Keeper
DRAM_ADDR00	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	H1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	J2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	E4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 98. 9x9 mm Functional Contact Assignments (continued)

SNVS_TAMPER0	R8	VDD_SNVS_IN	GPIO	—	GPIO5_IO00/SNVS_TAMPER0[1]	Input	Keeper[1,2]
SNVS_TAMPER1	P6	VDD_SNVS_IN	GPIO	—	GPIO5_IO01/SNVS_TAMPER1[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER2	N10	VDD_SNVS_IN	GPIO	—	GPIO5_IO02/SNVS_TAMPER2[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER3	P10	VDD_SNVS_IN	GPIO	—	GPIO5_IO03/SNVS_TAMPER3[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER4	P7	VDD_SNVS_IN	GPIO	—	GPIO5_IO04/SNVS_TAMPER4[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER5	P8	VDD_SNVS_IN	GPIO	—	GPIO5_IO05/SNVS_TAMPER5[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER6	R7	VDD_SNVS_IN	GPIO	—	GPIO5_IO06/SNVS_TAMPER6[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER7	N9	VDD_SNVS_IN	GPIO	—	GPIO5_IO07/SNVS_TAMPER7[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER8	N8	VDD_SNVS_IN	GPIO	—	GPIO5_IO08/SNVS_TAMPER8[1]	Input	Keeper/Floating[1,2]
SNVS_TAMPER9	P9	VDD_SNVS_IN	GPIO	—	GPIO5_IO09/SNVS_TAMPER9[1]	Input	Keeper/Floating[1,2]
TEST_MODE	N7	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	Keeper
UART1_CTS_B	L14	NVCC_UART	GPIO	ALT5	UART1_CTS_B	Input	Keeper
UART1_RTS_B	K14	NVCC_UART	GPIO	ALT5	UART1_RTS_B	Input	Keeper
UART1_RX_DATA	L17	NVCC_UART	GPIO	ALT5	UART1_RX_DATA	Input	Keeper
UART1_TX_DATA	L15	NVCC_UART	GPIO	ALT5	UART1_TX_DATA	Input	Keeper
UART2_CTS_B	J17	NVCC_UART	GPIO	ALT5	UART2_CTS_B	Input	Keeper
UART2_RTS_B	J14	NVCC_UART	GPIO	ALT5	UART2_RTS_B	Input	Keeper
UART2_RX_DATA	K16	NVCC_UART	GPIO	ALT5	UART2_RX_DATA	Input	Keeper
UART2_TX_DATA	L16	NVCC_UART	GPIO	ALT5	UART2_TX_DATA	Input	Keeper
UART3_CTS_B	H16	NVCC_UART	GPIO	ALT5	UART3_CTS_B	Input	Keeper
UART3_RTS_B	H15	NVCC_UART	GPIO	ALT5	UART3_RTS_B	Input	Keeper
UART3_RX_DATA	K15	NVCC_UART	GPIO	ALT5	UART3_RX_DATA	Input	Keeper
UART3_TX_DATA	K17	NVCC_UART	GPIO	ALT5	UART3_TX_DATA	Input	Keeper
UART4_RX_DATA	H17	NVCC_UART	GPIO	ALT5	UART4_RX_DATA	Input	Keeper
UART4_TX_DATA	J16	NVCC_UART	GPIO	ALT5	UART4_TX_DATA	Input	Keeper
UART5_RX_DATA	J13	NVCC_UART	GPIO	ALT5	UART5_RX_DATA	Input	Keeper
UART5_TX_DATA	K13	NVCC_UART	GPIO	ALT5	UART5_TX_DATA	Input	Keeper
USB_OTG1_CHD_B	T15	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—

Table 99. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

P	N	M	L	K	J	H
DRAM_DATA08	DRAM_DATA14	VSS	DRAM_CS0_B	DRAM_SDCKE1	DRAM_ADDR09	DRAM_ADDR02
DRAM_DATA15	DRAM_DATA13	DRAM_ADDR10	DRAM_SDCKE0	DRAM_ODT0	DRAM_ADDR03	DRAM_ADDR05
DRAM_DATA10	DRAM_SDQS1_P	VSS	DRAM_ADDR12	DRAM_SDCLK0_P	VSS	DRAM_SDBA0
DRAM_DATA12	DRAM_SDQS1_N	DRAM_ADDR04	DRAM_RAS_B	DRAM_SDCLK0_N	DRAM_ADDR07	DRAM_ADDR13
DRAM_SDQS0_P	DRAM_DATA01	NVCC_DRAM	NVCC_DRAM	DRAM_ADDR11	DRAM_ADDR08	DRAM_CSI_B
SNVS_TAMPER1	NVCC_DRAM			NVCC_DRAM_2P5		VSS
SNVS_TAMPER4	TEST_MODE		VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER5	SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER9	SNVS_TAMPER7		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER3	SNVS_DAMPER2	NGND_KEL0	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
USB_OTG1_DP	VDD_USB_CAP		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
VDD_SNVS_IN	VDD_SNVS_CAP			VSS		VSS
JTAG_TRST_B	ADC_VREFH	NVCC_GPIO	NVCC_UART	UART5_TX_DATA	UART5_RX_DATA	ENET2_RX_ER
GPIO1_IO08	GPIO1_IO07	GPIO1_IO00	UART1_CTS_B	UART1_RTS_B	UART2_RTS_B	ENET2_TX_CLK
GPIO1_IO05	GPIO1_IO06	GPIO_IO01	UART1_TX_DATA	UART3_RX_DATA	VSS	UART3_RTS_B
GPIO1_IO09	GPIO1_IO03	GPIO1_IO02	UART2_TX-DATA	UART2_RX_DATA	UART4_TX_DATA	UART3_CTS_B
JTAG_TDI	GPIO1_IO04	VSS	UART1_RX_DATA	UART3_TX_DATA	UART2_CTS_B	UART4_RX_DATA
P	N	M	L	K	J	H