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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l083czt6

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode. The LCD is not stopped automatically by entering Stop mode.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.8 Memories

The STM32L083xx devices have the following features:

- 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 64, 128 or 192 Kbytes of embedded Flash program memory
  - 6 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus Kbytes of system memory

Flash program and data EEPROM are divided into two banks. This allows writing in one bank while running code or reading data from the other bank.

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USB (PA11, PA12), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.16 Touch sensing controller (TSC)

The STM32L083xx provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (such as glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 9. Capacitive sensing GPIOs available on STM32L083xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PC0
	TSC_G3_IO2	PB0		TSC_G7_IO2	PC1
	TSC_G3_IO3	PB1		TSC_G7_IO3	PC2
	TSC_G3_IO4	PB2		TSC_G7_IO4	PC3
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PC6
	TSC_G4_IO2	PA10		TSC_G8_IO2	PC7
	TSC_G4_IO3	PA11		TSC_G8_IO3	PC8
	TSC_G4_IO4	PA12		TSC_G8_IO4	PC9

3.17 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.18 Timers and watchdogs

The ultra-low-power STM32L083xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 10 compares the features of the general-purpose and basic timers.

Table 10. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.18.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L083xx device (see *Table 10* for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

3.19.5 Universal serial bus (USB)

The STM32L083xx embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.20 Clock recovery system (CRS)

The STM32L083xx embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.21 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 18. Alternate functions port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I 2C1/LCD/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/L PTIM1/TIM2/3/E VENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port B	PB0	EVENTOUT	LCD_SEG5	TIM3_CH3	TSC_G3_IO2	-	-	-	-
	PB1	-	LCD_SEG6	TIM3_CH4	TSC_G3_IO3	LPUART1_RTS_DE	-	-	-
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-	I2C3_SMBA
	PB3	SPI1_SCK	LCD_SEG7	TIM2_CH2	TSC_G5_IO1	EVENTOUT	USART1_RTS_DE	USART5_TX	-
	PB4	SPI1_MISO	LCD_SEG8	TIM3_CH1	TSC_G5_IO2	TIM22_CH1	USART1_CTS	USART5_RX	I2C3_SDA
	PB5	SPI1_MOSI	LCD_SEG9	LPTIM1_IN1	I2C1_SMBA	TIM3_CH2/ TIM22_CH2	USART1_CK	USART5_CK/ USART5_RTS_D E	-
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-	-
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	USART4_CTS	-
	PB8	-	LCD_SEG16	-	TSC_SYNC	I2C1_SCL	-	-	-
	PB9	-	LCD_COM3	EVENTOUT	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-
	PB10	-	LCD_SEG10	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL	LPUART1_RX
	PB11	EVENTOUT	LCD_SEG11	TIM2_CH4	TSC_G6_IO1	LPUART1_RX	-	I2C2_SDA	LPUART1_TX
	PB12	SPI2_NSS/I2S2_WS	LCD_SEG12	LPUART1_RTS_ DE	TSC_G6_IO2		I2C2_SMBA	EVENTOUT	-
	PB13	SPI2_SCK/I2S2_CK	LCD_SEG13	MCO	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1	-
	PB14	SPI2_MISO/ I2S2_MCK	LCD_SEG14	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_DE	I2C2_SDA	TIM21_CH2	-
	PB15	SPI2_MOSI/ I2S2_SD	LCD_SEG15	RTC_REFIN	-	-	-	-	-

Table 19. Alternate functions port C

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ LCD/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port C	PC0	LPTIM1_IN1	LCD_SEG18	EVENTOUT	TSC_G7_IO1			LPUART1_RX	I2C3_SCL
	PC1	LPTIM1_OUT	LCD_SEG19	EVENTOUT	TSC_G7_IO2			LPUART1_TX	I2C3_SDA
	PC2	LPTIM1_IN2	LCD_SEG20	SPI2_MISO/ I2S2_MCK	TSC_G7_IO3				
	PC3	LPTIM1_ETR	LCD_SEG21	SPI2_MOSI/ I2S2_SD	TSC_G7_IO4				
	PC4	EVENTOUT	LCD_SEG22	LPUART1_TX					
	PC5		LCD_SEG23	LPUART1_RX	TSC_G3_IO1				
	PC6	TIM22_CH1	LCD_SEG24	TIM3_CH1	TSC_G8_IO1				
	PC7	TIM22_CH2	LCD_SEG25	TIM3_CH2	TSC_G8_IO2				
	PC8	TIM22_ETR	LCD_SEG26	TIM3_CH3	TSC_G8_IO3				
	PC9	TIM21_ETR	LCD_SEG27	USB_OE/TIM3_CH4	TSC_G8_IO4				I2C3_SDA
	PC10	LPUART1_TX	LCD_COM4/LCD_SEG 28/LCD_SEG48					USART4_TX	
	PC11	LPUART1_RX	LCD_COM5/LCD_SEG 29/LCD_SEG49					USART4_RX	
	PC12		LCD_COM6/LCD_SEG 30/LCD_SEG50	USART5_TX				USART4_CK	
	PC13								
	PC14								
	PC15								

6.3 Operating conditions

6.3.1 General operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}	Analog operating voltage (DAC not used)	Must be the same voltage as V_{DD}(1)	1.65	3.6	V
V_{DDA}	Analog operating voltage (all features)	Must be the same voltage as V_{DD}(1)	1.8	3.6	V
V_{DD_USB}	Standard operating voltage, USB domain(2)	USB peripheral used	3.0	3.6	V
		USB peripheral not used	1.65	3.6	
V_{IN}	Input voltage on FT, FTf and RST pins(3)	2.0 V ≤ V_{DD} ≤ 3.6 V	-0.3	5.5	V
		1.65 V ≤ V_{DD} ≤ 2.0 V	-0.3	5.2	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on TC pin	-	-0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A = 85 °C (range 6) or T_A = 105 °C (range 7) (4)	UFBGA100 package	-	351	mW
		LQFP100 package	-	488	
		TFBGA64 package	-	313	
		LQFP64 package	-	435	
		LQFP48 package	-	370	
	Power dissipation at T_A = 125 °C (range 3) (4)	UFBGA100 package	-	88	
		LQFP100 package	-	122	
		TFBGA64 package	-	78	
		LQFP64 package	-	109	
		LQFP48 package		93	

Table 26. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Maximum power dissipation (range 3)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	
	Junction temperature range (range 3)	-40 °C ≤ T_A ≤ 125 °C	–40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. V_{DD_USB} must respect the following conditions:

- When V_{DD} is powered on (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
- When V_{DD} is powered down (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
- In operating mode, V_{DD_USB} could be lower or higher V_{DD}.
- If the USB is not used, V_{DD_USB} must range from V_{DD_min} to V_{DD_max} to be able to use PA11 and PA12 as standard I/Os.

3. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 90: Thermal characteristics on page 134*).

Table 27. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 29* are based on characterization results, unless otherwise specified.

Table 28. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 29. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 29. Embedded internal reference voltage(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 41: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 43: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 51*, *Table 26* and *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Low-speed external user clock generated from an external source

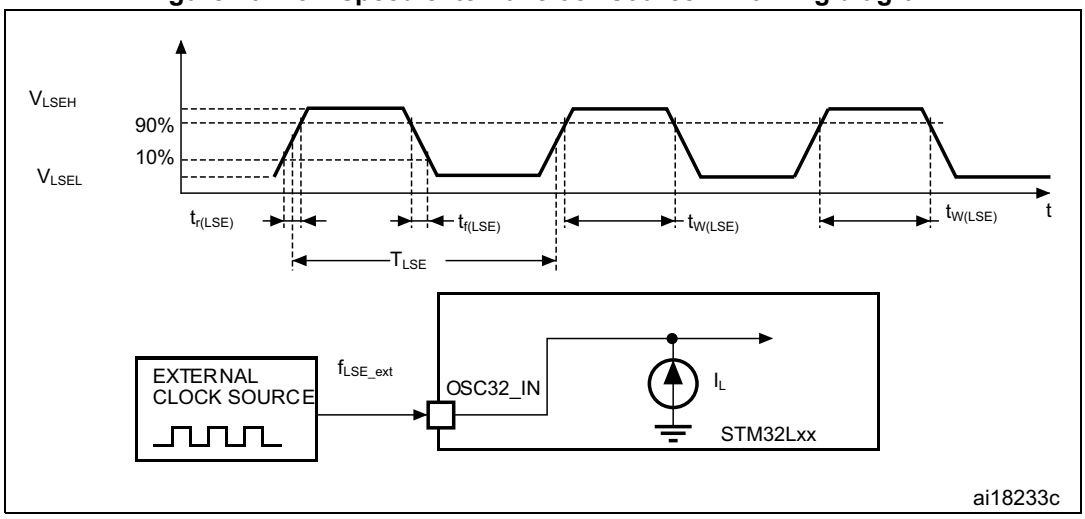
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 44. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram



6.3.18 Comparators

Table 70. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V, V_{IN+} = 0 V, V_{IN-} = V_{REFINT}, T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 71. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C, V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 79. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 80. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

Table 83. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

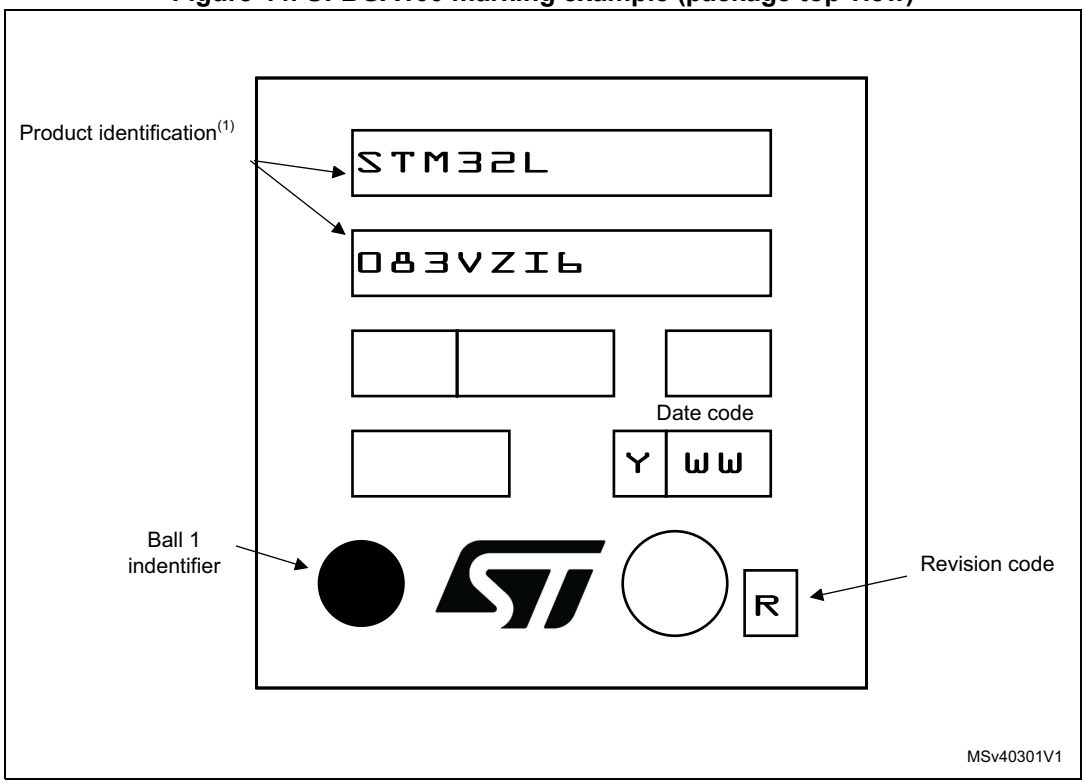
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for UFBGA100

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 44. UFBGA100 marking example (package top view)

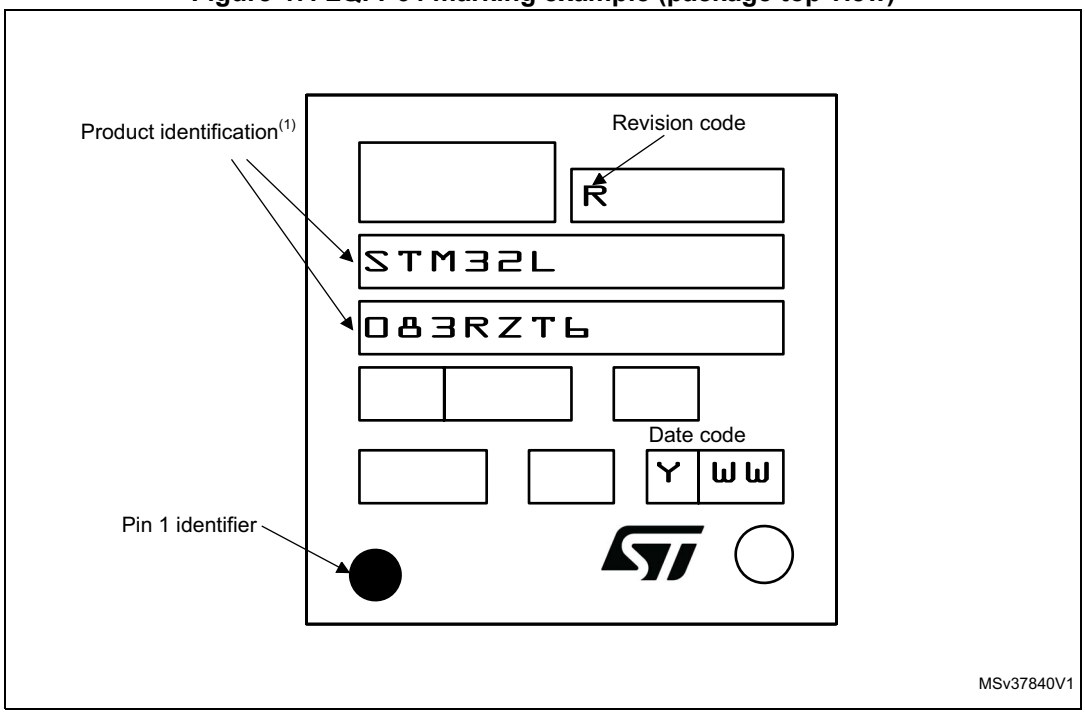


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 47. LQFP64 marking example (package top view)

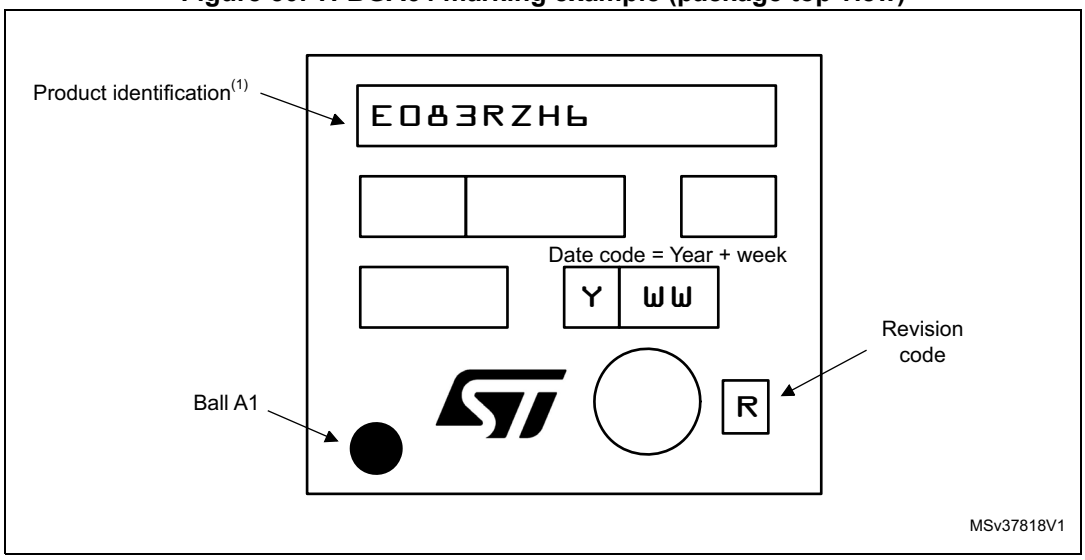


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 50. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 90. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 x 7 mm / 0.5 mm pitch	54	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	64	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm / 0.5 mm pitch	57	