What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l083vzt6

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V[1]	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance	Functional[2]
V_{DD} = 1.8 to 2.0 V[1]	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional[2]
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional[2]
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional[2]

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.17 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

The AES can be served by the DMA controller.

3.18 Timers and watchdogs

The ultra-low-power STM32L083xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 10 compares the features of the general-purpose and basic timers.

Table 10. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.18.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L083xx device (see *Table 10* for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

3.18.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.19 Communication interfaces

3.19.1 I^{2}C bus

Up to three I^{2}C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I^{2}C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 11. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

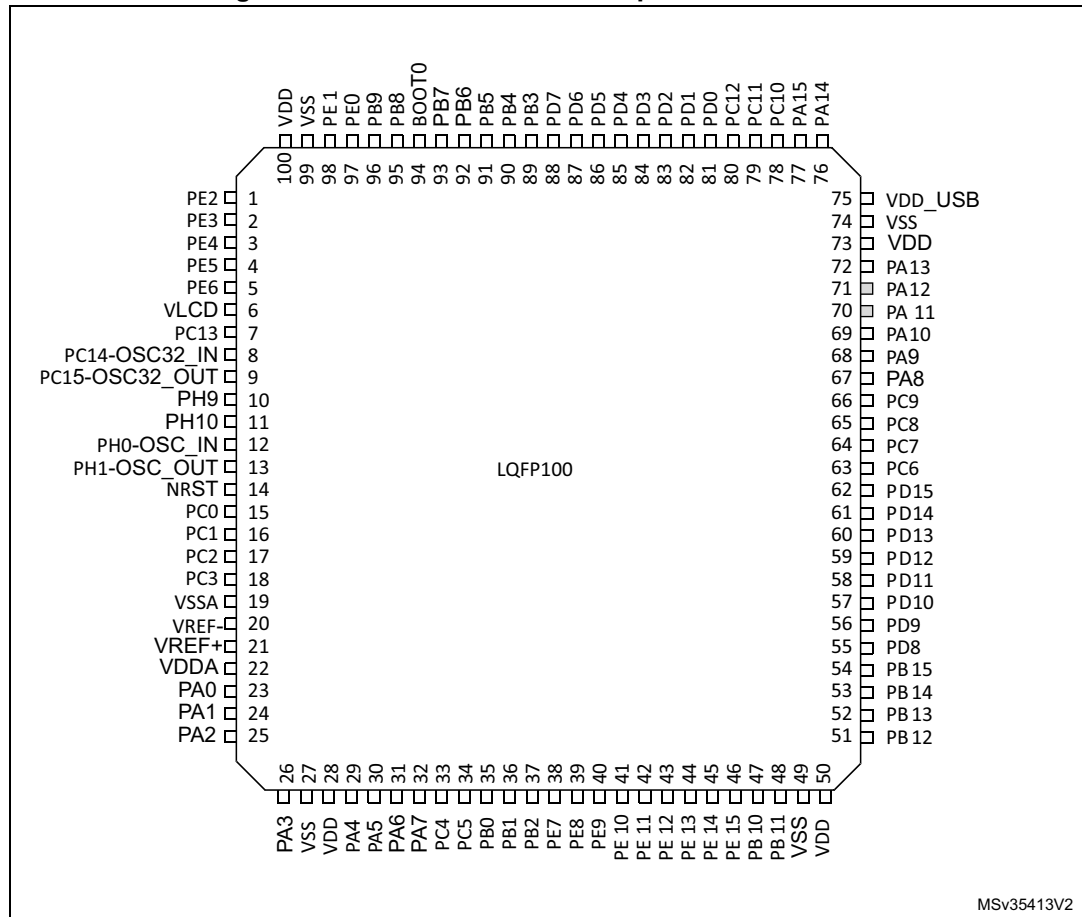Each I2C interface can be served by the DMA controller.

Refer to *Table 12* for an overview of I2C interface features.

Table 12. STM32L083xx I^{2}C implementation

I2C features[1]	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X

4 Pin descriptions

Figure 3. STM32L083xx LQFP100 pinout - 14 x 14 mm

1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 20. Alternate functions port D

Port		AF0 SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	AF1 SPI1/SPI2/I2S2/I2C1/ LCD/TIM2/21	AF2 SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	AF3 I2C1/TSC/ EVENTOUT	AF4 I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	AF5 SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	AF6 I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	AF7 I2C3/LPUART1/ COMP1/2/TIM3
Port D	PD0	TIM21_CH1	SPI2_NSS/I2S2_WS	-	-	-	-	-	-
	PD1	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-
	PD2	LPUART1_RTS_ DE	LCD_COM7/ LCD_SEG31/ LCD_SEG51	TIM3_ETR	-	-	-	USART5_RX	-
	PD3	USART2_CTS	LCD_SEG44	SPI2_MISO/ I2S2_MCK	-	-	-	-	-
	PD4	USART2_RTS_D E	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-
	PD5	USART2_TX	-	-	-	-	-	-	-
	PD6	USART2_RX	-	-	-	-	-	-	-
	PD7	USART2_CK	TIM21_CH2	-	-	-	-	-	-
	PD8	LPUART1_TX	LCD_SEG28	-	-	-	-	-	-
	PD9	LPUART1_RX	LCD_SEG29	-	-	-	-	-	-
	PD10	-	LCD_SEG30	-	-	-	-	-	-
	PD11	LPUART1_CTS	LCD_SEG31	-	-	-	-	-	-
	PD12	LPUART1_RTS_ DE	LCD_SEG32	-	-	-	-	-	-
	PD13	-	LCD_SEG33	-	-	-	-	-	-
	PD14	-	LCD_SEG34	-	-	-	-	-	-
	PD15	USB_CRS_SYNC	LCD_SEG35	-	-	-	-	-	-

Table 27. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 29* are based on characterization results, unless otherwise specified.

Table 28. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 29. Embedded internal reference voltage[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$[2]	Internal reference voltage	$-40\ °C < T_J < +125\ °C$	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value[3]	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}[4]	Temperature coefficient	$-40\ °C < T_J < +125\ °C$	-	25	100	ppm/°C
A_{Coeff}[4]	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$[4]	Voltage coefficient	$3.0\ V < V_{DDA} < 3.6\ V$	-	-	2000	ppm/V
$T_{S\_vrefint}$[4][5]	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}[4]	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}[4]	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}[4]	VREF_OUT output current[6]	-	-	-	1	µA
C_{VREF_OUT}[4]	VREF_OUT output load	-	-	-	50	pF

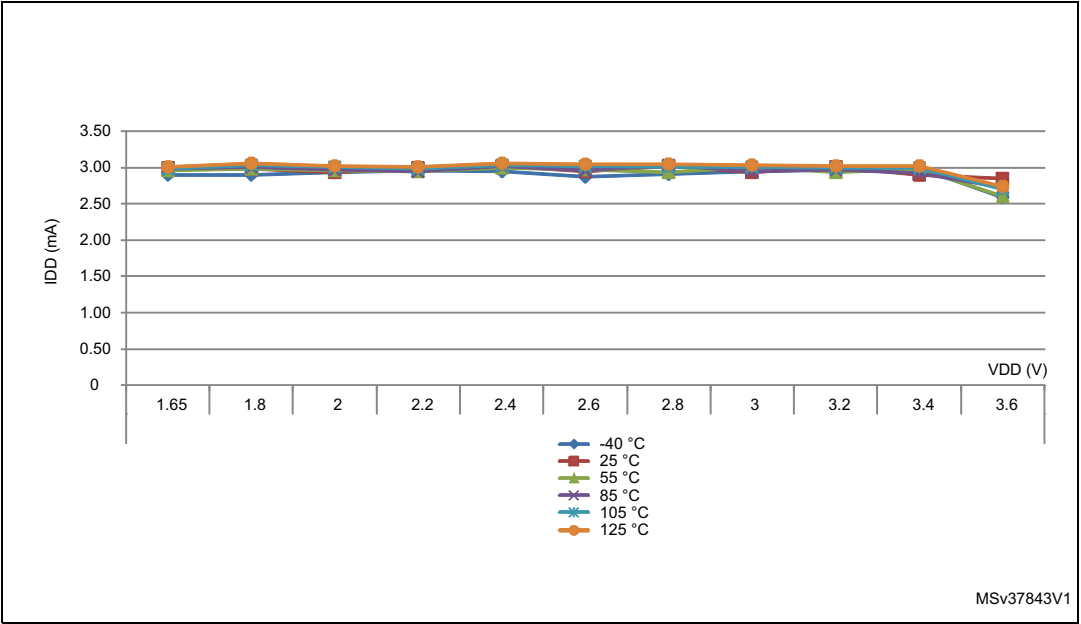**Figure 14. I$_{DD}$ vs V$_{DD}$, at T$_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS**

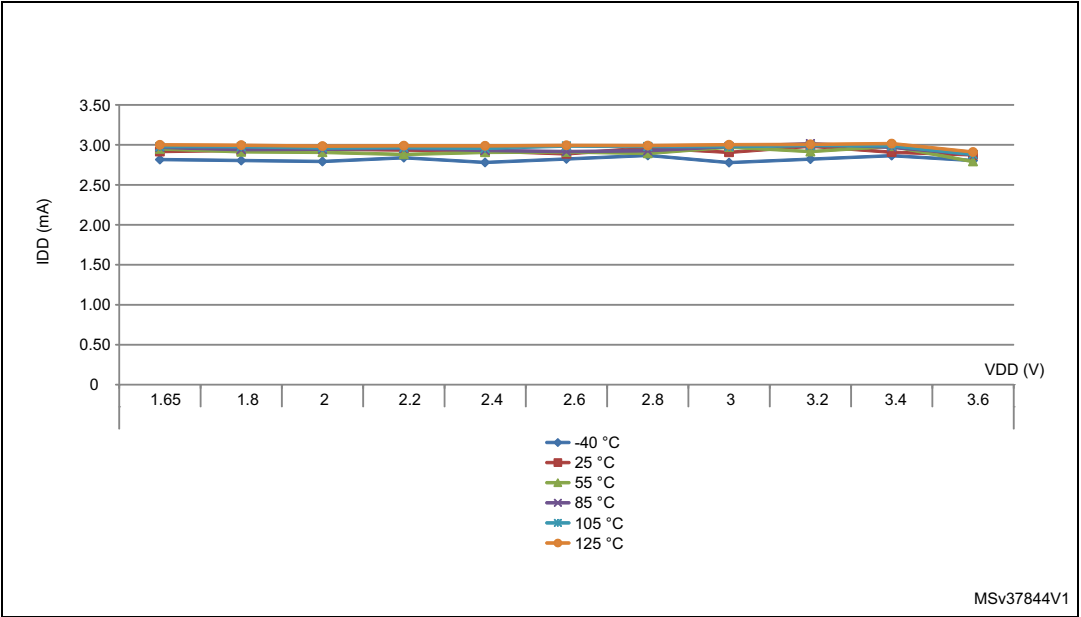**Figure 15. I$_{DD}$ vs V$_{DD}$, at T$_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS**

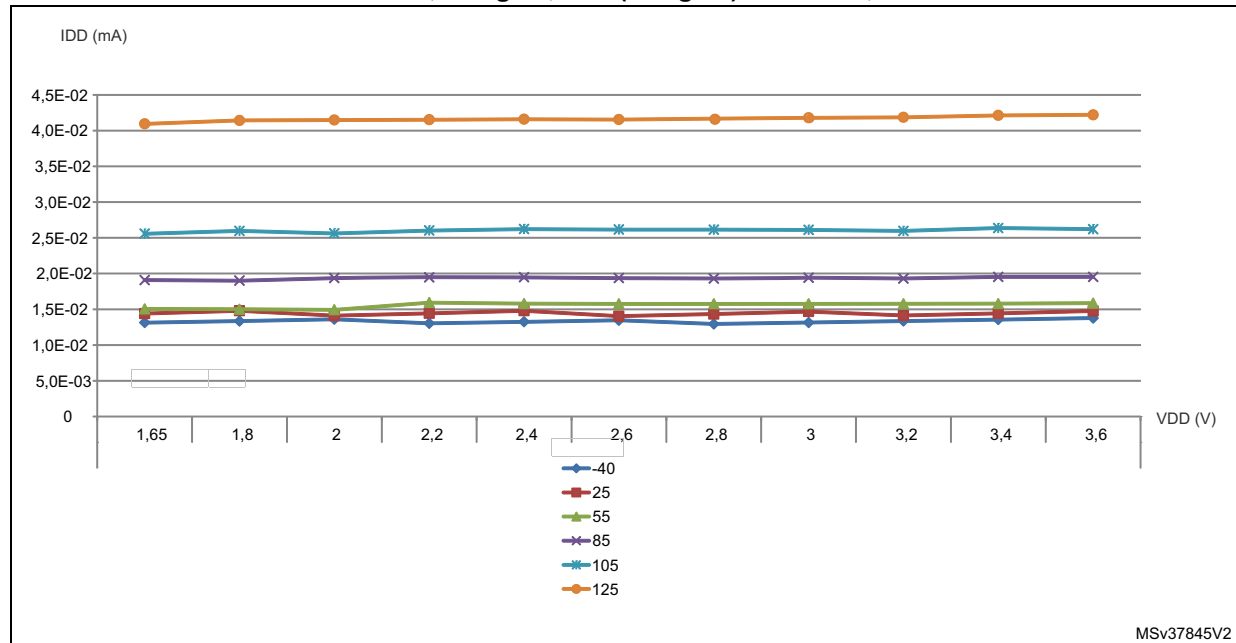**Figure 16. I_{DD} vs V_{DD}, at T_A= 25 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**

Table 36. Current consumption in Low-power sleep mode

Symbol	Parameter	Condition		Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, code executed from Flash memory, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK}= 32 kHz, Flash memory OFF, T_A = − 40 to 25°C	4,7	-	µA
			MSI clock = 65 kHz, f_{HCLK}= 32 kHz, T_A = − 40 to 25°C	17	24	
			T_A = 85°C	19,5	30	
			T_A = 105°C	23	47	
			T_A= 125°C	32,5	70	
			MSI clock = 65 kHz, f_{HCLK}= 65 kHz, T_A= − 40 to 25°C	17	24	
			T_A= 85°C	20	31	
			T_A = 105°C	23,5	47	
			T_A = 125°C	32,5	70	
			MSI clock = 131kHz, f_{HCLK}= 131 kHz, T_A= − 40 to 25°C	19,5	27	
			T_A = 55°C	20,5	28	
			T_A = 85°C	22,5	33	
			T_A = 105°C	26	50	
			T_A= 125°C	35	73	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Table 40. Peripheral current consumption in Run or Sleep mode[1] (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	ADC1[2]	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0[3]	0[3]	0[3]	0[3]	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
	AES	0[3]	0[3]	0[3]	0[3]	
All enabled		204	162	130	202	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. HSI oscillator is off for this measure.

3. Current consumption is negligible and close to 0 µA.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 45. HSE oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
G_m	Maximum critical crystal transconductance	Startup	-	-	700	µA /V
$t_{SU(HSE)}$[2]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.

2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website *www.st.com*.

Figure 21. HSE oscillator circuit diagram
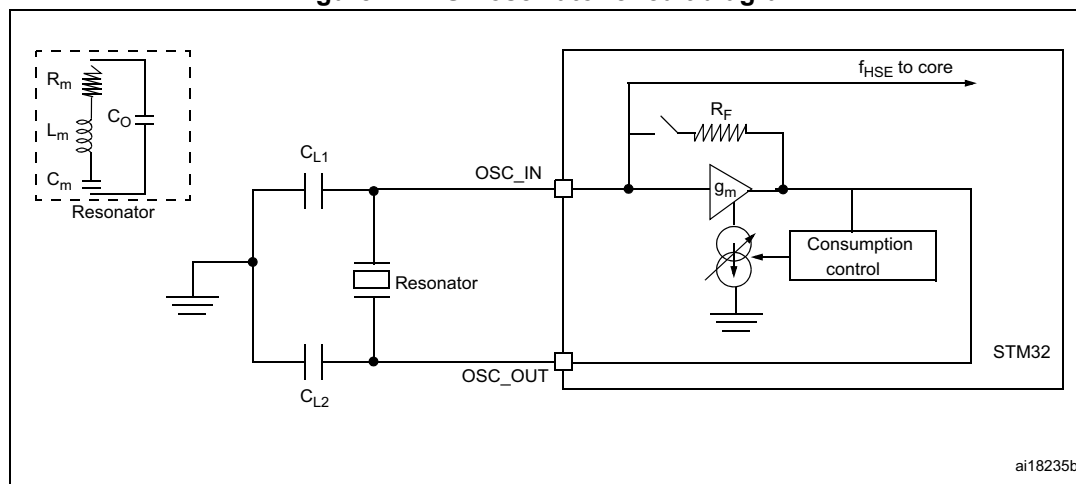
6.3.9 Memory characteristics

RAM memory

Table 52. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode[1]	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 53. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	$T_A = 25\ °C$, $V_{DD} = 3.6\ V$	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 54. Flash memory and data EEPROM endurance and retention

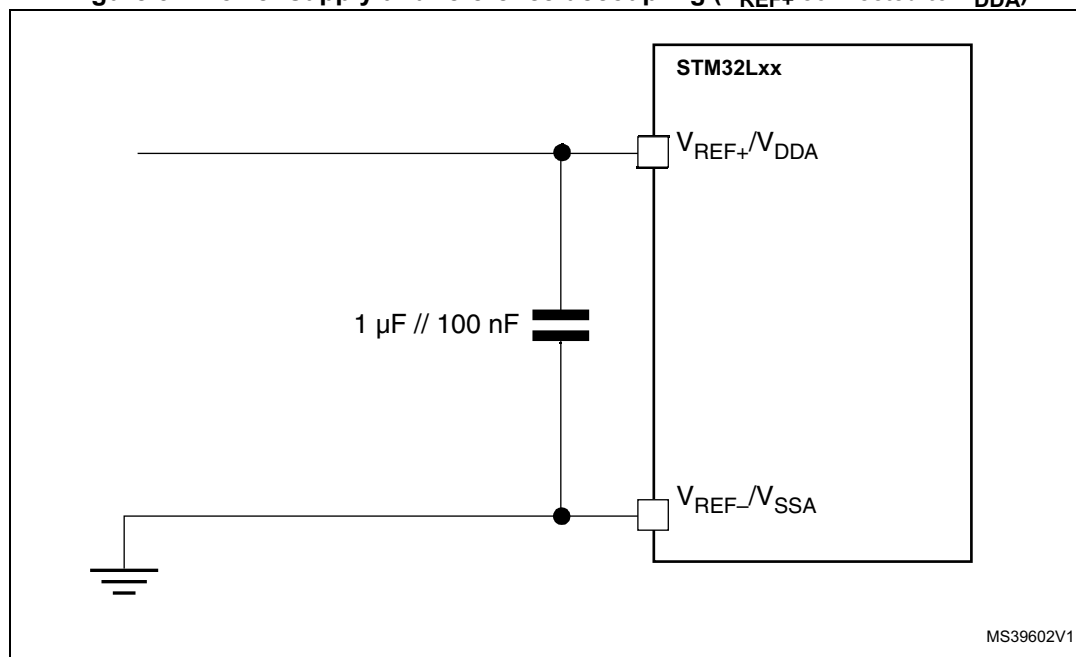| Symbol	Parameter	Conditions	Value Min[1]	Unit
N_{CYC}[2]	Cycling (erase / write) Program memory	$T_A = -40°C$ to $105\ °C$	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	$T_A = -40°C$ to $125\ °C$	0.2	
	Cycling (erase / write) EEPROM data memory		2	

Figure 31. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

Table 76. SPI characteristics in voltage Range 2 [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65 < V_{DD} < 3.6V$			8	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$			8[2]	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	11	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	20	56.5	
$t_{v(MO)}$		Master mode	-	5	9	
$t_{h(SO)}$	Data output hold time	Slave mode	13	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

1. Guaranteed by characterization results.

2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

I2S characteristics

Table 78. I2S characteristics[1]

| Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs [2]	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	15	ns
$t_{h(WS)}$	WS hold time	Master mode	11	-	
$t_{su(WS)}$	WS setup time	Slave mode	6	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	6.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	18	-	
$t_{h(SD\_SR)}$		Slave receiver	15.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	77	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	8	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	18	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.

2. 256xFs maximum value is equal to the maximum clock frequency.

Note: *Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

7.2 UFBGA100 package information

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline
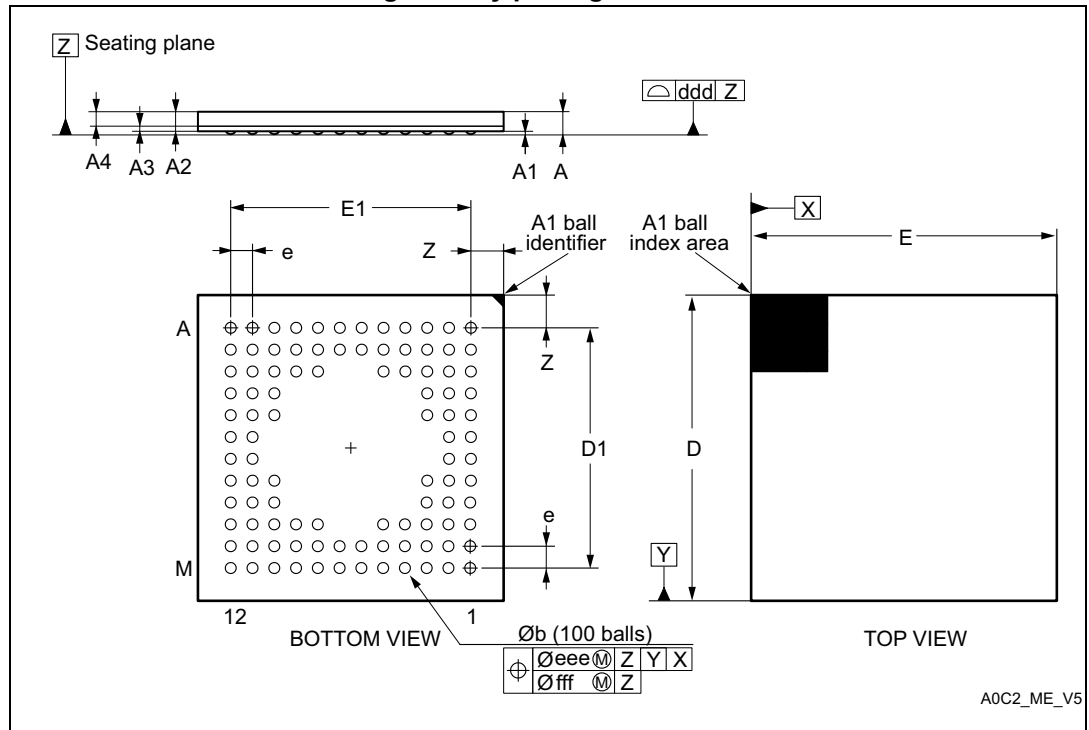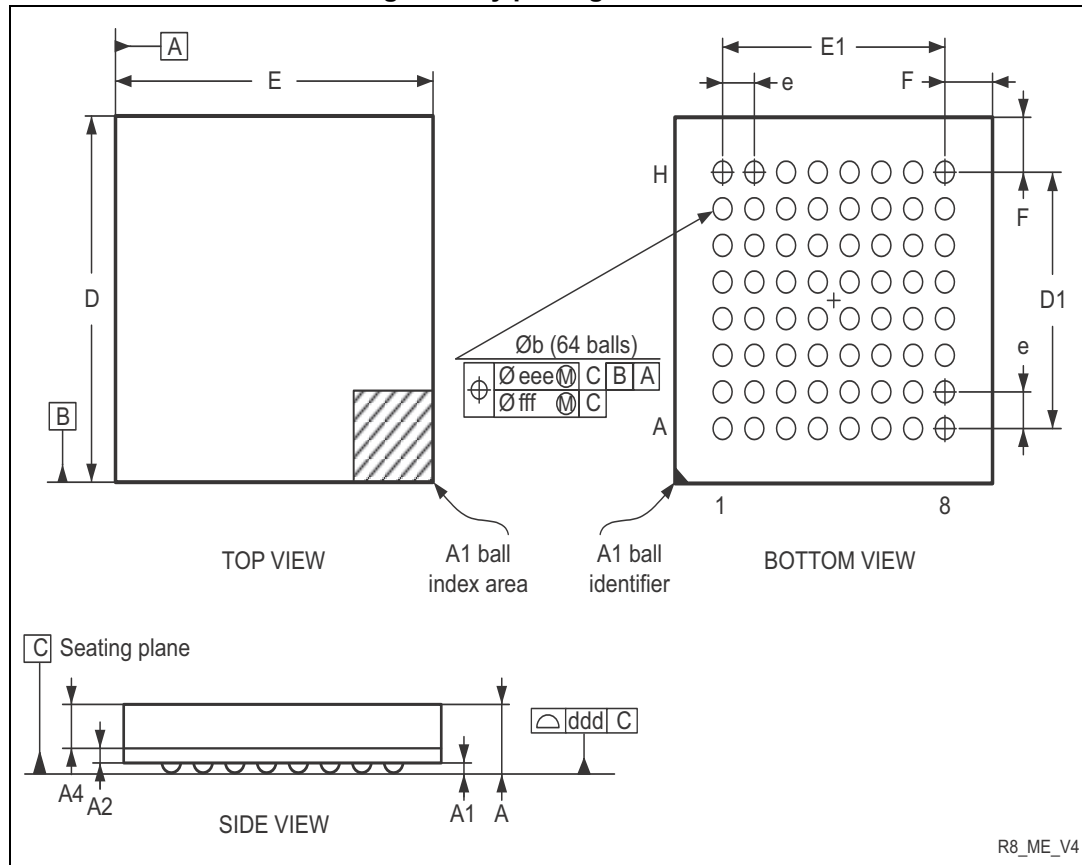

1. Drawing is not to scale.

Table 84. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

7.4 TFBGA64 package information

Figure 48. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline

1. Drawing is not to scale.

Table 87. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

Table 87. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint
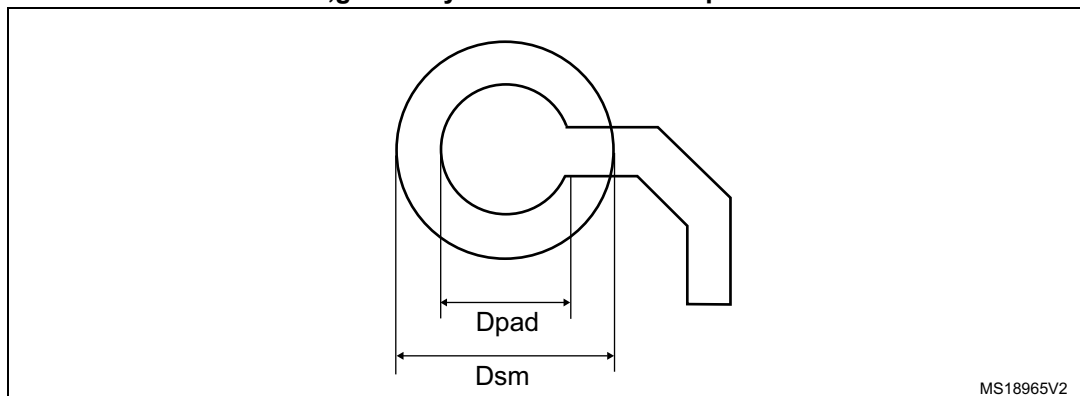

**Table 88. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: *Non solder mask defined (NSMD) pads are recommended.*

4 to 6 mils solder paste screen printing process.

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 50. TFBGA64 marking example (package top view)
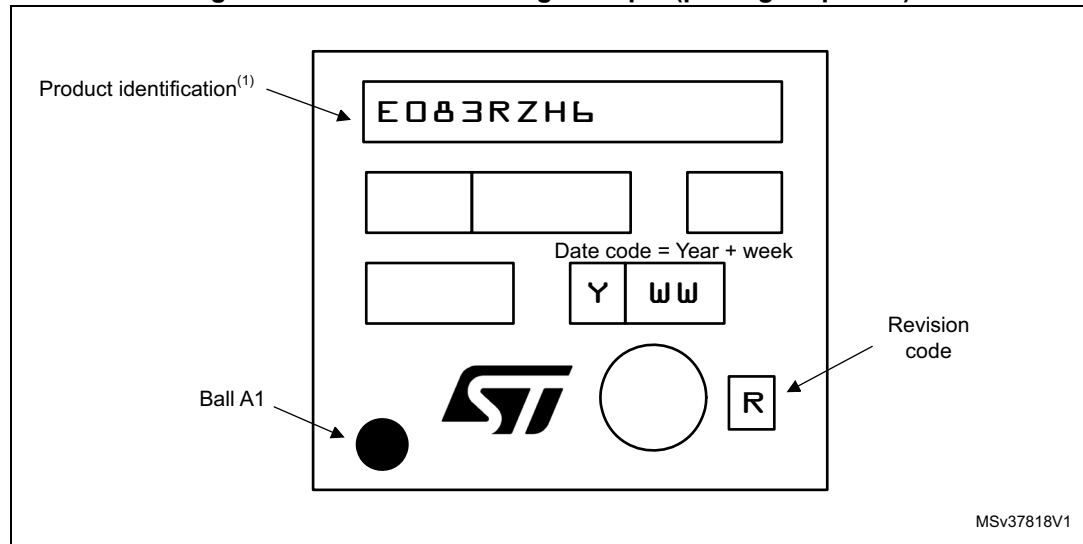
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 54. Thermal resistance
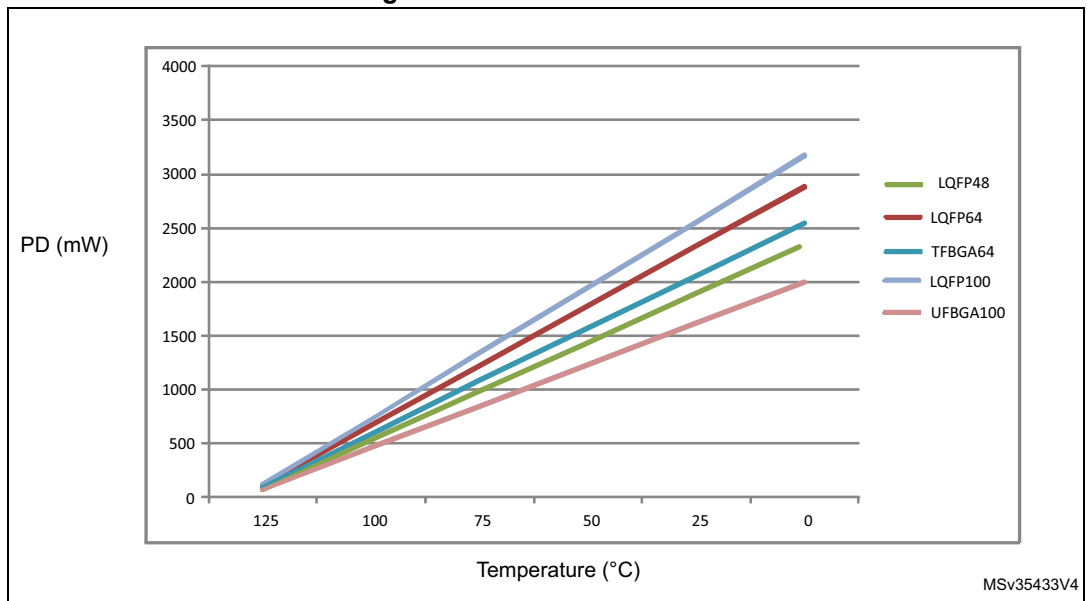
7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.