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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2104bbd48-151

- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute whilst the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell enables non-intrusive high speed real-time tracing of instruction execution.
- Multiple serial interfaces including two UARTs (16C550), Fast I²C-bus (400 kbit/s), and SPI.
- Two 32-bit timers (7 capture/compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Up to thirty-two 5 V tolerant general purpose I/O pins in a tiny LQFP48 (7 mm × 7 mm) package.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
 - ◆ CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 8.3 %).
 - ◆ I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2104BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2104FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2104FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	Port 0: Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.
P0.0/TXD0/PWM1	13 ^[1]	I/O	P0.0 — Port 0 bit 0.
		O	TXD0 — Transmitter output for UART 0.
		O	PWM1 — Pulse Width Modulator output 1.
P0.1/RXD0/PWM3	14 ^[1]	I/O	P0.1 — Port 0 bit 1.
		I	RXD0 — Receiver input for UART 0.
		O	PWM3 — Pulse Width Modulator output 3.
P0.2/SCL/CAP0.0	18 ^[2]	I/O	P0.2 — Port 0 bit 2. The output is open-drain.
		I/O	SCL — I ² C-bus clock input/output. Open-drain output (for I ² C-bus compliance).
		I	CAP0.0 — Capture input for Timer 0, channel 0.
P0.3/SDA/MAT0.0	21 ^[2]	I/O	P0.3 — Port 0 bit 3. The output is open-drain.
		I/O	SDA — I ² C-bus data input/output. Open-drain output (for I ² C-bus compliance).
		O	MAT0.0 — Match output for Timer 0, channel 0. The output is open-drain.
P0.4/SCK/CAP0.1	22 ^[1]	I/O	P0.4 — Port 0 bit 4.
		I/O	SCK — Serial clock for SPI/SSP ^[3] . Clock output from master or input to slave.
		I	CAP0.1 — Capture input for Timer 0, channel 1.
P0.5/MISO/MAT0.1	23 ^[1]	I/O	P0.5 — Port 0 bit 5.
		I/O	MISO — Master In Slave Out for SPI/SSP ^[3] . Data input to SPI/SSP master or data output from SPI/SSP slave.
		O	MAT0.1 — Match output for Timer 0, channel 1.
P0.6/MOSI/CAP0.2	24 ^[1]	I/O	P0.6 — Port 0 bit 6.
		I/O	MOSI — Master Out Slave In for SPI/SSP ^[3] . Data output from SPI/SSP master or data input to SPI/SSP slave.
		I	CAP0.2 — Capture input for Timer 0, channel 2.
P0.7/SSEL/PWM2	28 ^[1]	I/O	P0.7 — Port 0 bit 7.
		I	SSEL — Slave Select for SPI/SSP ^[3] . Selects the SPI/SSP interface as a slave.
		O	PWM2 — Pulse Width Modulator output 2.
P0.8/TXD1/PWM4	29 ^[1]	I/O	P0.8 — Port 0 bit 8.
		O	TXD1 — Transmitter output for UART 1.
		O	PWM4 — Pulse Width Modulator output 4.
P0.9/RXD1/PWM6	30 ^[1]	I/O	P0.9 — Port 0 bit 9.
		I	RXD1 — Receiver input for UART 1.
		O	PWM6 — Pulse Width Modulator output 6.
P0.10/RTS1/CAP1.0	35 ^[1]	I/O	P0.10 — Port 0 bit 10.
		O	RTS1 — Request to Send output for UART 1.
		I	CAP1.0 — Capture input for Timer 1, channel 0.

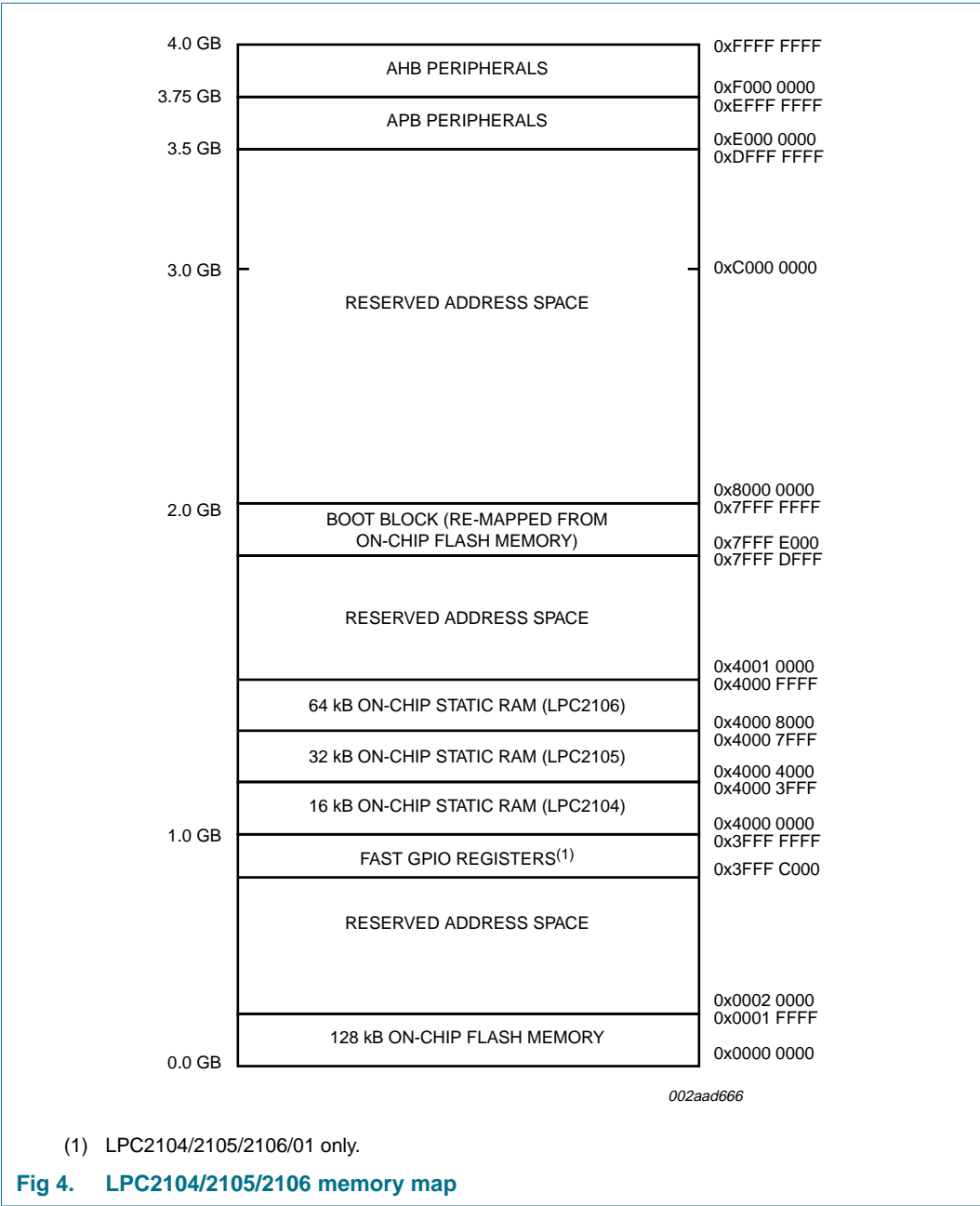
Table 3. Pin description ...continued

Symbol	Pin	Type	Description
P0.11/CTS1/CAP1.1	36 ^[1]	I/O	P0.11 — Port 0 bit 11.
		I	CTS1 — Clear to Send input for UART 1.
		I	CAP1.1 — Capture input for Timer 1, channel 1.
P0.12/DSR1/MAT1.0	37 ^[1]	I/O	P0.12 — Port 0 bit 12.
		I	DSR1 — Data Set Ready input for UART 1.
		O	MAT1.0 — Match output for Timer 1, channel 0.
P0.13/DTR1/MAT1.1	41 ^[1]	I/O	P0.13 — Port 0 bit 13.
		O	DTR1 — Data Terminal Ready output for UART 1.
		O	MAT1.1 — Match output for Timer 1, channel 1.
P0.14/DCD1/EINT1	44 ^[1]	I/O	P0.14 — Port 0 bit 14.
		I	DCD1 — Data Carrier Detect input for UART 1.
		I	EINT1 — External interrupt 1 input.
P0.15/RI1/EINT2	45 ^[1]	I/O	P0.15 — Port 0 bit 15.
		I	RI1 — Ring Indicator input for UART 1.
		O	EINT2 — External interrupt 2 input.
P0.16/EINT0/MAT0.2	46 ^[1]	I/O	P0.16 — Port 0 bit 16.
		I	EINT0 — External interrupt 0 input.
		O	MAT0.2 — Match output for Timer 0, channel 2.
P0.17/CAP1.2/TRST	47 ^[1]	I/O	P0.17 — Port 0 bit 17.
		I	CAP1.2 — Capture input for Timer 1, channel 2.
		I	TRST — Test Reset for JTAG interface, primary JTAG pin group.
P0.18/CAP1.3/TMS	48 ^[1]	I/O	P0.18 — Port 0 bit 18.
		I	CAP1.3 — Capture input for Timer 1, channel 3.
		I	TMS — Test Mode Select for JTAG interface, primary JTAG pin group.
P0.19/MAT1.2/TCK	1 ^[1]	I/O	P0.19 — Port 0 bit 19.
		O	MAT1.2 — Match output for Timer 1, channel 2.
		I	TCK — Test Clock for JTAG interface, primary JTAG pin group.
P0.20/MAT1.3/TDI	2 ^[1]	I/O	P0.20 — Port 0 bit 20.
		O	MAT1.3 — Match output for Timer 1, channel 3.
		I	TDI — Test Data In for JTAG interface, primary JTAG pin group.
P0.21/PWM5/TDO	3 ^[1]	I/O	P0.21 — Port 0 bit 21.
		O	PWM5 — Pulse Width Modulator output 5.
		O	TDO — Test Data Out for JTAG interface, primary JTAG pin group.
P0.22/TRACECLK	32 ^[4]	I/O	P0.22 — Port 0 bit 22.
		O	TRACECLK — Trace Clock. Standard I/O port with internal pull-up.
P0.23/PIPESTAT0	33 ^[4]	I/O	P0.23 — Port 0 bit 23.
		O	PIPESTAT0 — Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P0.24/PIPESTAT1	34 ^[4]	I/O	P0.24 — Port 0 bit 24.
		O	PIPESTAT1 — Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P0.25/PIPESTAT2	38 ^[4]	I/O	P0.25 — Port 0 bit 25.
		O	PIPESTAT2 — Pipeline Status, bit 2. Standard I/O port with internal pull-up.

6.4 Memory map

The LPC2104/2105/2106 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in [Section 6.18 “System control”](#).



6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the Interrupt Request (IRQ) inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

[Table 4](#) lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 2 (CR0, CR1, CR2)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART 0	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) Auto-Baud Time-Out (ABTO) ^[1] End of Auto-Baud (ABEO) ^[1]	6

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000)

PINSEL0	Pin name	Value		Function	Value after reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TXD (UART 0)	
		1	0	PWM1	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RXD (UART 0)	
		1	0	PWM3	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL (I ² C-bus)	
		1	0	Capture 0.0 (Timer 0)	
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA (I ² C-bus)	
		1	0	Match 0.0 (Timer 0)	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK (SPI/SSP)	
		1	0	Capture 0.1 (Timer 0)	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI/SSP)	
		1	0	Match 0.1 (Timer 0)	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI/SSP)	
		1	0	Capture 0.2 (Timer 0)	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI/SSP)	
		1	0	PWM2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD (UART 1)	
		1	0	PWM4	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD (UART 1)	
		1	0	PWM6	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS (UART 1)	
		1	0	Capture 1.0 (Timer 1)	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS (UART 1)	
		1	0	Capture 1.1 (Timer 1)	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR (UART 1)	
		1	0	Match 1.0 (Timer 1)	

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000) ...continued

PINSEL0	Pin name	Value		Function	Value after reset
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR (UART 1)	
		1	0	Match 1.1 (Timer 1)	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD (UART 1)	
		1	0	EINT1	
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI (UART 1)	
		1	0	EINT2	

6.8 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in [Table 7](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically.

Remark: The primary JTAG port and the trace port can be selected only through the DBGSEL pin at reset (Debug mode). Function control for the pins P0[31:17] is effective only when the DBGSEL input is pulled LOW during reset.

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
13:12	P0.22	0	0	GPIO Port 0.22	0
15:14	P0.23	0	0	GPIO Port 0.23	0
17:16	P0.24	0	0	GPIO Port 0.24	0
19:18	P0.25	0	0	GPIO Port 0.25	0
21:20	P0.26	0	0	GPIO Port 0.26	0
23:22	P0.27	0	0	GPIO Port 0.27	0
		0	1	TRST	

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004) ...continued

PINSEL1	Pin name	Value		Function	Value after reset
25:24	P0.28	0	0	GPIO Port 0.28	0
		0	1	TMS	
27:26	P0.29	0	0	GPIO Port 0.29	0
		0	1	TCK	
29:28	P0.30	0	0	GPIO Port 0.30	0
		0	1	TDI	
31:30	P0.31	0	0	GPIO Port 0.31	0
		0	1	TDO	

6.9 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.9.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.9.2 Features added with the Fast GPIO set of registers available on LPC2104/2105/2106/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.10 UARTs

The LPC2104/2105/2106 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.10.1 Features

- 16 byte Receive and Transmit FIFOs
- Register locations conform to 16C550 industry standard
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in baud rate generator

- Standard modem interface signals included on UART 1.

6.10.2 UART features available in LPC2104/2105/2106/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2104/2105/2106/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Autobauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.11 I²C-bus serial I/O controller

I²C is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. I²C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2104/2105/2106 supports bit rate up to 400 kbit/s (Fast I²C-bus).

6.11.1 Features

- Standard I²C compliant bus interface.
- Easy to configure as Master, Slave or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, serial, full duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12.2 Features available in LPC2104/2105/2106/01 only

- Selectable transfer width of eight to 16 bit per frame.
- When the SPI interface is used in Master mode, the SSEL pin is not needed (can be used for a different function).

6.13 SSP controller (LPC2104/2105/2106/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

Because the SSP and SPI peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI to SSP and back.

6.13.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.14 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Up to four (Timer 1) and three (Timer 0) 32-bit capture channels, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Up to four (Timer 1) and three (Timer 0) external outputs corresponding to match registers, with the following capabilities:
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.

6.14.2 Features available in LPC2104/2105/2106/01 only

The LPC2104/2105/2106/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $\frac{PCLK}{4}$. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than $\frac{1}{2}PCLK$.

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.

- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from $(T_{cy(PCLK)} \times 256 \times 4)$ to $(T_{cy(PCLK)} \times 2^{32} \times 4)$ in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2104/2105/2106. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2104/2105/2106: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2104/2105/2106/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection:

1. CRP1 disables access to the chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2104/2105/2106 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Each of these functions requires a trade-off of debugging features versus device pins. Because the LPC2104/2105/2106 are provided in a small package, there is no room for permanently assigned JTAG or Trace pins. An alternate JTAG port allows an option to debug functions assigned to the pins used by the primary JTAG port (see [Section 6.8](#)).

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace

Since the LPC2104/2105/2106 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

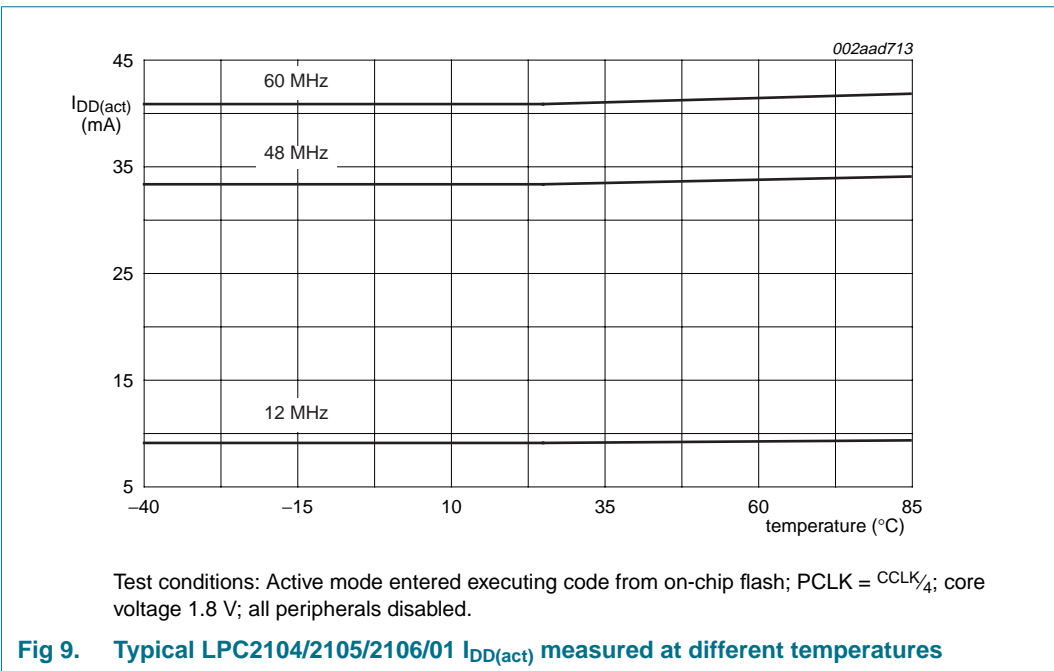
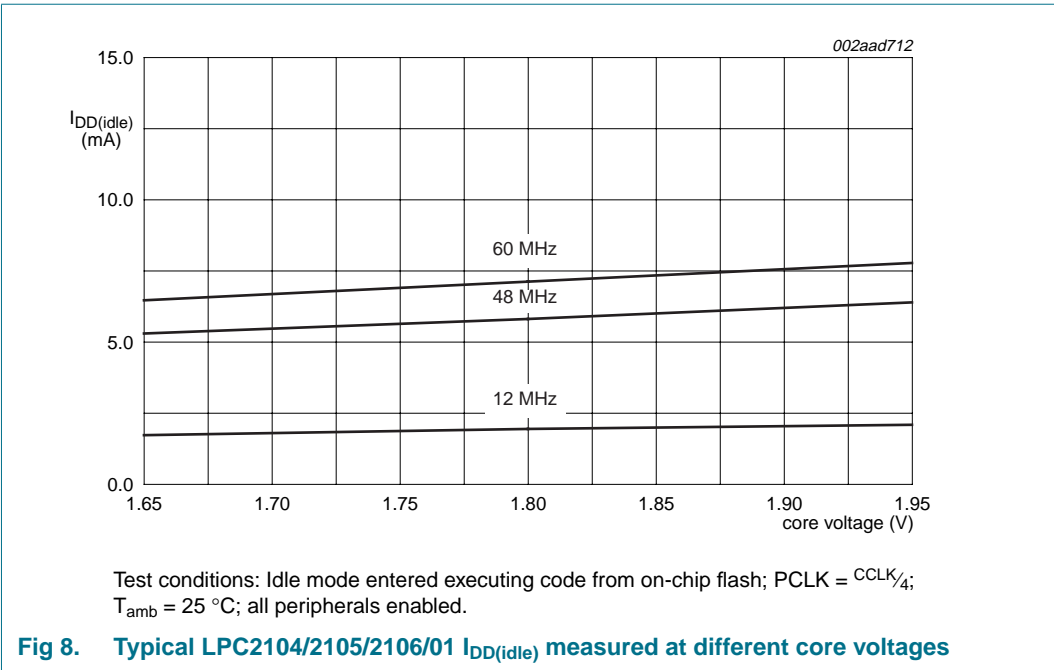
The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

Table 9. Static characteristics ...continued $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
LPC2104/2105/2106 and LPC2104/2105/2106/00 power consumption						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP register but not configured to run	-	35	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C,	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	50	500	μA
LPC2104/2105/2106/01 power consumption						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP register but not configured to run ^[11]	-	40	-	mA
I _{DD(idle)}	Idle mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP register but not configured to run ^[11]	-	7	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C,	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	-	300	μA
I ² C-bus pins						
V _{IH}	HIGH-state input voltage		0.7V _{DD(3V3)}	-	-	V
V _{IL}	LOW-state input voltage		-	-	0.3V _{DD(3V3)}	V
V _{hys}	hysteresis voltage		-	0.5V _{DD(3V3)}	-	V
V _{OL}	LOW-state output voltage	I _{OLS} = 3 mA	^[7] -	-	0.4	V
I _{LI}	input leakage current	V _I = V _{DD(3V3)}	^[12] -	2	4	μA
		V _I = 5 V	-	10	22	μA



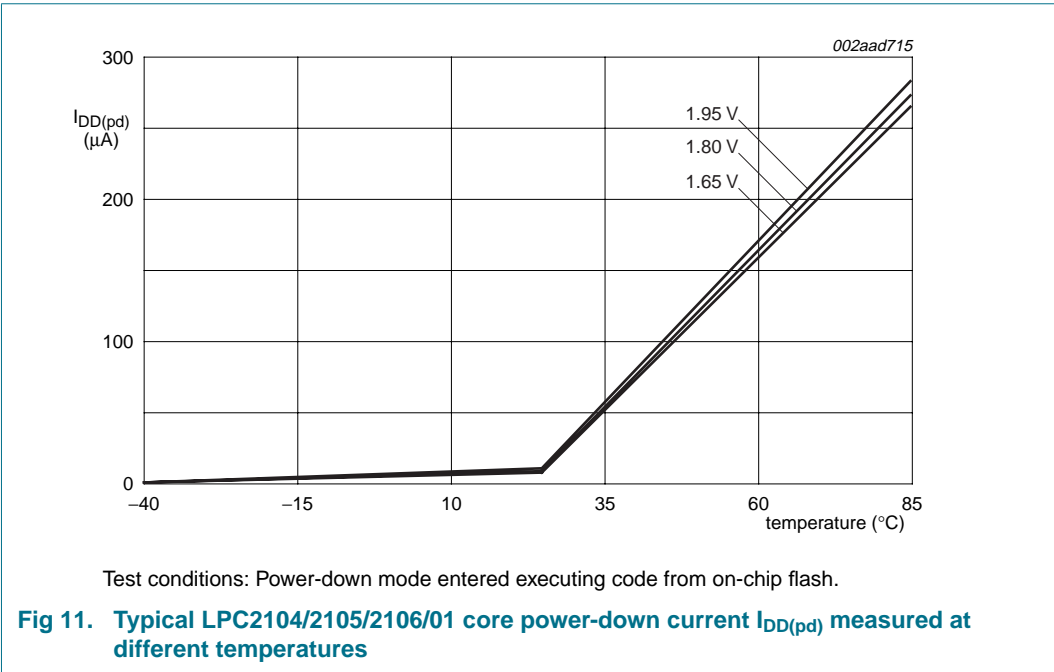
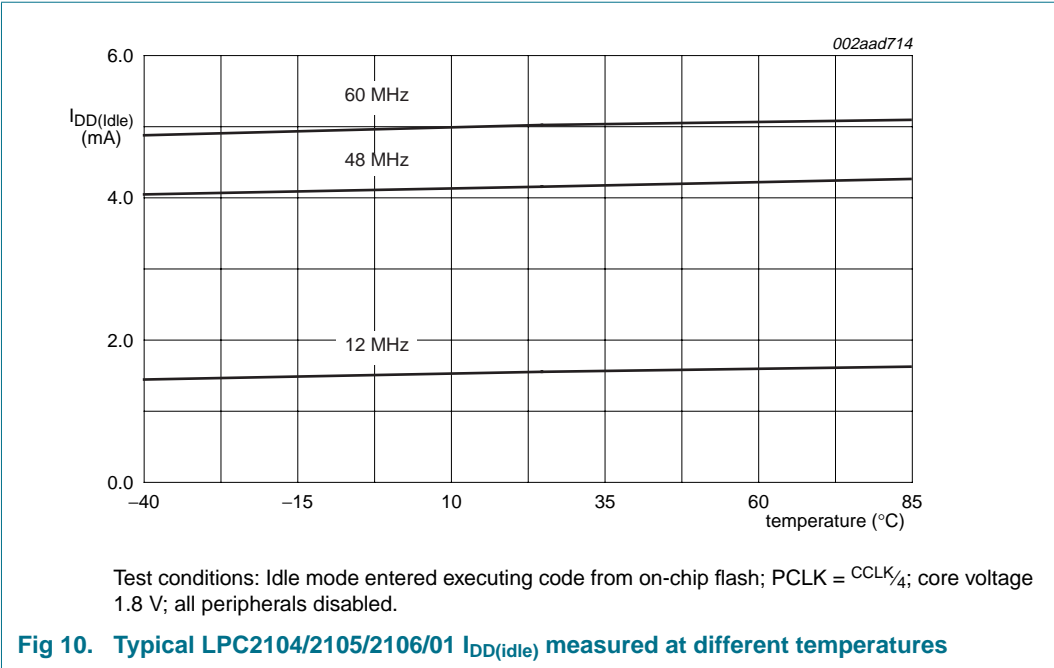


Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
 Core voltage 1.8 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; all measurements in mA; PCLK = CCLK/4

Peripheral	CCLK = 60 MHz
Timer 0	0.258
Timer 1	0.254
UART 0	0.494
UART 1	0.561

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
...continued

Peripheral	CCLK = 60 MHz
PWM0	0.511
I ² C-bus	0.078
SPI	0.060
RTC	0.109
SSP	0.377

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter