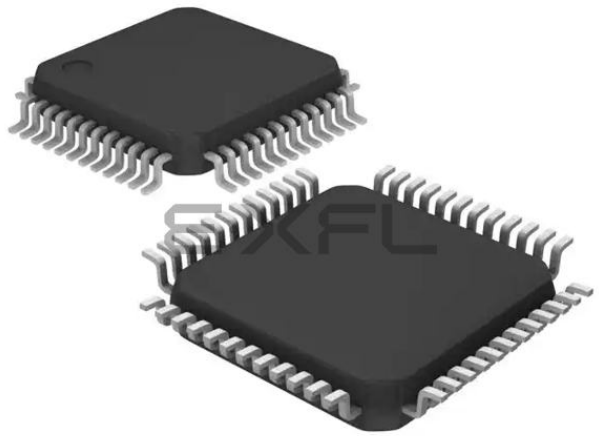

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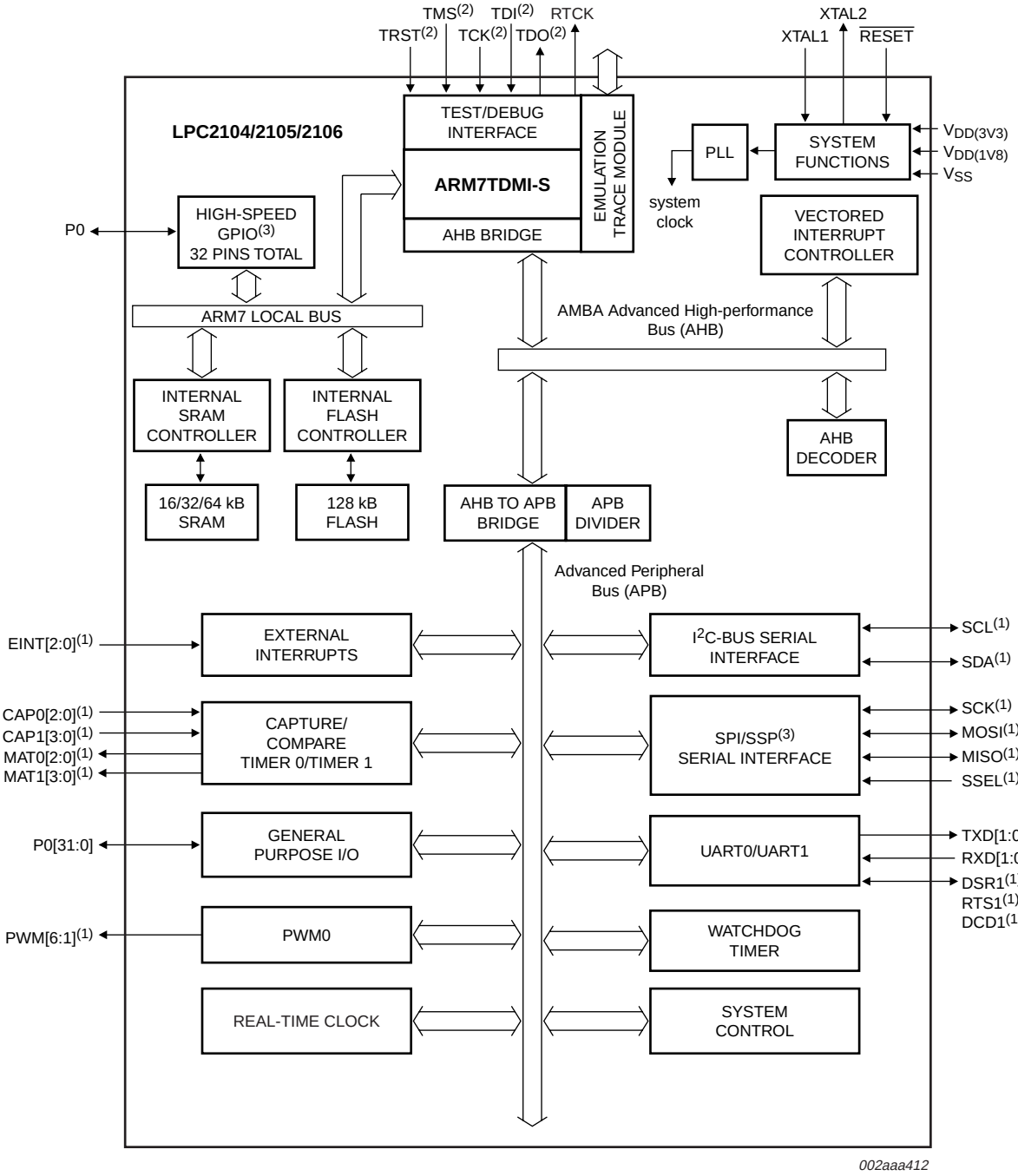
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2104fbd48-01-15

4. Block diagram



(1) Shared with GPIO.

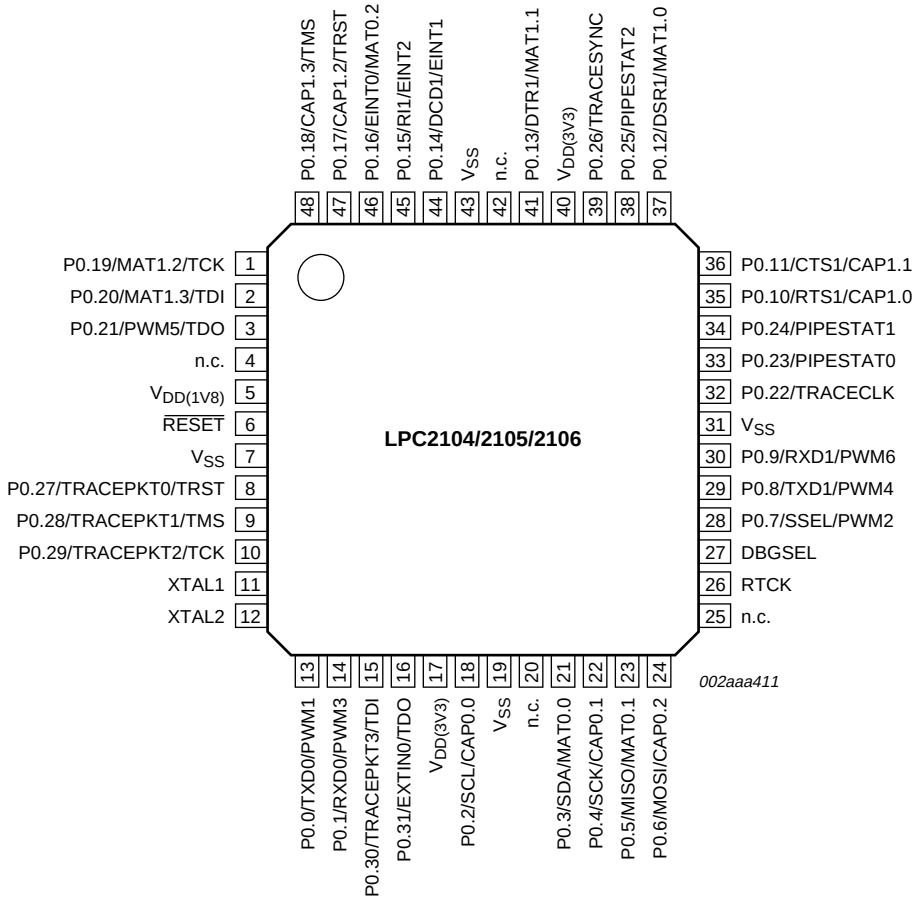
(2) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(3) Available on LPC2104/2105/2106/01 only.

Fig 1. Block diagram

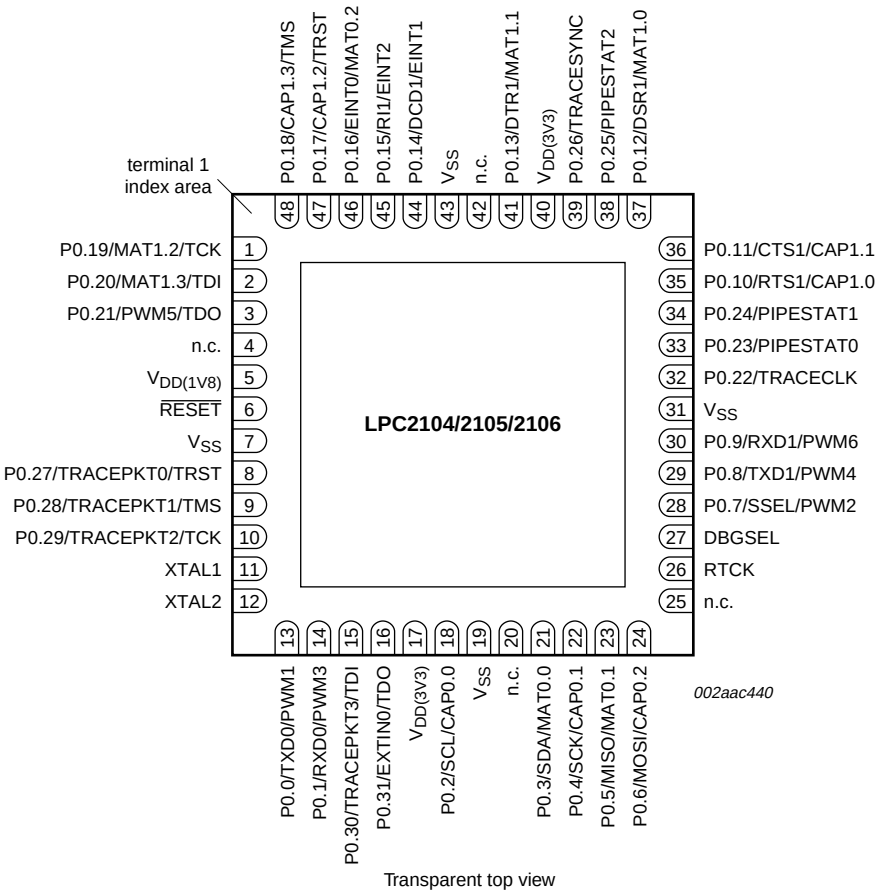
5. Pinning information

5.1 Pinning



Pin configuration is identical for all LQFP48 packages.

Fig 2. Pin configuration (LQFP48)



Pin configuration is identical for LPC2106FHN48, LPC2106FHN48/00, and LPC2106FHN48/01.

Fig 3. Pin configuration (HVQFN48)

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.
P0.0/TXD0/PWM1	13[1]	I/O	**P0.0 —** Port 0 bit 0.
		O	**TXD0 —** Transmitter output for UART 0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/PWM3	14[1]	I/O	**P0.1 —** Port 0 bit 1.
		I	**RXD0 —** Receiver input for UART 0.
		O	**PWM3 —** Pulse Width Modulator output 3.
P0.2/SCL/CAP0.0	18[2]	I/O	**P0.2 —** Port 0 bit 2. The output is open-drain.
		I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/MAT0.0	21[2]	I/O	**P0.3 —** Port 0 bit 3. The output is open-drain.
		I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0. The output is open-drain.
P0.4/SCK/CAP0.1	22[1]	I/O	**P0.4 —** Port 0 bit 4.
		I/O	**SCK —** Serial clock for SPI/SSP[3]. Clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO/MAT0.1	23[1]	I/O	**P0.5 —** Port 0 bit 5.
		I/O	**MISO —** Master In Slave Out for SPI/SSP[3]. Data input to SPI/SSP master or data output from SPI/SSP slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI/CAP0.2	24[1]	I/O	**P0.6 —** Port 0 bit 6.
		I/O	**MOSI —** Master Out Slave In for SPI/SSP[3]. Data output from SPI/SSP master or data input to SPI/SSP slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL/PWM2	28[1]	I/O	**P0.7 —** Port 0 bit 7.
		I	**SSEL —** Slave Select for SPI/SSP[3]. Selects the SPI/SSP interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
P0.8/TXD1/PWM4	29[1]	I/O	**P0.8 —** Port 0 bit 8.
		O	**TXD1 —** Transmitter output for UART 1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0.9/RXD1/PWM6	30[1]	I/O	**P0.9 —** Port 0 bit 9.
		I	**RXD1 —** Receiver input for UART 1.
		O	**PWM6 —** Pulse Width Modulator output 6.
P0.10/RTS1/CAP1.0	35[1]	I/O	**P0.10 —** Port 0 bit 10.
		O	**RTS1 —** Request to Send output for UART 1.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2104/2105/2106 incorporate a 128 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120 kB of flash memory is available for user code.

The LPC2104/2105/2106 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2104/2105/2106 provide 16/32/64 kB of static RAM, respectively.

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000)

PINSEL0	Pin name	Value		Function	Value after reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TXD (UART 0)	
		1	0	PWM1	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RXD (UART 0)	
		1	0	PWM3	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL (I^2C-bus)	
		1	0	Capture 0.0 (Timer 0)	
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA (I^2C-bus)	
		1	0	Match 0.0 (Timer 0)	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK (SPI/SSP)	
		1	0	Capture 0.1 (Timer 0)	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI/SSP)	
		1	0	Match 0.1 (Timer 0)	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI/SSP)	
		1	0	Capture 0.2 (Timer 0)	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI/SSP)	
		1	0	PWM2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD (UART 1)	
		1	0	PWM4	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD (UART 1)	
		1	0	PWM6	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS (UART 1)	
		1	0	Capture 1.0 (Timer 1)	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS (UART 1)	
		1	0	Capture 1.1 (Timer 1)	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR (UART 1)	
		1	0	Match 1.0 (Timer 1)	

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004) *...continued*

PINSEL1	Pin name	Value		Function	Value after reset
25:24	P0.28	0	0	GPIO Port 0.28	0
		0	1	TMS	
27:26	P0.29	0	0	GPIO Port 0.29	0
		0	1	TCK	
29:28	P0.30	0	0	GPIO Port 0.30	0
		0	1	TDI	
31:30	P0.31	0	0	GPIO Port 0.31	0
		0	1	TDO	

6.9 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.9.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.9.2 Features added with the Fast GPIO set of registers available on LPC2104/2105/2106/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.10 UARTs

The LPC2104/2105/2106 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.10.1 Features

- 16 byte Receive and Transmit FIFOs
- Register locations conform to 16C550 industry standard
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in baud rate generator

- Standard modem interface signals included on UART 1.

6.10.2 UART features available in LPC2104/2105/2106/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2104/2105/2106/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Autobauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.11 I^2C-bus serial I/O controller

I^2C is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. I^2C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2104/2105/2106 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, serial, full duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12.2 Features available in LPC2104/2105/2106/01 only

- Selectable transfer width of eight to 16 bit per frame.
- When the SPI interface is used in Master mode, the SSEL pin is not needed (can be used for a different function).

6.13 SSP controller (LPC2104/2015/2106/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

Because the SSP and SPI peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI to SSP and back.

6.13.1 Features

- Compatible with Motorola’s SPI, Texas Instrument’s 4-wire SSI, and National Semiconductor’s Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.14 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2104/2105/2106. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must “release” new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called FOSC and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. FOSC and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide

by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2104/2105/2106: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2104/2105/2106/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection:

1. CRP1 disables access to the chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2104/2105/2106 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Each of these functions requires a trade-off of debugging features versus device pins. Because the LPC2104/2105/2106 are provided in a small package, there is no room for permanently assigned JTAG or Trace pins. An alternate JTAG port allows an option to debug functions assigned to the pins used by the primary JTAG port (see Section 6.8).

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace

Since the LPC2104/2105/2106 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][6]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		–2000	+2000	V
		machine model	[12]			
		all pins		–200	+200	V

[1] The following applies to Table 8:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

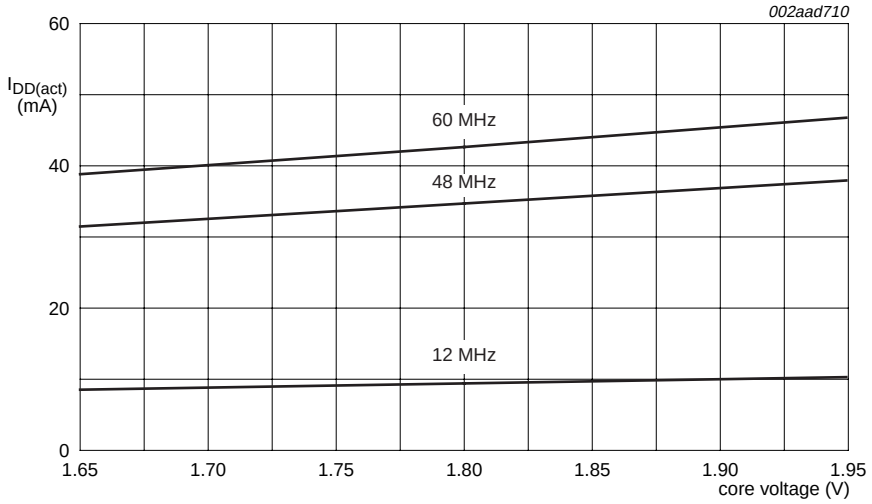
[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω series resistor.

Table 9. Static characteristics *…continued*

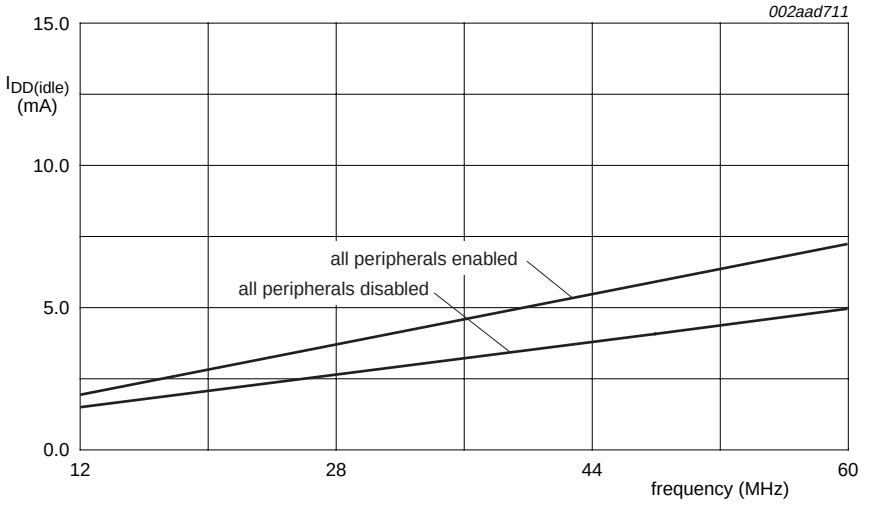
T_{amb} = 0 °C to +70 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
LPC2104/2105/2106 and LPC2104/2105/2106/00 power consumption							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP register but not configured to run		-	35	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	50	500	µA
LPC2104/2105/2106/01 power consumption							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP register but not configured to run[11]		-	40	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP register but not configured to run[11]		-	7	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C,		-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	-	300	µA
I^2C-bus pins							
V_{IH}	HIGH-state input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-state input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD(3V3)}$	-	V
V_{OL}	LOW-state output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	µA
		V_I = 5 V		-	10	22	µA



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled.

Fig 6. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different core voltages

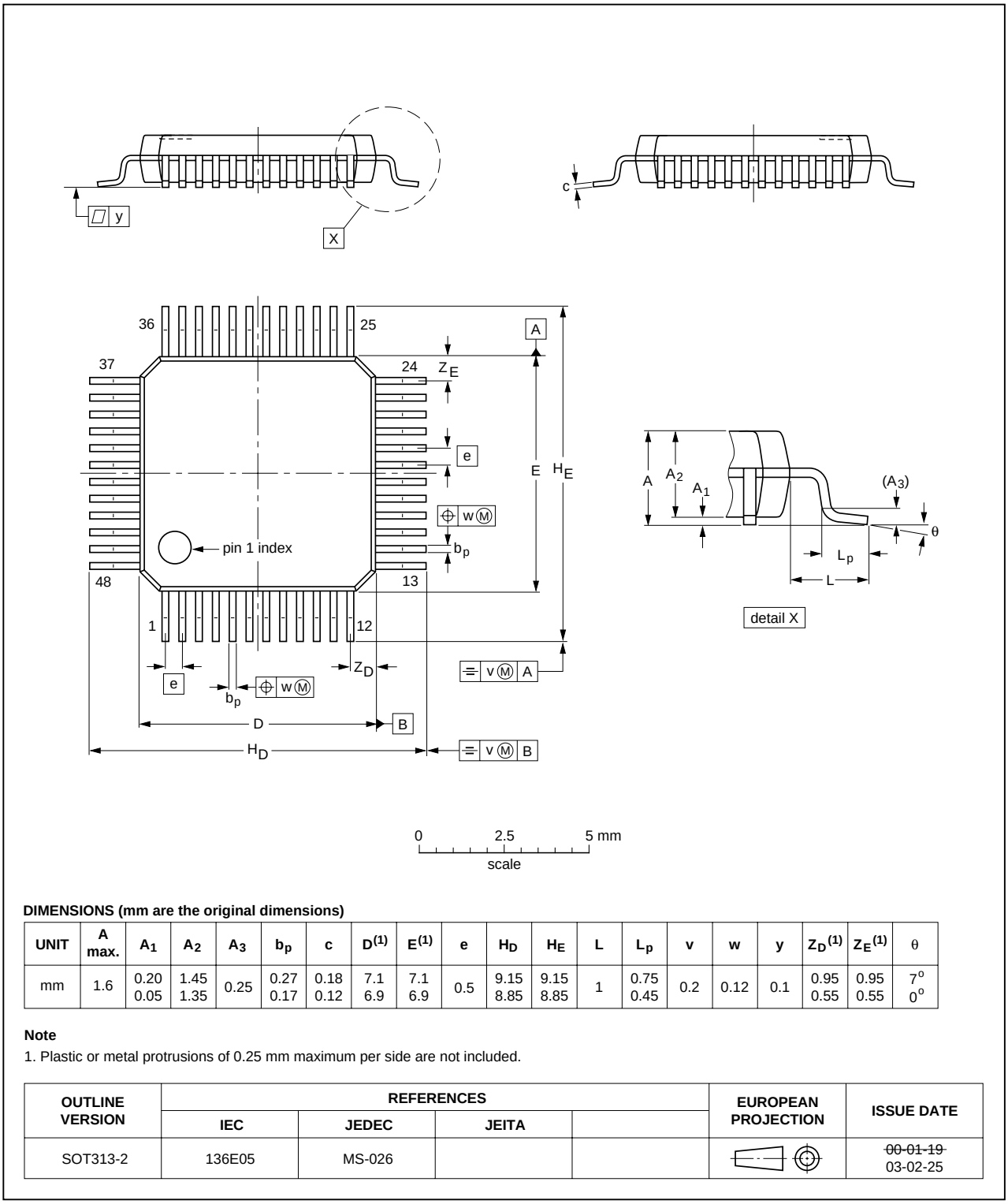


Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

Fig 7. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different frequencies

10. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 13. Package outline SOT313-2 (LQFP48)

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2104_2105_2106_7	20080620	Product data sheet	-	LPC2104_2105_2106_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3 “Ordering information”; corrected temperature range for LPC2104FBD48/00, LPC2105FBD48/00. • Parts LPC2104FBD48/01, LPC2105FBD48/01, LPC2106BBD48, LPC2106FBD48/01, and LPC2106FHN48/01 added. • Description of /01 features added. • LPC2104/2105/2106/01 power consumption measurements added. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Figure 12 “External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)” updated. • Condition for I_{OHS} and I_{OLS} updated in Table 9 “Static characteristics”.			
LPC2104_2105_2106_6	20060725	Product data sheet	-	LPC2104_2105_2106-05
LPC2104_2105_2106-05	20041222	Product data	-	LPC2104_2105_2106-04
LPC2104_2105_2106-04	20040205	Product data	-	LPC2104_2105_2106-03
LPC2104_2105_2106-03	20031007	Product data	-	LPC2104_2105_2106-02
LPC2104_2105_2106-02	20030611	Product data	-	LPC2104_2105_2106-01
LPC2104_2105_2106-01	20030425	Product data	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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