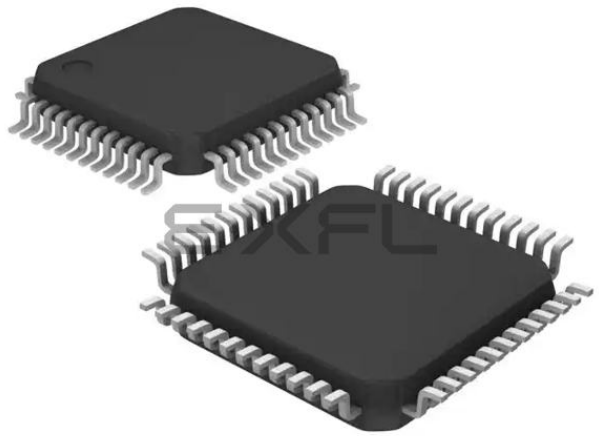

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2105bbd48-151

- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute whilst the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell enables non-intrusive high speed real-time tracing of instruction execution.
- Multiple serial interfaces including two UARTs (16C550), Fast I^2C-bus (400 kbit/s), and SPI.
- Two 32-bit timers (7 capture/compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Up to thirty-two 5 V tolerant general purpose I/O pins in a tiny LQFP48 (7 mm $\times$ 7 mm) package.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 µs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V $\pm$ 8.3 %).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V $\pm$ 10 %) with 5 V tolerant I/O pads.

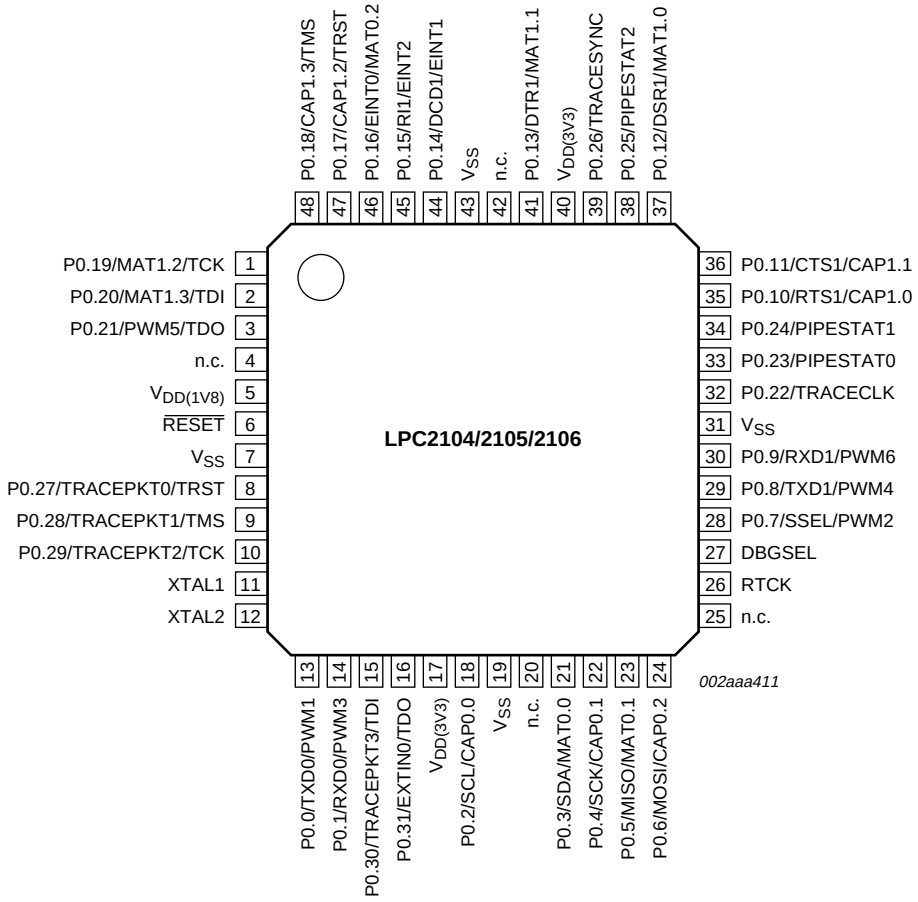
3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2104BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2104FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2104FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2105FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2106BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2
LPC2106FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 $\times$ 7 $\times$ 1.4 mm	SOT313-2

5. Pinning information

5.1 Pinning



Pin configuration is identical for all LQFP48 packages.

Fig 2. Pin configuration (LQFP48)

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.
P0.0/TXD0/PWM1	13[1]	I/O	**P0.0 —** Port 0 bit 0.
		O	**TXD0 —** Transmitter output for UART 0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/PWM3	14[1]	I/O	**P0.1 —** Port 0 bit 1.
		I	**RXD0 —** Receiver input for UART 0.
		O	**PWM3 —** Pulse Width Modulator output 3.
P0.2/SCL/CAP0.0	18[2]	I/O	**P0.2 —** Port 0 bit 2. The output is open-drain.
		I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/MAT0.0	21[2]	I/O	**P0.3 —** Port 0 bit 3. The output is open-drain.
		I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0. The output is open-drain.
P0.4/SCK/CAP0.1	22[1]	I/O	**P0.4 —** Port 0 bit 4.
		I/O	**SCK —** Serial clock for SPI/SSP[3]. Clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO/MAT0.1	23[1]	I/O	**P0.5 —** Port 0 bit 5.
		I/O	**MISO —** Master In Slave Out for SPI/SSP[3]. Data input to SPI/SSP master or data output from SPI/SSP slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI/CAP0.2	24[1]	I/O	**P0.6 —** Port 0 bit 6.
		I/O	**MOSI —** Master Out Slave In for SPI/SSP[3]. Data output from SPI/SSP master or data input to SPI/SSP slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL/PWM2	28[1]	I/O	**P0.7 —** Port 0 bit 7.
		I	**SSEL —** Slave Select for SPI/SSP[3]. Selects the SPI/SSP interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
P0.8/TXD1/PWM4	29[1]	I/O	**P0.8 —** Port 0 bit 8.
		O	**TXD1 —** Transmitter output for UART 1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0.9/RXD1/PWM6	30[1]	I/O	**P0.9 —** Port 0 bit 9.
		I	**RXD1 —** Receiver input for UART 1.
		O	**PWM6 —** Pulse Width Modulator output 6.
P0.10/RTS1/CAP1.0	35[1]	I/O	**P0.10 —** Port 0 bit 10.
		O	**RTS1 —** Request to Send output for UART 1.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.

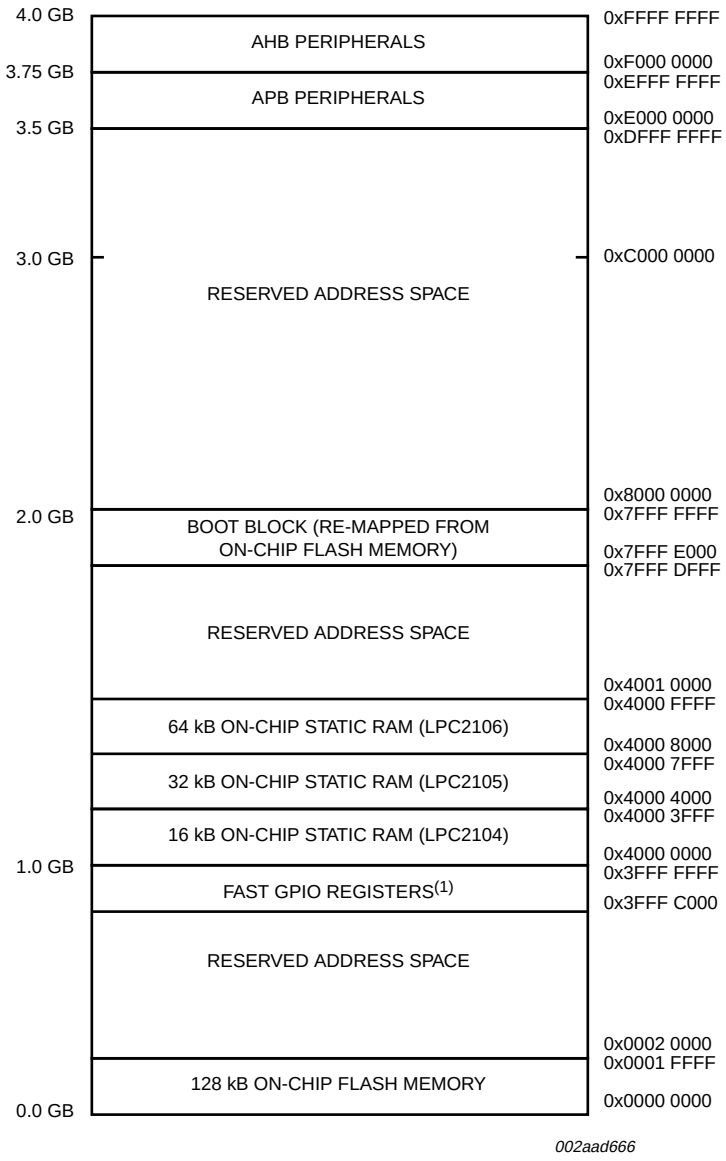
Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/CAP1.1	36[1]	I/O	**P0.11 —** Port 0 bit 11.
		I	**CTS1 —** Clear to Send input for UART 1.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
P0.12/DSR1/MAT1.0	37[1]	I/O	**P0.12 —** Port 0 bit 12.
		I	**DSR1 —** Data Set Ready input for UART 1.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
P0.13/DTR1/MAT1.1	41[1]	I/O	**P0.13 —** Port 0 bit 13.
		O	**DTR1 —** Data Terminal Ready output for UART 1.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
P0.14/DCD1/EINT1	44[1]	I/O	**P0.14 —** Port 0 bit 14.
		I	**DCD1 —** Data Carrier Detect input for UART 1.
		I	**EINT1 —** External interrupt 1 input.
P0.15/RI1/EINT2	45[1]	I/O	**P0.15 —** Port 0 bit 15.
		I	**RI1 —** Ring Indicator input for UART 1.
		O	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/MAT0.2	46[1]	I/O	**P0.16 —** Port 0 bit 16.
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.17/CAP1.2/TRST	47[1]	I/O	**P0.17 —** Port 0 bit 17.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I	**TRST —** Test Reset for JTAG interface, primary JTAG pin group.
P0.18/CAP1.3/TMS	48[1]	I/O	**P0.18 —** Port 0 bit 18.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I	**TMS —** Test Mode Select for JTAG interface, primary JTAG pin group.
P0.19/MAT1.2/TCK	1[1]	I/O	**P0.19 —** Port 0 bit 19.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I	**TCK —** Test Clock for JTAG interface, primary JTAG pin group.
P0.20/MAT1.3/TDI	2[1]	I/O	**P0.20 —** Port 0 bit 20.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**TDI —** Test Data In for JTAG interface, primary JTAG pin group.
P0.21/PWM5/TDO	3[1]	I/O	**P0.21 —** Port 0 bit 21.
		O	**PWM5 —** Pulse Width Modulator output 5.
		O	**TDO —** Test Data Out for JTAG interface, primary JTAG pin group.
P0.22/TRACECLK	32[4]	I/O	**P0.22 —** Port 0 bit 22.
		O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P0.23/PIPESTAT0	33[4]	I/O	**P0.23 —** Port 0 bit 23.
		O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P0.24/PIPESTAT1	34[4]	I/O	**P0.24 —** Port 0 bit 24.
		O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P0.25/PIPESTAT2	38[4]	I/O	**P0.25 —** Port 0 bit 25.
		O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.

6.4 Memory map

The LPC2104/2105/2106 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 "System control".



(1) LPC2104/2105/2106/01 only.

Fig 4. LPC2104/2105/2106 memory map

Table 4. Interrupt sources *...continued*

Block	Flag(s)	VIC channel #
UART 1	Rx Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	Rx Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI)	
	Auto-Baud Time-Out (ABTO)[1]	
	End of Auto-Baud (ABEO)[1]	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C-bus	SI (state change)	9
SPI and SSP[1]	SPIF, MODF (SPI)	10
	TXRIS, RXRIS, RTRIS, RORRIS (SSP)[1]	
-	reserved	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
System Control	External Interrupt 1 (EINT1)	15
System Control	External Interrupt 2 (EINT2)	16

[1] Available on LPC2104/2105/2106/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module contains two registers as shown in Table 5.

Table 5. Pin control module registers

Address	Name	Description	Access
0xE002 C000	PINSEL0	Pin function select register 0	Read/Write
0xE002 C004	PINSEL1	Pin function select register 1	Read/Write

6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 6. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in Table 6 are reserved, and should not be used

- Standard modem interface signals included on UART 1.

6.10.2 UART features available in LPC2104/2105/2106/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2104/2105/2106/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Autobauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.11 I^2C-bus serial I/O controller

I^2C is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. I^2C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2104/2105/2106 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Up to four (Timer 1) and three (Timer 0) 32-bit capture channels, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four (Timer 1) and three (Timer 0) external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.14.2 Features available in LPC2104/2105/2106/01 only

The LPC2104/2105/2106/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $^{PCLK}/_{4}$. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than $^{1}/_{(2PCLK)}$.

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.

- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2104/2105/2106. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) a flash update mechanism using IAP calls or a call to reinvoke ISP command to enable flash update via UART 0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

6.18.5 External interrupt inputs

The LPC2104/2105/2106 include three external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

6.18.6 Memory mapping control

The Memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.7 Power control

The LPC2104/2105/2106 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

The power can be controlled for each peripheral individually allowing peripherals to be turned off if they are not needed in the application and resulting in additional power savings.

6.18.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][6]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		–2000	+2000	V
		machine model	[12]			
		all pins		–200	+200	V

[1] The following applies to Table 8:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

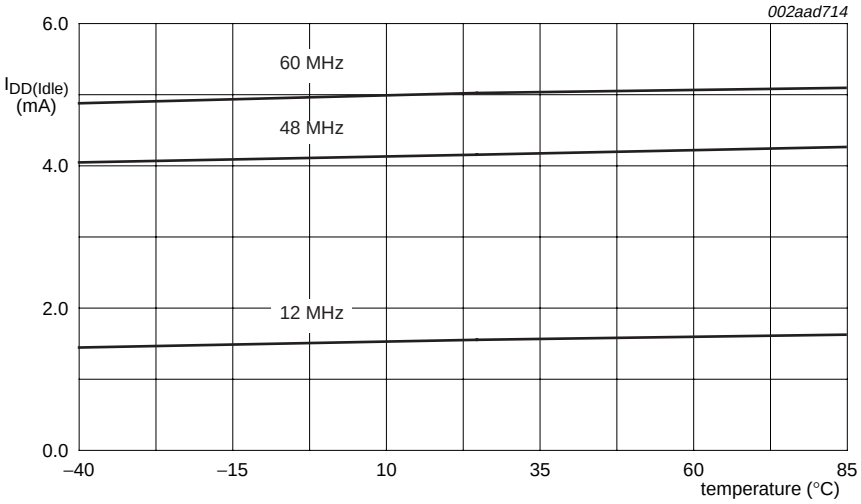
[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

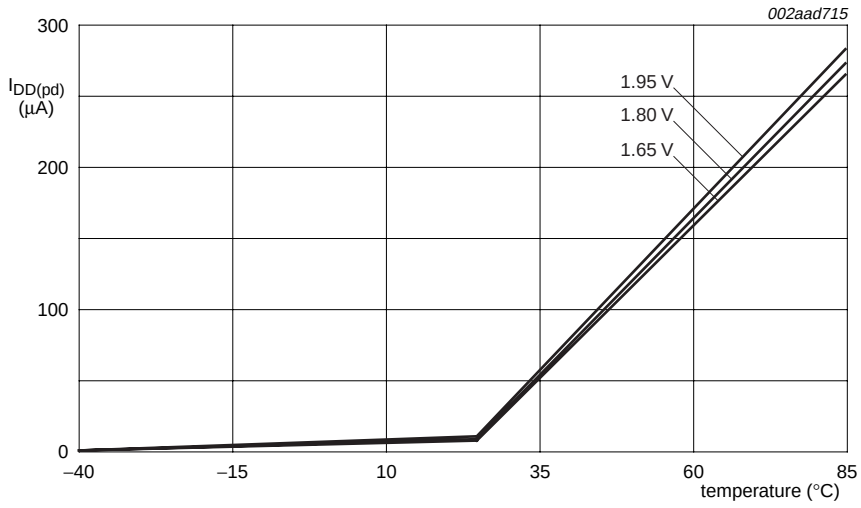
[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω series resistor.



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 10. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 11. Typical LPC2104/2105/2106/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in mA; PCLK = $^{CCLK}/_{4}$

Peripheral	CCLK = 60 MHz
Timer 0	0.258
Timer 1	0.254
UART 0	0.494
UART 1	0.561

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
…continued

Peripheral	CCLK = 60 MHz
PWM0	0.511
I^2C-bus	0.078
SPI	0.060
RTC	0.109
SSP	0.377

9.1 Timing

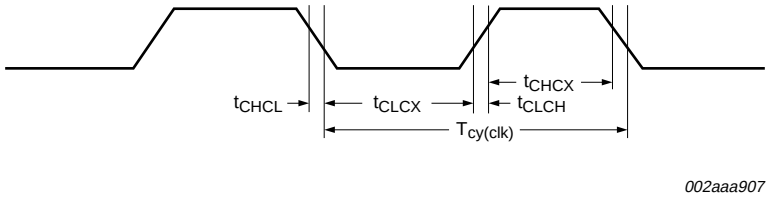
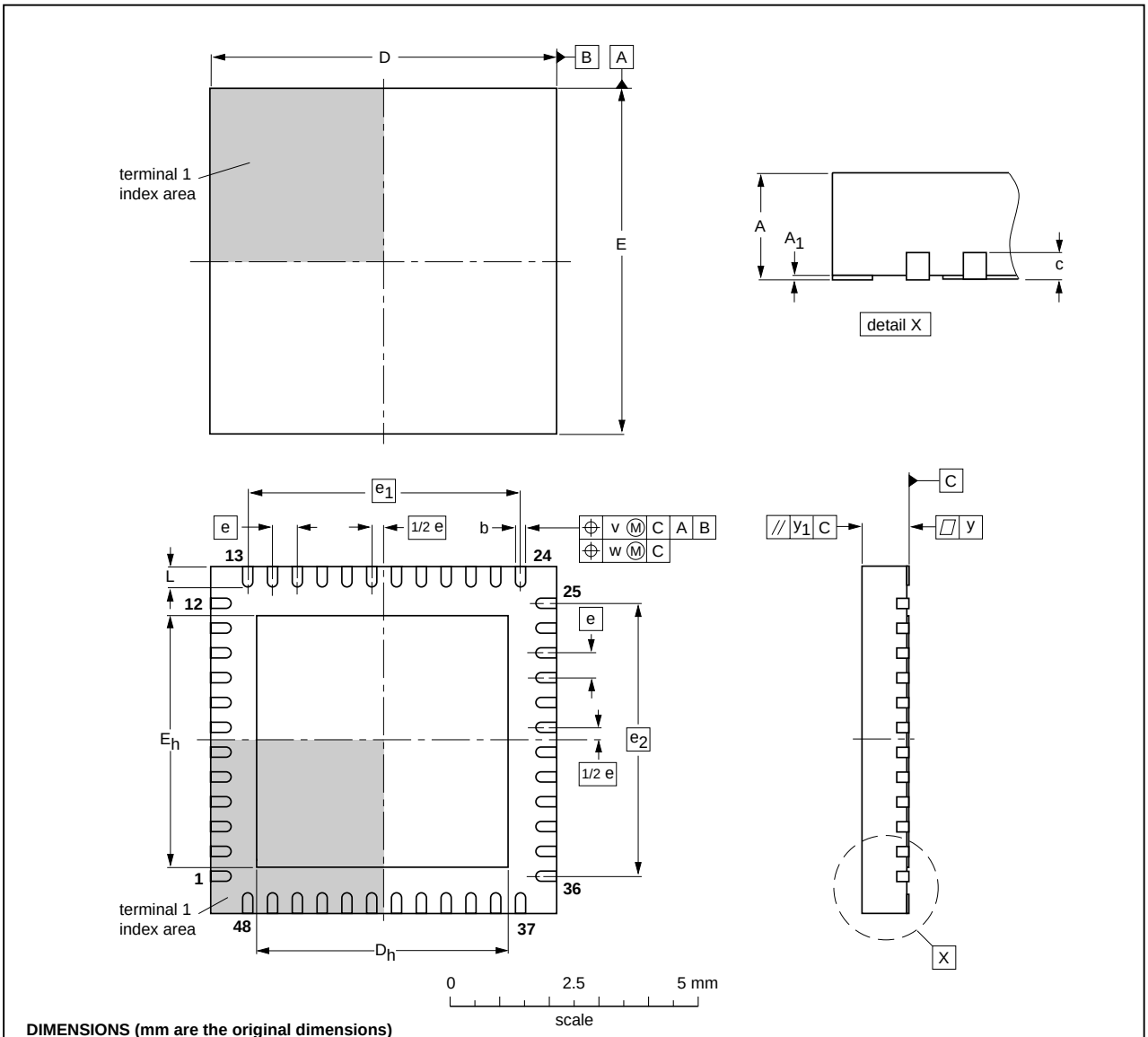


Fig 12. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.25 4.95	7.1 6.9	5.25 4.95	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 14. Package outline SOT619-1 (HVQFN48)

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2104_2105_2106_7	20080620	Product data sheet	-	LPC2104_2105_2106_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3 “Ordering information”; corrected temperature range for LPC2104FBD48/00, LPC2105FBD48/00. • Parts LPC2104FBD48/01, LPC2105FBD48/01, LPC2106BBD48, LPC2106FBD48/01, and LPC2106FHN48/01 added. • Description of /01 features added. • LPC2104/2105/2106/01 power consumption measurements added. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Figure 12 “External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)” updated. • Condition for I_{OHS} and I_{OLS} updated in Table 9 “Static characteristics”.			
LPC2104_2105_2106_6	20060725	Product data sheet	-	LPC2104_2105_2106-05
LPC2104_2105_2106-05	20041222	Product data	-	LPC2104_2105_2106-04
LPC2104_2105_2106-04	20040205	Product data	-	LPC2104_2105_2106-03
LPC2104_2105_2106-03	20031007	Product data	-	LPC2104_2105_2106-02
LPC2104_2105_2106-02	20030611	Product data	-	LPC2104_2105_2106-01
LPC2104_2105_2106-01	20030425	Product data	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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