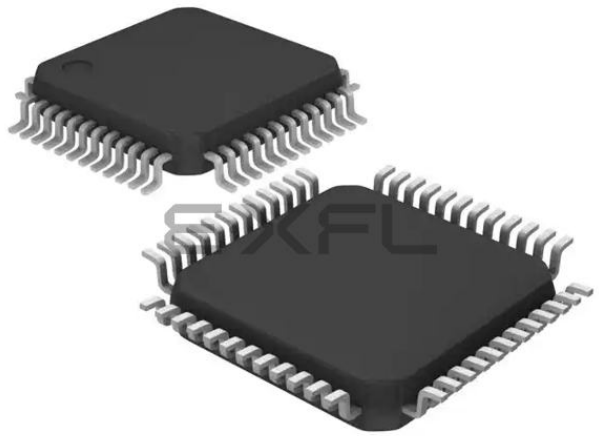

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2106fbd48-01-15

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC2106FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FHN48	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC2106FHN48/00	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC2106FHN48/01	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

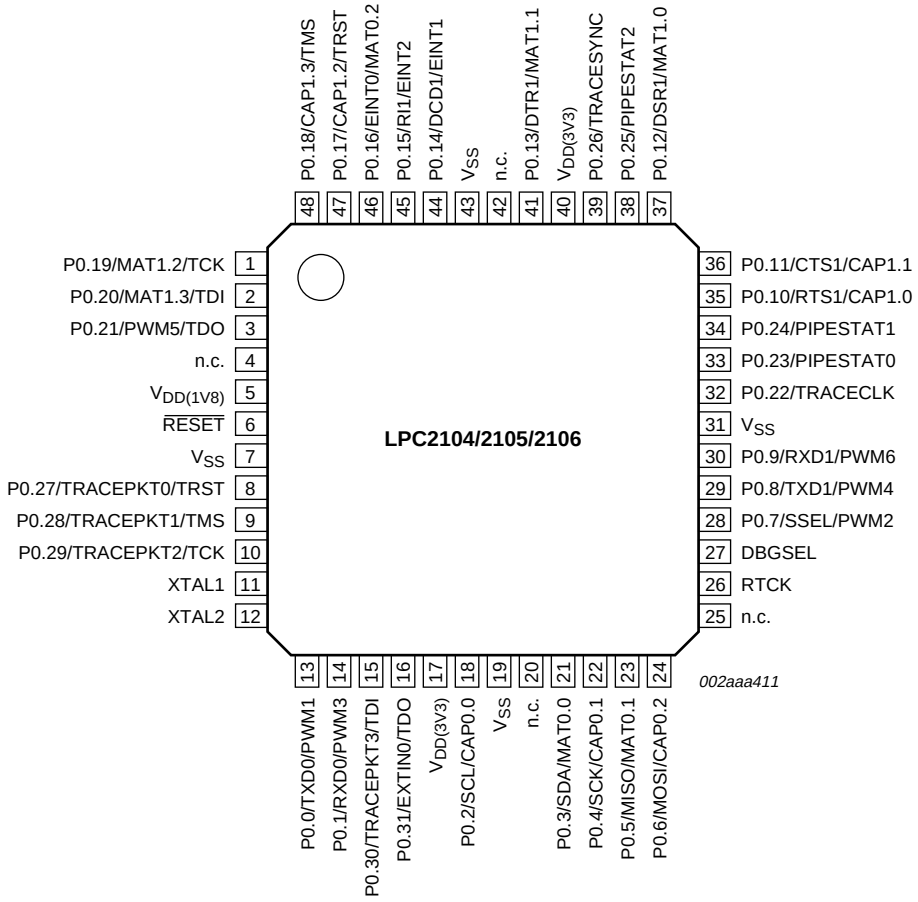
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Temperature range
LPC2104BBD48	128 kB	16 kB	0 °C to +70 °C
LPC2104FBD48/00	128 kB	16 kB	–40 °C to +85 °C
LPC2104FBD48/01	128 kB	16 kB	–40 °C to +85 °C
LPC2105BBD48	128 kB	32 kB	0 °C to +70 °C
LPC2105FBD48/00	128 kB	32 kB	–40 °C to +85 °C
LPC2105FBD48/01	128 kB	32 kB	–40 °C to +85 °C
LPC2106BBD48	128 kB	64 kB	0 °C to +70 °C
LPC2106FBD48	128 kB	64 kB	–40 °C to +85 °C
LPC2106FBD48/00	128 kB	64 kB	–40 °C to +85 °C
LPC2106FBD48/01	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48/00	128 kB	64 kB	–40 °C to +85 °C
LPC2106FHN48/01	128 kB	64 kB	–40 °C to +85 °C

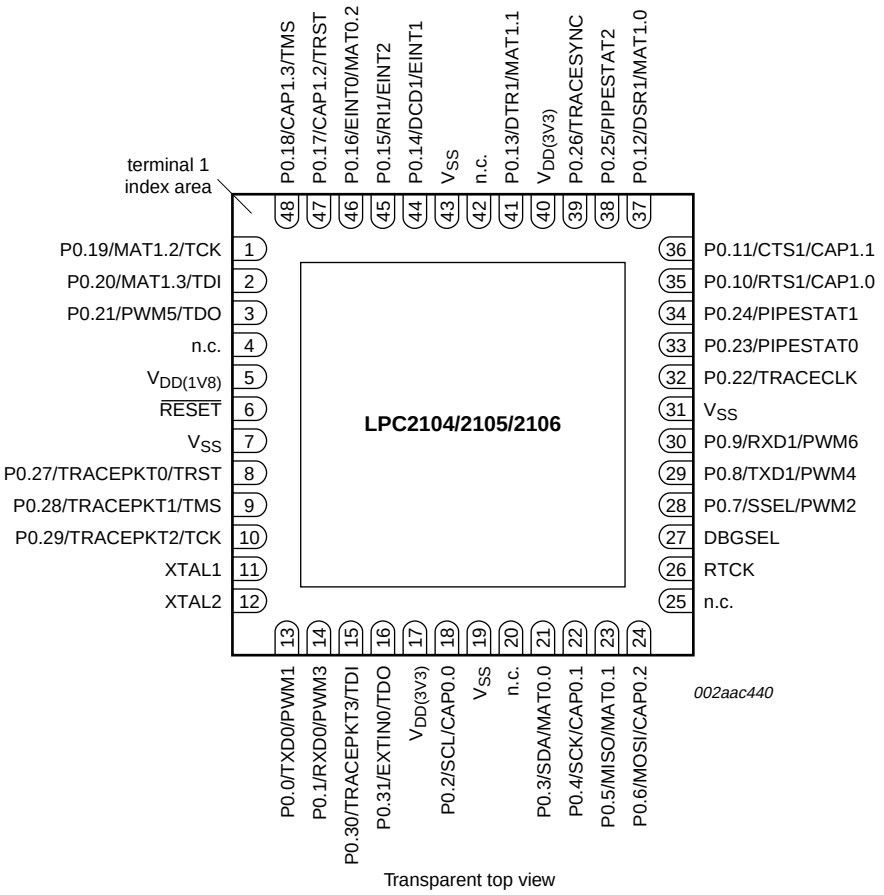
5. Pinning information

5.1 Pinning



Pin configuration is identical for all LQFP48 packages.

Fig 2. Pin configuration (LQFP48)



Pin configuration is identical for LPC2106FHN48, LPC2106FHN48/00, and LPC2106FHN48/01.

Fig 3. Pin configuration (HVQFN48)

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/CAP1.1	36[1]	I/O	**P0.11 —** Port 0 bit 11.
		I	**CTS1 —** Clear to Send input for UART 1.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
P0.12/DSR1/MAT1.0	37[1]	I/O	**P0.12 —** Port 0 bit 12.
		I	**DSR1 —** Data Set Ready input for UART 1.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
P0.13/DTR1/MAT1.1	41[1]	I/O	**P0.13 —** Port 0 bit 13.
		O	**DTR1 —** Data Terminal Ready output for UART 1.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
P0.14/DCD1/EINT1	44[1]	I/O	**P0.14 —** Port 0 bit 14.
		I	**DCD1 —** Data Carrier Detect input for UART 1.
		I	**EINT1 —** External interrupt 1 input.
P0.15/RI1/EINT2	45[1]	I/O	**P0.15 —** Port 0 bit 15.
		I	**RI1 —** Ring Indicator input for UART 1.
		O	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/MAT0.2	46[1]	I/O	**P0.16 —** Port 0 bit 16.
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.17/CAP1.2/TRST	47[1]	I/O	**P0.17 —** Port 0 bit 17.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I	**TRST —** Test Reset for JTAG interface, primary JTAG pin group.
P0.18/CAP1.3/TMS	48[1]	I/O	**P0.18 —** Port 0 bit 18.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I	**TMS —** Test Mode Select for JTAG interface, primary JTAG pin group.
P0.19/MAT1.2/TCK	1[1]	I/O	**P0.19 —** Port 0 bit 19.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I	**TCK —** Test Clock for JTAG interface, primary JTAG pin group.
P0.20/MAT1.3/TDI	2[1]	I/O	**P0.20 —** Port 0 bit 20.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**TDI —** Test Data In for JTAG interface, primary JTAG pin group.
P0.21/PWM5/TDO	3[1]	I/O	**P0.21 —** Port 0 bit 21.
		O	**PWM5 —** Pulse Width Modulator output 5.
		O	**TDO —** Test Data Out for JTAG interface, primary JTAG pin group.
P0.22/TRACECLK	32[4]	I/O	**P0.22 —** Port 0 bit 22.
		O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P0.23/PIPESTAT0	33[4]	I/O	**P0.23 —** Port 0 bit 23.
		O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P0.24/PIPESTAT1	34[4]	I/O	**P0.24 —** Port 0 bit 24.
		O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P0.25/PIPESTAT2	38[4]	I/O	**P0.25 —** Port 0 bit 25.
		O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000)

PINSEL0	Pin name	Value		Function	Value after reset
1:0	P0.0	0	0	GPIO Port 0.0	0
		0	1	TXD (UART 0)	
		1	0	PWM1	
3:2	P0.1	0	0	GPIO Port 0.1	0
		0	1	RXD (UART 0)	
		1	0	PWM3	
5:4	P0.2	0	0	GPIO Port 0.2	0
		0	1	SCL (I^2C-bus)	
		1	0	Capture 0.0 (Timer 0)	
7:6	P0.3	0	0	GPIO Port 0.3	0
		0	1	SDA (I^2C-bus)	
		1	0	Match 0.0 (Timer 0)	
9:8	P0.4	0	0	GPIO Port 0.4	0
		0	1	SCK (SPI/SSP)	
		1	0	Capture 0.1 (Timer 0)	
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI/SSP)	
		1	0	Match 0.1 (Timer 0)	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI/SSP)	
		1	0	Capture 0.2 (Timer 0)	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI/SSP)	
		1	0	PWM2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD (UART 1)	
		1	0	PWM4	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD (UART 1)	
		1	0	PWM6	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS (UART 1)	
		1	0	Capture 1.0 (Timer 1)	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS (UART 1)	
		1	0	Capture 1.1 (Timer 1)	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR (UART 1)	
		1	0	Match 1.0 (Timer 1)	

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004) *...continued*

PINSEL1	Pin name	Value		Function	Value after reset
25:24	P0.28	0	0	GPIO Port 0.28	0
		0	1	TMS	
27:26	P0.29	0	0	GPIO Port 0.29	0
		0	1	TCK	
29:28	P0.30	0	0	GPIO Port 0.30	0
		0	1	TDI	
31:30	P0.31	0	0	GPIO Port 0.31	0
		0	1	TDO	

6.9 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.9.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.9.2 Features added with the Fast GPIO set of registers available on LPC2104/2105/2106/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.10 UARTs

The LPC2104/2105/2106 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.10.1 Features

- 16 byte Receive and Transmit FIFOs
- Register locations conform to 16C550 industry standard
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in baud rate generator

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Up to four (Timer 1) and three (Timer 0) 32-bit capture channels, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four (Timer 1) and three (Timer 0) external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.14.2 Features available in LPC2104/2105/2106/01 only

The LPC2104/2105/2106/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $^{PCLK}/_{4}$. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than $^{1}/_{(2PCLK)}$.

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.

- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real time clock

The Real Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2104/2105/2106. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. It also includes four capture inputs to save the timer value when an input signal transitions, and optionally generate an interrupt when those events occur. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must “release” new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called FOSC and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. FOSC and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide

processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2104/2105/2106 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Each of these functions requires a trade-off of debugging features versus device pins. Because the LPC2104/2105/2106 are provided in a small package, there is no room for permanently assigned JTAG or Trace pins. An alternate JTAG port allows an option to debug functions assigned to the pins used by the primary JTAG port (see Section 6.8).

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace

Since the LPC2104/2105/2106 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.19.3 RealMonitor

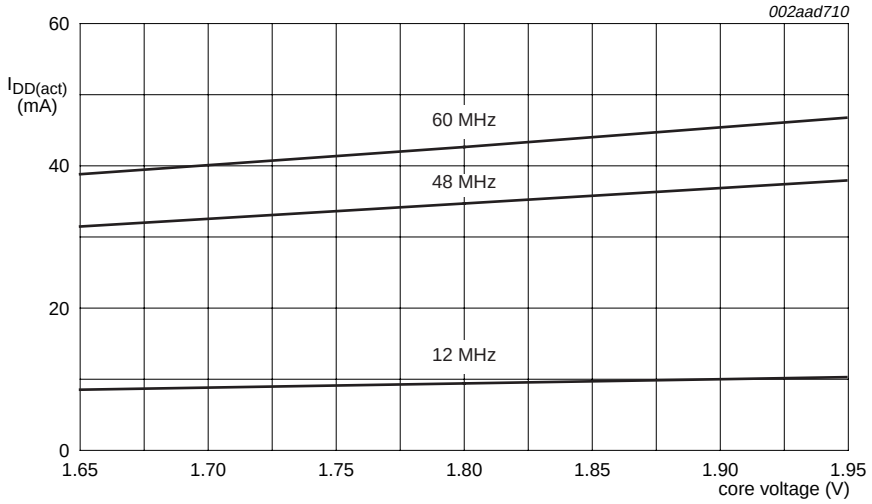
RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

8. Static characteristics

Table 9. Static characteristics

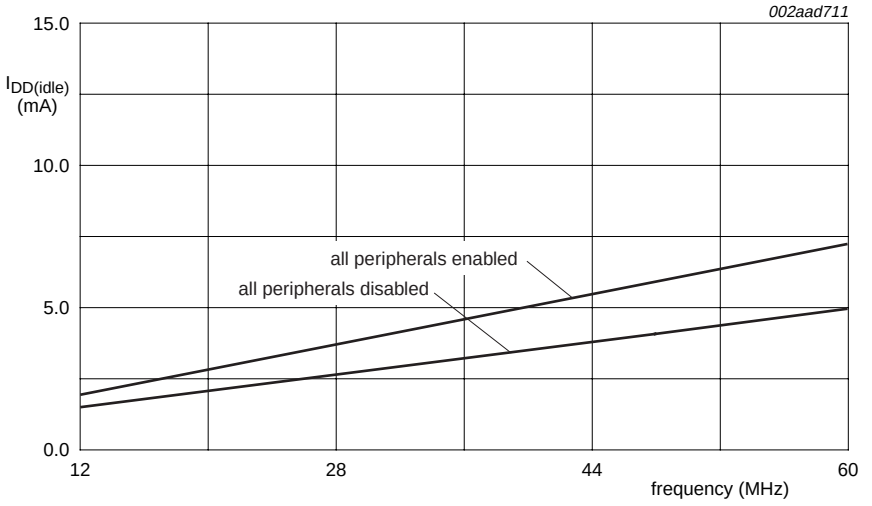
T_{amb} = 0 °C to +70 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK, and DBGSEL							
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5] [6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-state input voltage			2.0	-	-	V
V_{IL}	LOW-state input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-state output voltage	I_{OH} = –4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	–4	-	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V	[8]	-	-	–45	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V; applies to DBGSEL	[9]	20	50	100	µA
LPC2104/2105/2106 and LPC2104/2105/2106/00							
I_{pu}	pull-up current	V_I = 0 V	[10]	–25	–50	–65	µA
		$V_{DD(3V3)} < V_I < 5$ V	[9][10]	0	0	0	µA
LPC2104/2105/2106/01							
I_{pu}	pull-up current	V_I = 0 V	[10]	–15	–50	–85	µA
		$V_{DD(3V3)} < V_I < 5$ V	[9][10]	0	0	0	µA



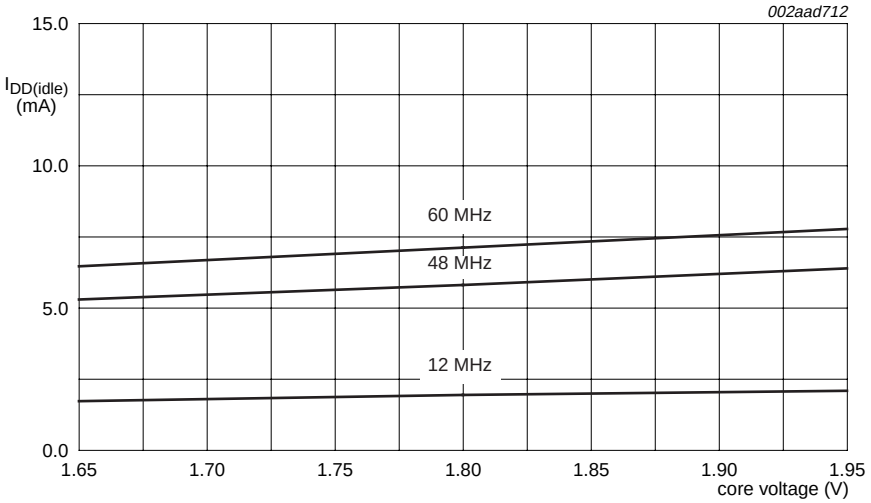
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled.

Fig 6. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different core voltages



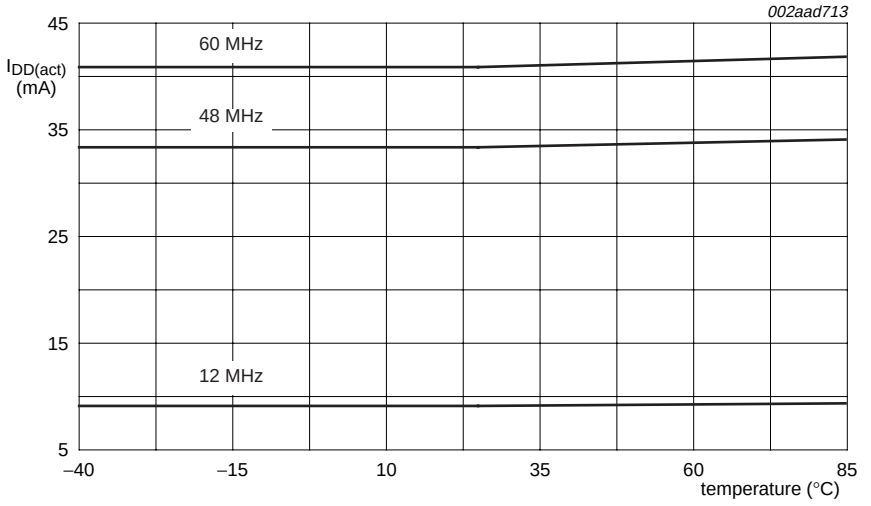
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

Fig 7. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different frequencies



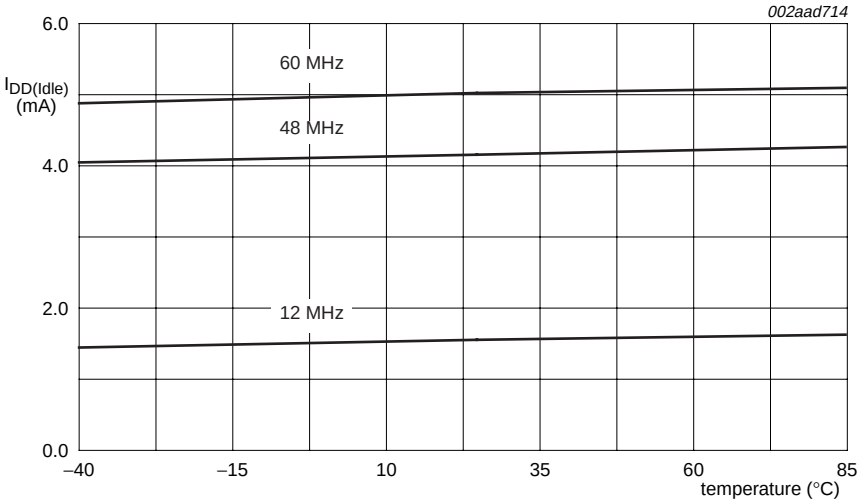
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled.

Fig 8. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different core voltages



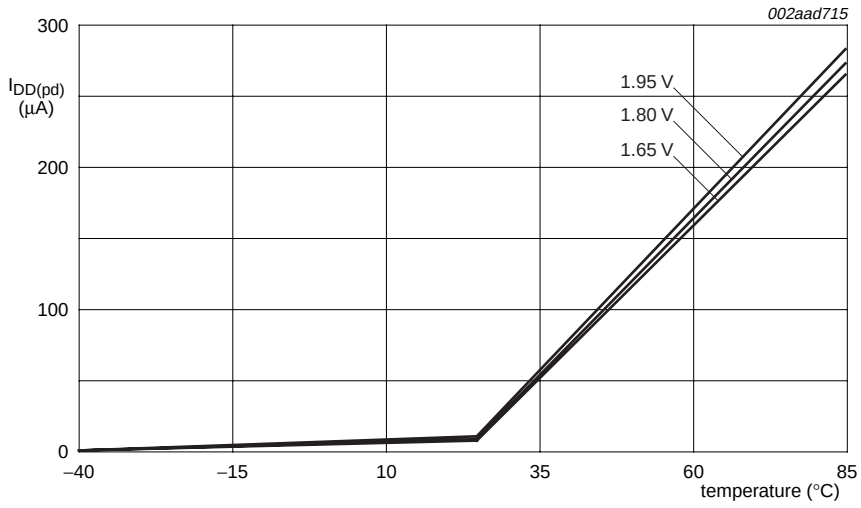
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 9. Typical LPC2104/2105/2106/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 10. Typical LPC2104/2105/2106/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 11. Typical LPC2104/2105/2106/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in mA; PCLK = $^{CCLK}/_{4}$

Peripheral	CCLK = 60 MHz
Timer 0	0.258
Timer 1	0.254
UART 0	0.494
UART 1	0.561

9. Dynamic characteristics

Table 11. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2104_2105_2106_7	20080620	Product data sheet	-	LPC2104_2105_2106_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3 “Ordering information”; corrected temperature range for LPC2104FBD48/00, LPC2105FBD48/00. • Parts LPC2104FBD48/01, LPC2105FBD48/01, LPC2106BBD48, LPC2106FBD48/01, and LPC2106FHN48/01 added. • Description of /01 features added. • LPC2104/2105/2106/01 power consumption measurements added. • Maximum frequency f_{osc} for external oscillator and external crystal updated. • Figure 12 “External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)” updated. • Condition for I_{OHS} and I_{OLS} updated in Table 9 “Static characteristics”.			
LPC2104_2105_2106_6	20060725	Product data sheet	-	LPC2104_2105_2106-05
LPC2104_2105_2106-05	20041222	Product data	-	LPC2104_2105_2106-04
LPC2104_2105_2106-04	20040205	Product data	-	LPC2104_2105_2106-03
LPC2104_2105_2106-03	20031007	Product data	-	LPC2104_2105_2106-02
LPC2104_2105_2106-02	20030611	Product data	-	LPC2104_2105_2106-01
LPC2104_2105_2106-01	20030425	Product data	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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