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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2106fhn48-551

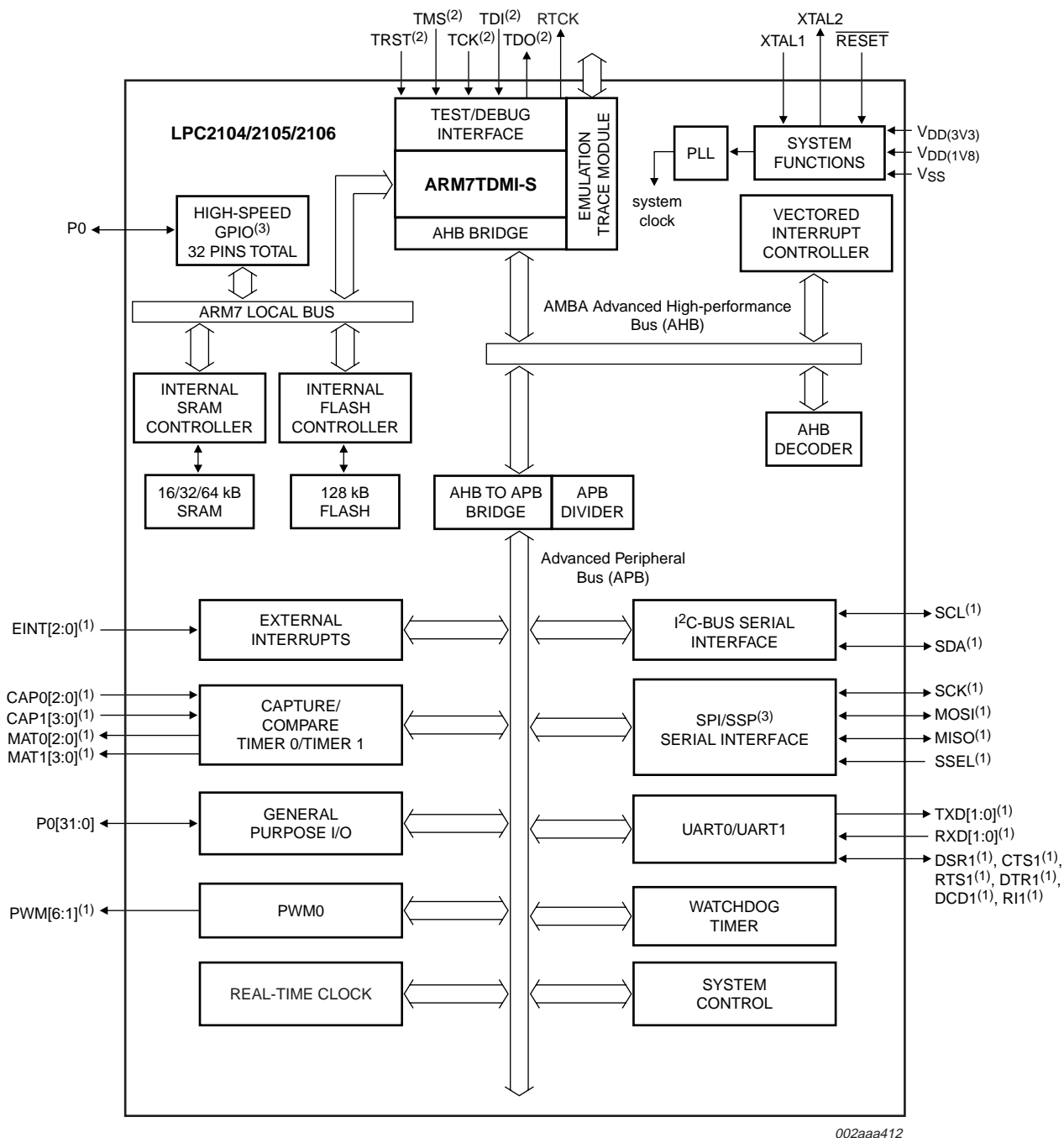
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute whilst the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell enables non-intrusive high speed real-time tracing of instruction execution.
- Multiple serial interfaces including two UARTs (16C550), Fast I²C-bus (400 kbit/s), and SPI.
- Two 32-bit timers (7 capture/compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Up to thirty-two 5 V tolerant general purpose I/O pins in a tiny LQFP48 (7 mm × 7 mm) package.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
 - ◆ CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 8.3 %).
 - ◆ I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2104BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2104FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2104FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105FBD48/00	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2105FBD48/01	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106BBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2106FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

4. Block diagram



(1) Shared with GPIO.

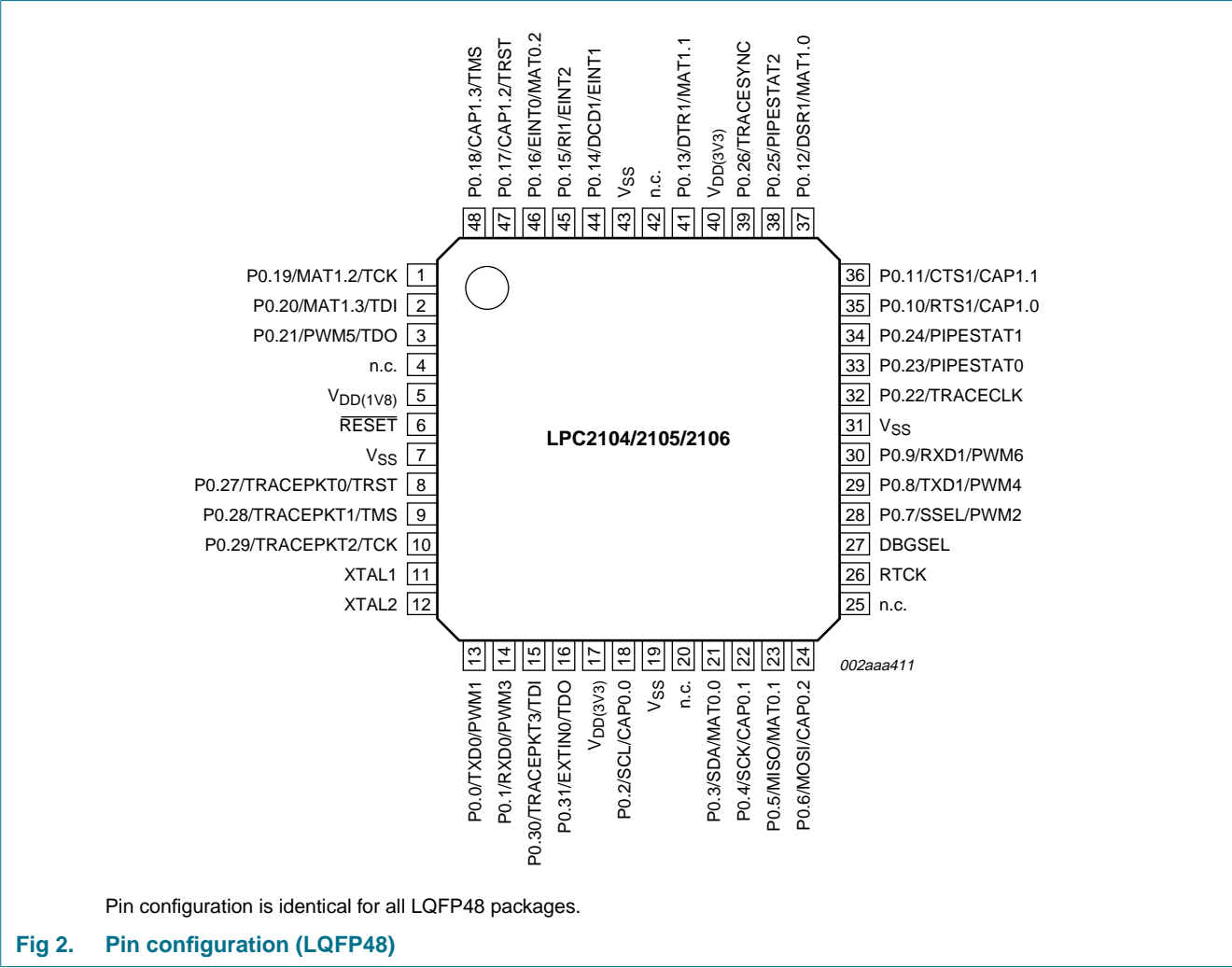
(2) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(3) Available on LPC2104/2105/2106/01 only.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	Port 0: Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.
P0.0/TXD0/PWM1	13 ^[1]	I/O	P0.0 — Port 0 bit 0.
		O	TXD0 — Transmitter output for UART 0.
		O	PWM1 — Pulse Width Modulator output 1.
P0.1/RXD0/PWM3	14 ^[1]	I/O	P0.1 — Port 0 bit 1.
		I	RXD0 — Receiver input for UART 0.
		O	PWM3 — Pulse Width Modulator output 3.
P0.2/SCL/CAP0.0	18 ^[2]	I/O	P0.2 — Port 0 bit 2. The output is open-drain.
		I/O	SCL — I ² C-bus clock input/output. Open-drain output (for I ² C-bus compliance).
		I	CAP0.0 — Capture input for Timer 0, channel 0.
P0.3/SDA/MAT0.0	21 ^[2]	I/O	P0.3 — Port 0 bit 3. The output is open-drain.
		I/O	SDA — I ² C-bus data input/output. Open-drain output (for I ² C-bus compliance).
		O	MAT0.0 — Match output for Timer 0, channel 0. The output is open-drain.
P0.4/SCK/CAP0.1	22 ^[1]	I/O	P0.4 — Port 0 bit 4.
		I/O	SCK — Serial clock for SPI/SSP ^[3] . Clock output from master or input to slave.
		I	CAP0.1 — Capture input for Timer 0, channel 1.
P0.5/MISO/MAT0.1	23 ^[1]	I/O	P0.5 — Port 0 bit 5.
		I/O	MISO — Master In Slave Out for SPI/SSP ^[3] . Data input to SPI/SSP master or data output from SPI/SSP slave.
		O	MAT0.1 — Match output for Timer 0, channel 1.
P0.6/MOSI/CAP0.2	24 ^[1]	I/O	P0.6 — Port 0 bit 6.
		I/O	MOSI — Master Out Slave In for SPI/SSP ^[3] . Data output from SPI/SSP master or data input to SPI/SSP slave.
		I	CAP0.2 — Capture input for Timer 0, channel 2.
P0.7/SSEL/PWM2	28 ^[1]	I/O	P0.7 — Port 0 bit 7.
		I	SSEL — Slave Select for SPI/SSP ^[3] . Selects the SPI/SSP interface as a slave.
		O	PWM2 — Pulse Width Modulator output 2.
P0.8/TXD1/PWM4	29 ^[1]	I/O	P0.8 — Port 0 bit 8.
		O	TXD1 — Transmitter output for UART 1.
		O	PWM4 — Pulse Width Modulator output 4.
P0.9/RXD1/PWM6	30 ^[1]	I/O	P0.9 — Port 0 bit 9.
		I	RXD1 — Receiver input for UART 1.
		O	PWM6 — Pulse Width Modulator output 6.
P0.10/RTS1/CAP1.0	35 ^[1]	I/O	P0.10 — Port 0 bit 10.
		O	RTS1 — Request to Send output for UART 1.
		I	CAP1.0 — Capture input for Timer 1, channel 0.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2104/2105/2106 incorporate a 128 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120 kB of flash memory is available for user code.

The LPC2104/2105/2106 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

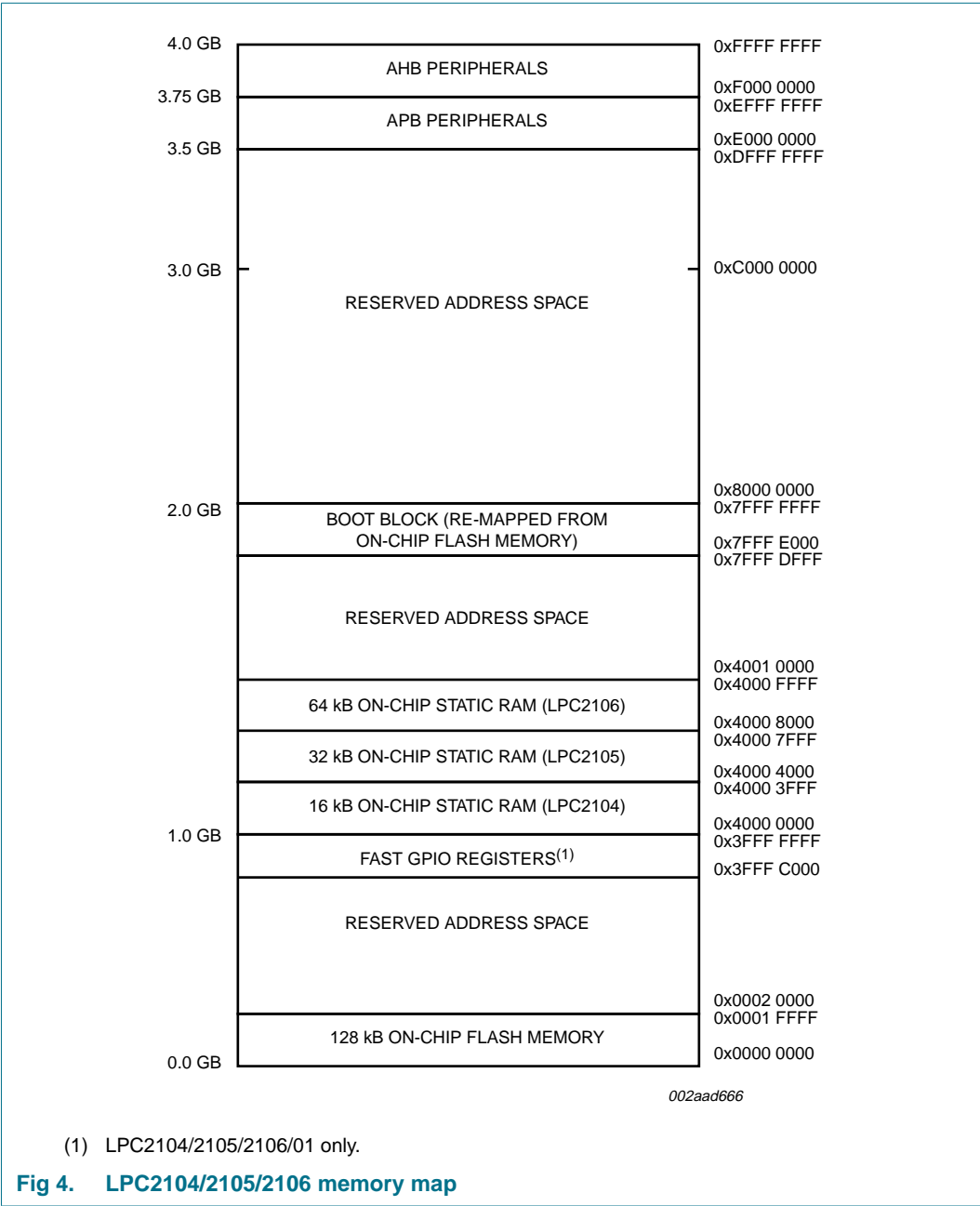
6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2104/2105/2106 provide 16/32/64 kB of static RAM, respectively.

6.4 Memory map

The LPC2104/2105/2106 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in [Section 6.18 “System control”](#).



6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the Interrupt Request (IRQ) inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

[Table 4](#) lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 2 (CR0, CR1, CR2)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART 0	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) Auto-Baud Time-Out (ABTO) ^[1] End of Auto-Baud (ABEO) ^[1]	6

Table 4. Interrupt sources ...continued

Block	Flag(s)	VIC channel #
UART 1	Rx Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	Rx Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI)	
	Auto-Baud Time-Out (ABTO) ^[1]	
	End of Auto-Baud (ABEO) ^[1]	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I ² C-bus	SI (state change)	9
SPI and SSP ^[1]	SPIF, MODF (SPI)	10
	TXRIS, RXRIS, RTRIS, RORRIS (SSP) ^[1]	
-	reserved	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
System Control	External Interrupt 1 (EINT1)	15
System Control	External Interrupt 2 (EINT2)	16

[1] Available on LPC2104/2105/2106/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module contains two registers as shown in [Table 5](#).

Table 5. Pin control module registers

Address	Name	Description	Access
0xE002 C000	PINSEL0	Pin function select register 0	Read/Write
0xE002 C004	PINSEL1	Pin function select register 1	Read/Write

6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in [Table 6](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in [Table 6](#) are reserved, and should not be used

Table 6. Pin function select register 0 (PINSEL0 - 0xE002 C000) ...continued

PINSEL0	Pin name	Value		Function	Value after reset
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR (UART 1)	
		1	0	Match 1.1 (Timer 1)	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD (UART 1)	
		1	0	EINT1	
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI (UART 1)	
		1	0	EINT2	

6.8 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in [Table 7](#). The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically.

Remark: The primary JTAG port and the trace port can be selected only through the DBGSEL pin at reset (Debug mode). Function control for the pins P0[31:17] is effective only when the DBGSEL input is pulled LOW during reset.

Table 7. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
13:12	P0.22	0	0	GPIO Port 0.22	0
15:14	P0.23	0	0	GPIO Port 0.23	0
17:16	P0.24	0	0	GPIO Port 0.24	0
19:18	P0.25	0	0	GPIO Port 0.25	0
21:20	P0.26	0	0	GPIO Port 0.26	0
23:22	P0.27	0	0	GPIO Port 0.27	0
		0	1	TRST	

by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2104/2105/2106: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Code security (Code Read Protection - CRP)

This feature of the LPC2104/2105/2106/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection:

1. CRP1 disables access to the chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) a flash update mechanism using IAP calls or a call to reinvoke ISP command to enable flash update via UART 0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

6.18.5 External interrupt inputs

The LPC2104/2105/2106 include three external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

6.18.6 Memory mapping control

The Memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.7 Power control

The LPC2104/2105/2106 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

The power can be controlled for each peripheral individually allowing peripherals to be turned off if they are not needed in the application and resulting in additional power savings.

6.18.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the

processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2104/2105/2106 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Each of these functions requires a trade-off of debugging features versus device pins. Because the LPC2104/2105/2106 are provided in a small package, there is no room for permanently assigned JTAG or Trace pins. An alternate JTAG port allows an option to debug functions assigned to the pins used by the primary JTAG port (see [Section 6.8](#)).

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace

Since the LPC2104/2105/2106 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2104/2105/2106 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD(1V8)}	supply voltage (1.8 V)		[2] -0.5	+2.5	V
V _{DD(3V3)}	supply voltage (3.3 V)		[3] -0.5	+3.6	V
V _I	input voltage	5 V tolerant I/O pins	[4][5] -0.5	+6.0	V
		other I/O pins	[4][6] -0.5	V _{DD(3V3)} + 0.5	V
I _{DD}	supply current		[7][8] -	100	mA
I _{SS}	ground current		[8][9] -	100	mA
T _{stg}	storage temperature		[10] -65	+150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V _{esd}	electrostatic discharge voltage	human body model	[11]		
		all pins	-2000	+2000	V
		machine model	[12]		
		all pins	-200	+200	V

[1] The following applies to [Table 8](#):

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the V_{DD(3V3)} supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

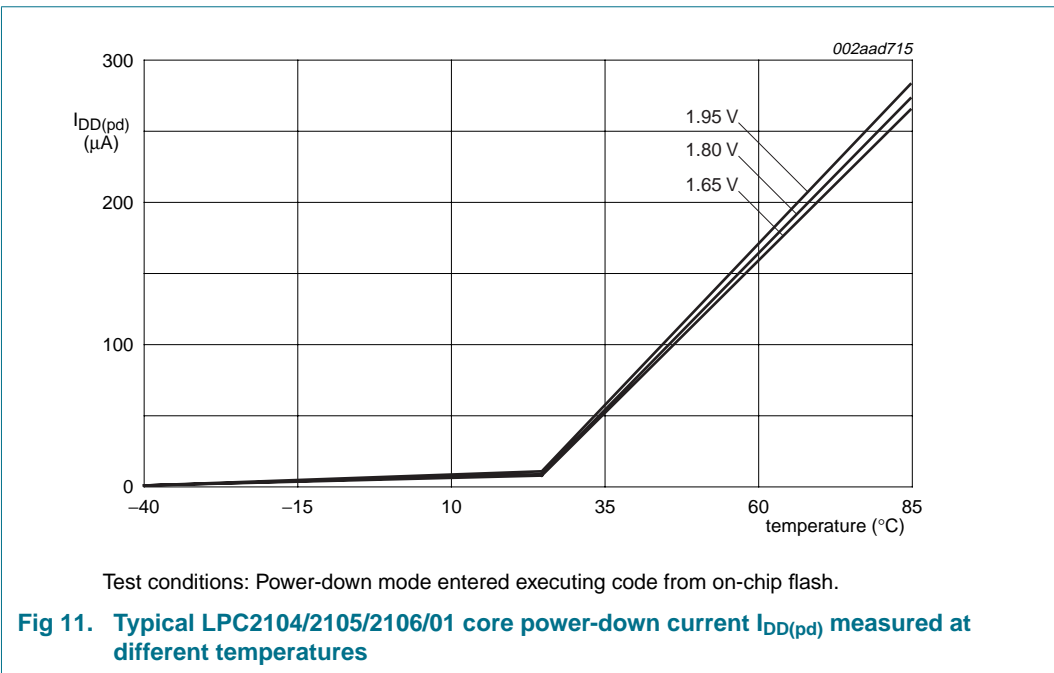
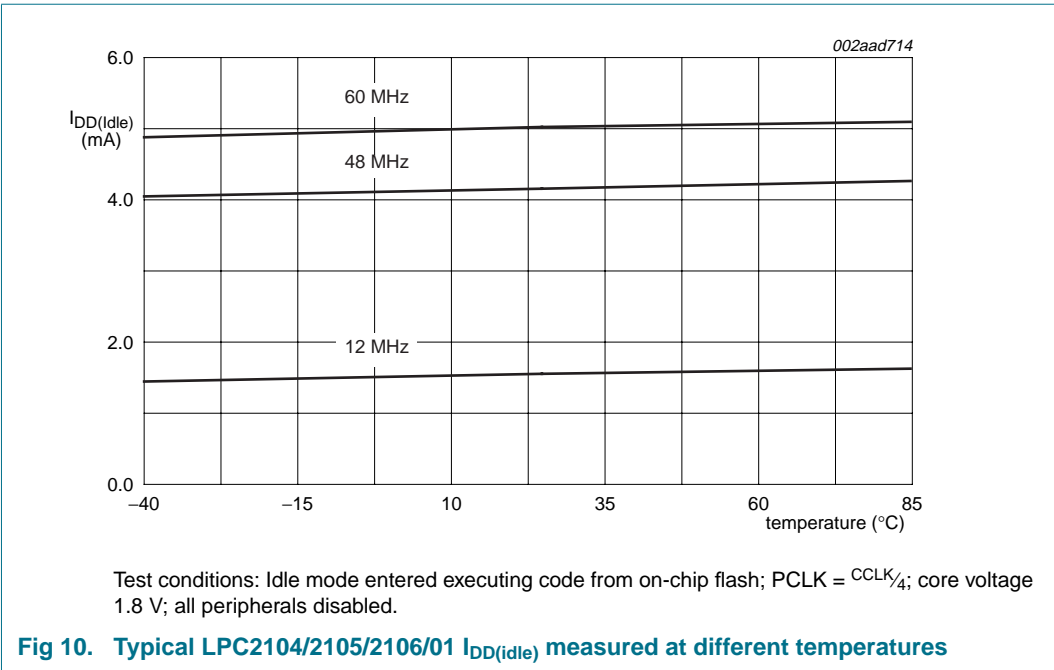


Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
Core voltage 1.8 V; $T_{amb} = 25\text{ °C}$; all measurements in mA; PCLK = CCLK/4

Peripheral	CCLK = 60 MHz
Timer 0	0.258
Timer 1	0.254
UART 0	0.494
UART 1	0.561

Table 10. Typical LPC2104/2105/2106/01 peripheral power consumption in Idle mode
...continued

Peripheral	CCLK = 60 MHz
PWM0	0.511
I ² C-bus	0.078
SPI	0.060
RTC	0.109
SSP	0.377

9. Dynamic characteristics

Table 11. Dynamic characteristics

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ for commercial applications, $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I²C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL}	^[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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