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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9301-cqzr

OVERVIEW

The EP9301 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Industrial controls
- Digital media servers
- Integrated home media gateways
- Digital audio jukeboxes
- Streaming audio players
- Set-top boxes
- Point-of-sale terminals
- Thin clients
- Biometric security systems
- GPS & fleet management systems
- Educational toys
- Industrial computers
- Industrial hand-held devices
- Voting machines
- Medical equipment

The EP9301 is one of a series of ARM920T-based devices. Other members of the family have different peripheral sets, a coprocessor, and different package configurations.

The ARM920T microprocessor core has a separate 16-kbyte, 64-way set-associative instruction and data caches.

The MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100 Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, AC'97 and I^2S audio. A two-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second), two UARTs, and a analog voltage measurement analog-to-digital converter (ADC) are included as well.

The EP9301 is a high-performance, low-power RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 166 MHz. The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 675 mW.

Table A. Change History

Revision	Date	Changes
1	October 2003	Initial Release.
2	February 2004	Update timing specifications.
3	July 2004	Update AC data.
4	July 2004	Add ADC data.
5	March 2005	Update with most-current characterization data.
F1	February 2010	Removed "Preliminary Data" statement from legal disclaimer. Removed lead-containing device part numbers. Increased minimum CVDD & VDD_PLL voltages from 1.65 V min. to 1.71 V min. Changed operating temperatures to 0 to 60°C commercial, -40 to 70°C industrial.
F2	March 2010	Increased commercial/industrial temperatures to 70/85 deg. C max.

Ethernet Media Access Controller (MAC)

The MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported. Features include:

- Supports 1/10/100 Mbps transfer rates for home / small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

Table C. Ethernet Media Access Controller Pin Assignments

Pin Mnemonic	Pin Description
MDC	Management Data Clock
MDIO	Management Data I/O
RXCLK	Receive Clock
MIIRXD[3:0]	Receive Data
RXDVAL	Receive Data Valid
RXERR	Receive Data Error
TXCLK	Transmit Clock
MIITXD[3:0]	Transmit Data
TXEN	Transmit Enable
TXERR	Transmit Error
CRS	Carrier Sense
CLD	Collision Detect

Serial Interfaces (SPI, I^{2}S, and AC ’97)

The Serial Peripheral Interface (SPI) port can be configured as a master or a slave, supporting the National Semiconductor®, Motorola®, and Texas Instruments® signaling protocols.

The AC'97 port supports multiple codecs for multichannel audio output with a single stereo input. The I^{2}S port supports stereo 24-bit audio.

These ports are multiplexed so that the I^{2}S port will take over either the AC'97 pins or the SPI pins.

- Normal Mode: One SPI Port and one AC’97 Port
- I^{2}S on SSP Mode: One AC’97 Port and one I^{2}S Port
- I^{2}S on AC’97 Mode: One SPI Port and one I^{2}S Port

Note: I^{2}S may not be output on AC’97 and SSP ports at the same time.

Table D. Audio Interfaces Pin Assignment

Pin Name	Normal Mode	I^{2}S on SSP Mode	I^{2}S on AC'97 Mode
	Pin Description	Pin Description	Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

12-bit Analog-to-digital Converter (ADC)

The ADC block consists of a 12-bit analog-to-digital converter with a analog input multiplexer. The multiplexer can select to measure battery voltage and other miscellaneous voltages on the external measurement pins. Features include:

- 5 external pins for ADC measurement
- Measurement pin input range: 0 to 3.3 V.
- ADC-conversion-complete interrupt signal

Table E. 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
ADC[0] (Ym, pin 135)	External Analog Measurement Input
ADC[1] (sXp, pin 134)	External Analog Measurement Input
ADC[2] (sXm, pin 133)	External Analog Measurement Input
ADC[3] (sYp, pin 132)	External Analog Measurement Input
ADC[4] (sYm, pin 131)	External Analog Measurement Input

Universal Asynchronous Receiver/Transmitters (UARTs)

Two 16550-compatible UARTs are supplied. One provides asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. The second UART provides IrDA® compatibility.

- UART1 supports modem bit rates up to 115.2 kbps, supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.

Table F. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn / DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0] / RI	UART1 Ring Indicator
TXD1 / SIROUT	UART2 Transmit / IrDA Output
RXD1 / SIRIN	UART2 Receive / IrDA Input

Dual Port USB Host

The USB Open Host Controller Interface (Open HCI) provides full speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered-start” topology.

This includes the following feature:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 2 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table G. Dual Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2,0]	USB Positive signals
USBm[2,0]	USB Negative Signals

Note: USBm[1] and USBp[1] are not bonded out.

Two-Wire Interface With EEPROM Support

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table H. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ± 1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9301device will not boot.

Table I. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 166 MHz.

Table N. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table O. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Internal Boot ROM

The Internal 16 kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Manual for operational details.

DC Characteristics

(T_A = 0 to 70° C; CVDD = VDD_PLL = 1.8; RVDD = 3.3 V;
All grounds = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	Iout = -4 mA	(Note 3)	V_{oh}	0.85 × RVDD	-	V
Low level output voltage	Iout = 4 mA		V_{ol}	-	0.15 × RVDD	V
High level input voltage		(Note 4)	V_{ih}	0.65 × RVDD	VDD + 0.3	V
Low level input voltage		(Note 4)	V_{il}	–0.3	0.35 × RVDD	V
High level leakage current	Vin = 3.3 V	(Note 4)	I_{ih}	-	10	µA
Low level leakage current	Vin = 0	(Note 4)	I_{il}	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded), 25° C					
Power Supply Current:	CVDD / VDD_PLL Total RVDD	- -	180 45	230 80	mA mA
Low-Power Mode Supply Current	CVDD / VDD_PLL Total RVDD	- -	2 1.0	3.5 2	mA mA

Note: 3. For open drain pins, high level output voltage is dependent on the external load.
4. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See Table Q on page 38). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

SDRAM Burst Read Cycle

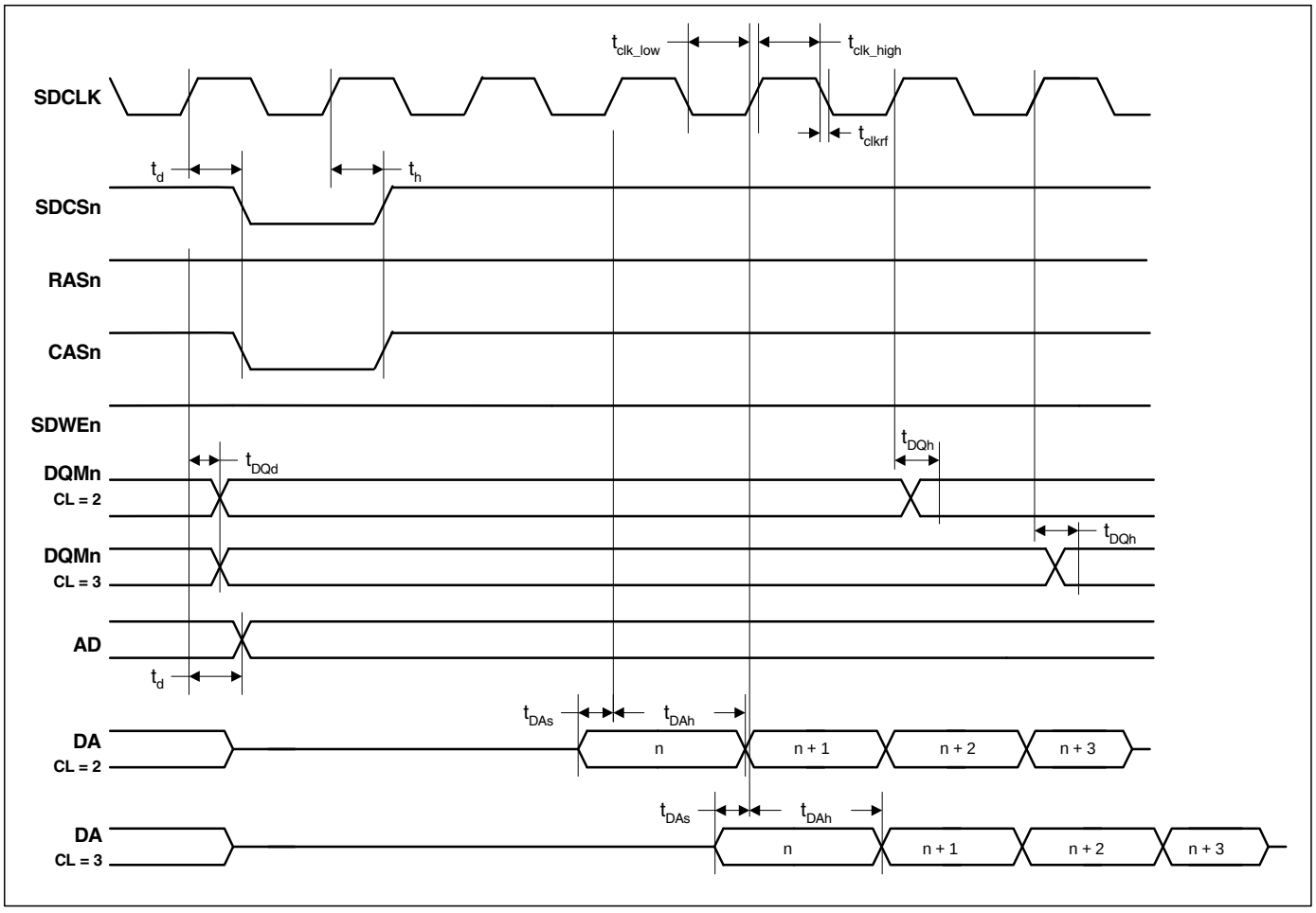


Figure 3. SDRAM Burst Read Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

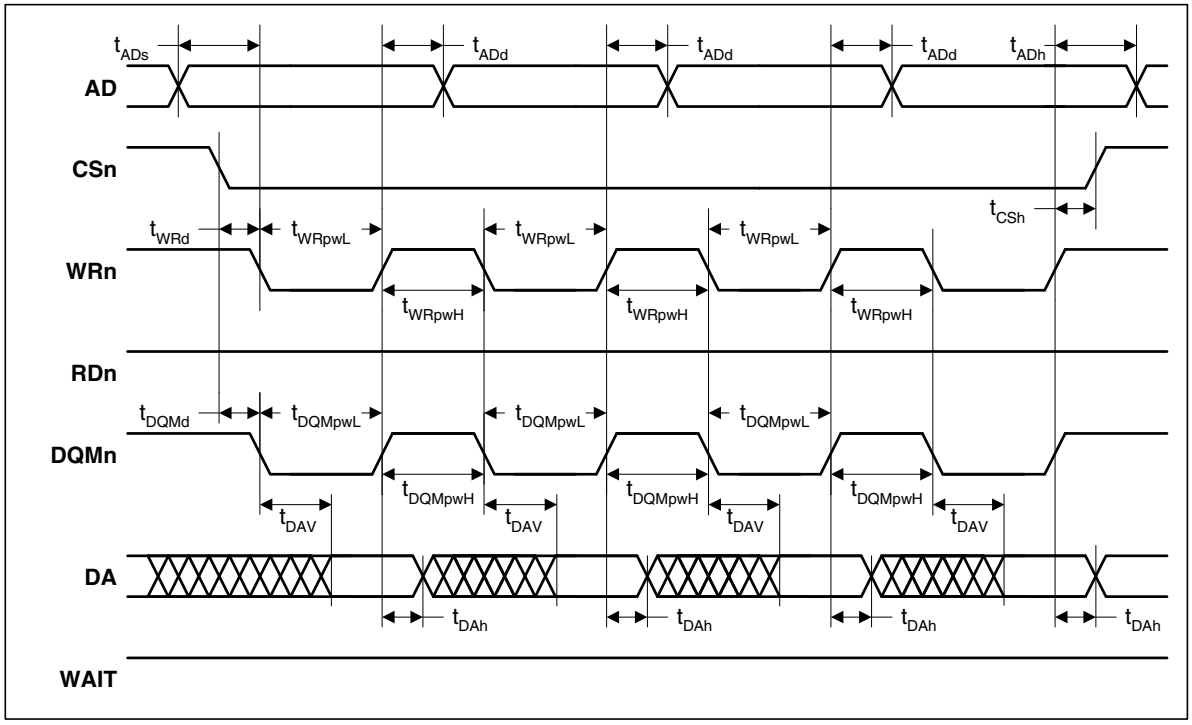


Figure 7. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory 32-bit Read on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to AD transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd2}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times ((2 \times WST1) + 3)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA to RDn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

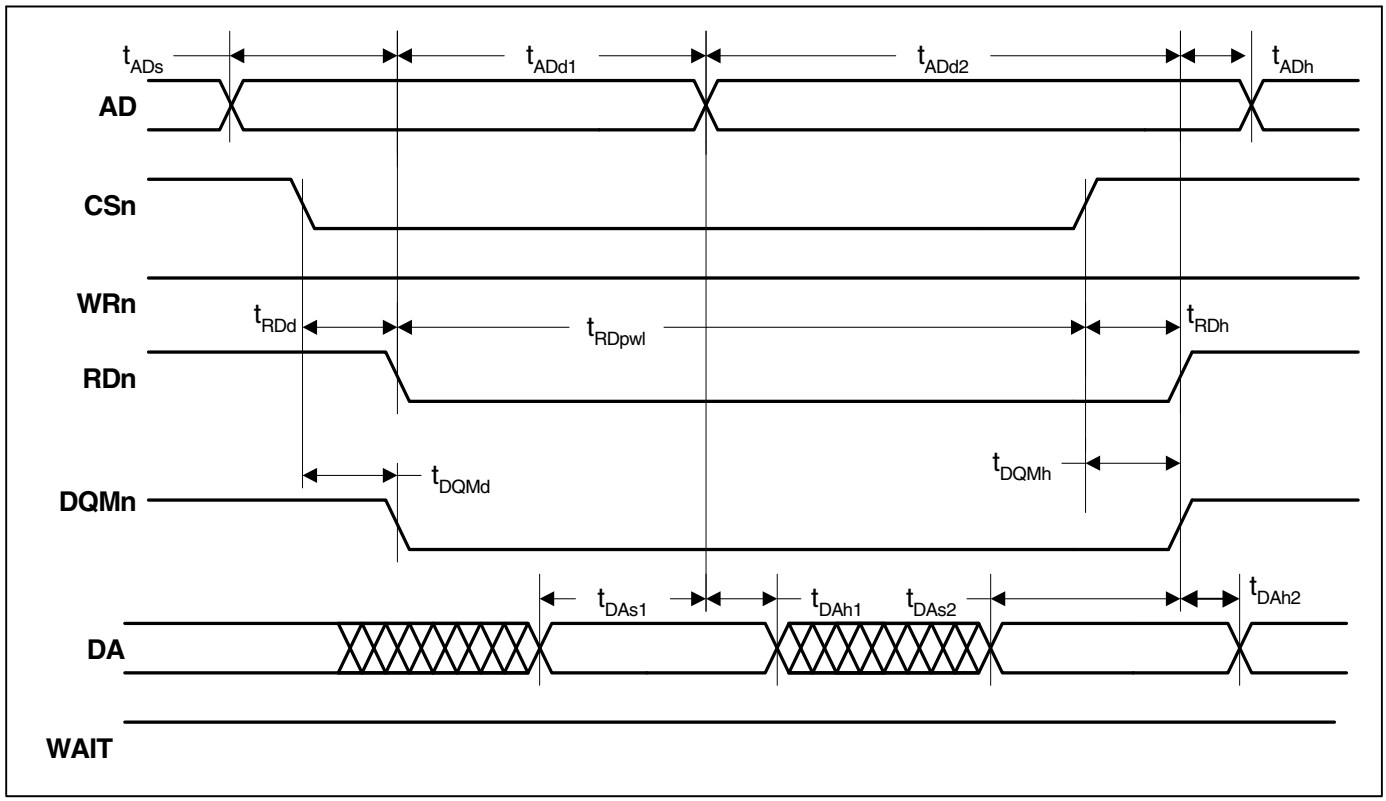


Figure 8. Static Memory Multiple Word Read 16-bit Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

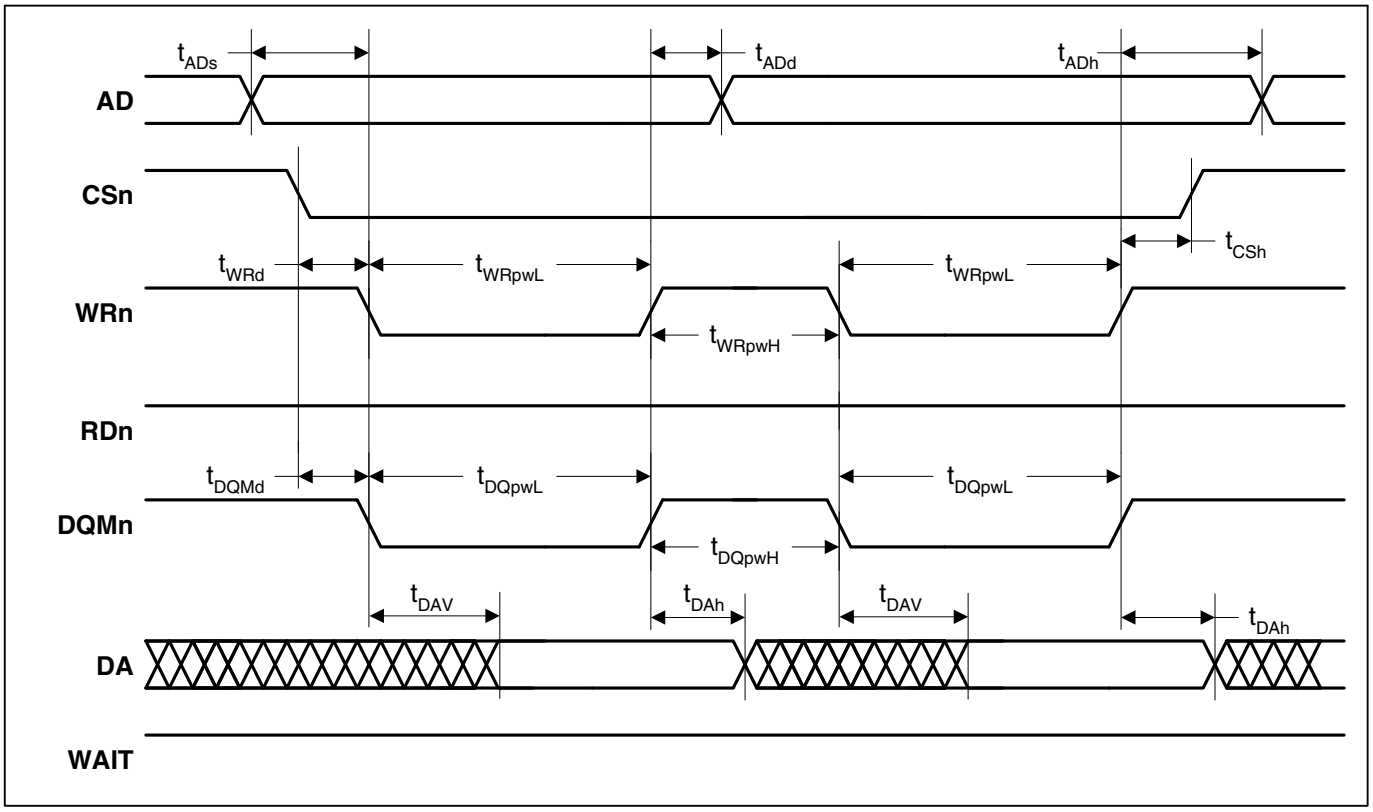


Figure 9. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

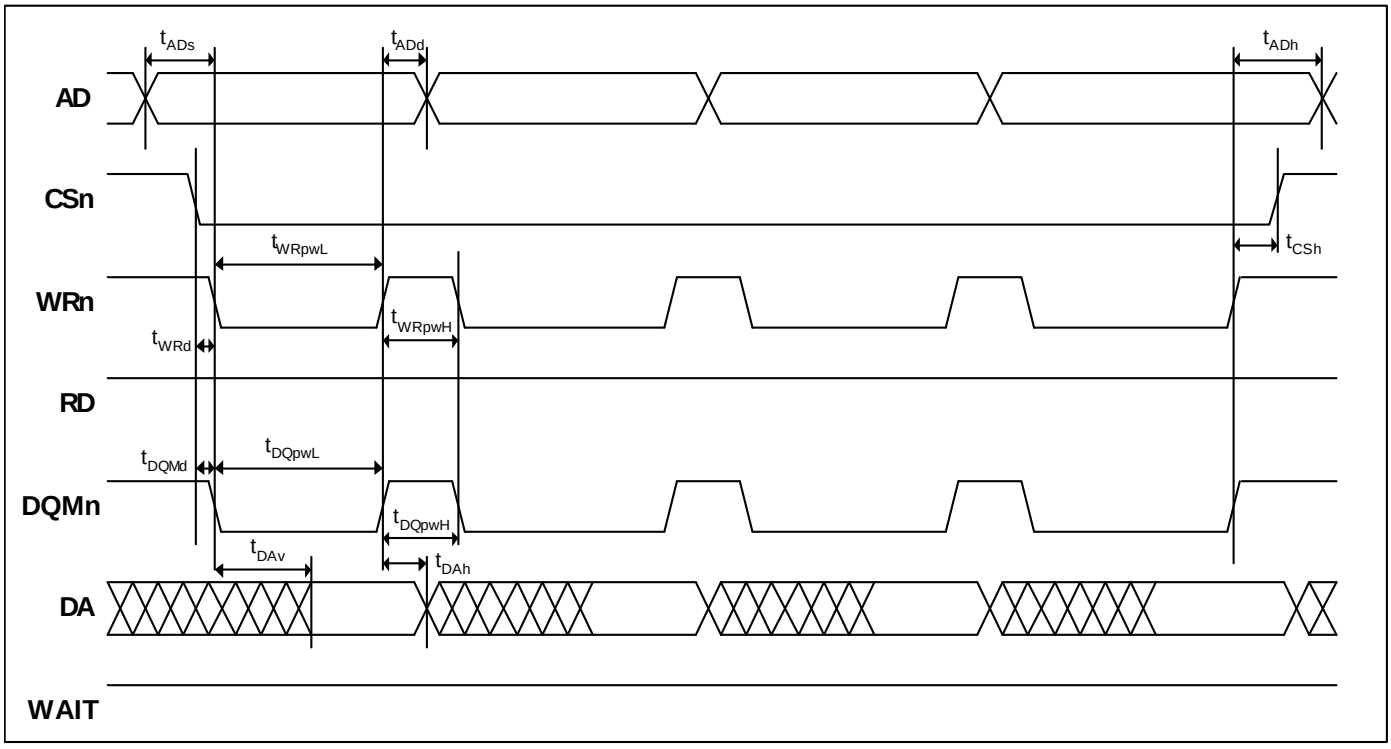


Figure 11. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

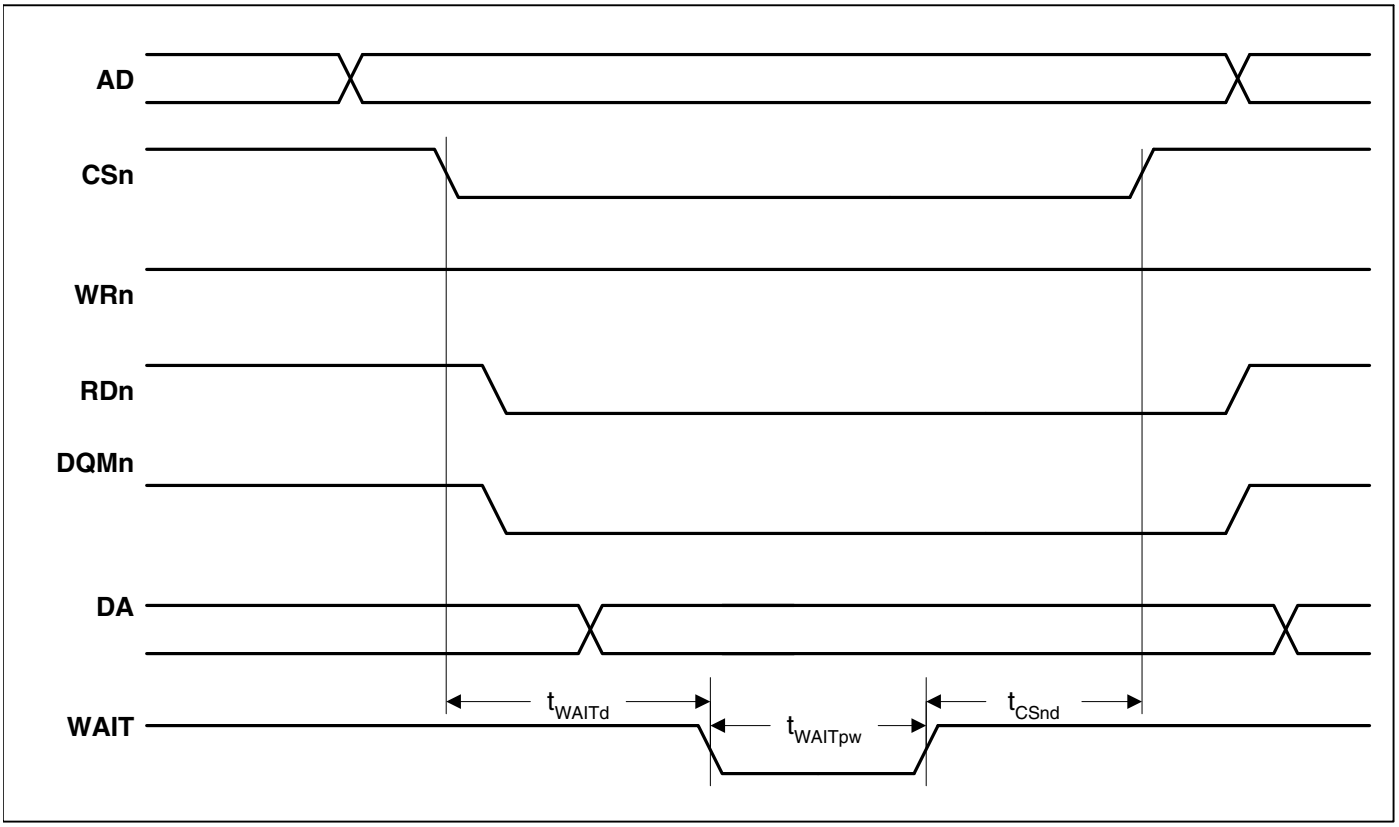


Figure 12. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

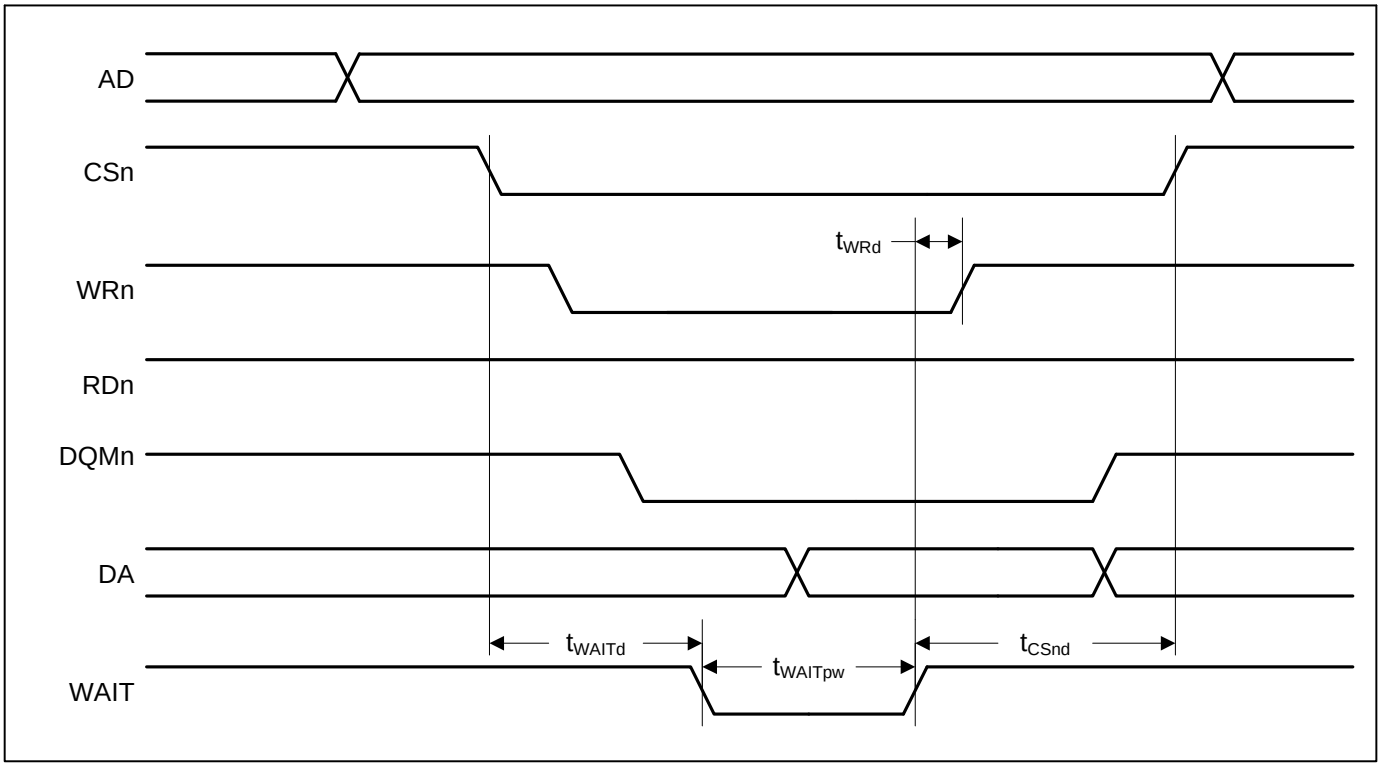


Figure 13. Static Memory Single Write Wait Cycle Timing Measurement

Ethernet MAC Interface

Parameter	Symbol	Min		Typ		Max		Unit
		10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	
TXCLK cycle time	t_{TX_per}	-	-	400	40	-	-	ns
TXCLK high time	t_{TX_high}	140	14	200	20	260	26	ns
TXCLK low time	t_{TX_low}	140	14	200	20	260	26	ns
TXCLK to signal transition delay time	t_{TXd}	0	0	10	10	25	25	ns
TXCLK rise/fall time	t_{TXrf}	-	-	-	-	5	5	ns
RXCLK cycle time	t_{RX_per}	-	-	400	40	-	-	ns
RXCLK high time	t_{RX_high}	140	14	200	20	260	26	ns
RXCLK low time	t_{RX_low}	140	14	200	20	260	26	ns
RXDVAL / RXERR setup time	t_{RXs}	10	10	-	-	-	-	ns
RXDVAL / RXERR hold time	t_{RXh}	10	10	-	-	-	-	ns
RXCLK rise/fall time	t_{RXrf}	-	-	-	-	5	5	ns
MDC cycle time	t_{MDC_per}	-	-	400	400	-	-	ns
MDC high time	t_{MDC_high}	160	160	-	-	-	-	ns
MDC low time	t_{MDC_low}	160	160	-	-	-	-	ns
MDC rise/fall time	t_{MDCrf}	-	-	-	-	5	5	ns
MDIO setup time (STA sourced)	t_{MDIOs}	10	10	-	-	-	-	ns
MDIO hold time (STA sourced)	t_{MDIOh}	10	10	-	-	-	-	ns
MDC to MDIO signal transition delay time (PHY sourced)	t_{MDIOd}	-	-	-	-	300	300	ns

STA - Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium.

PHY - Ethernet physical layer interface.

AC'97

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_per}	-	81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	-	45	ns
ABITCLK input low time	t_{clk_low}	36	-	45	ns
ABITCLK input rise/fall time	t_{clkrf}	2	-	6	ns
ASDI setup to ABITCLK falling	t_s	10	-	-	ns
ASDI hold after ABITCLK falling	t_h	10	-	-	ns
ASDI input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDO / ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC / ASDO rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

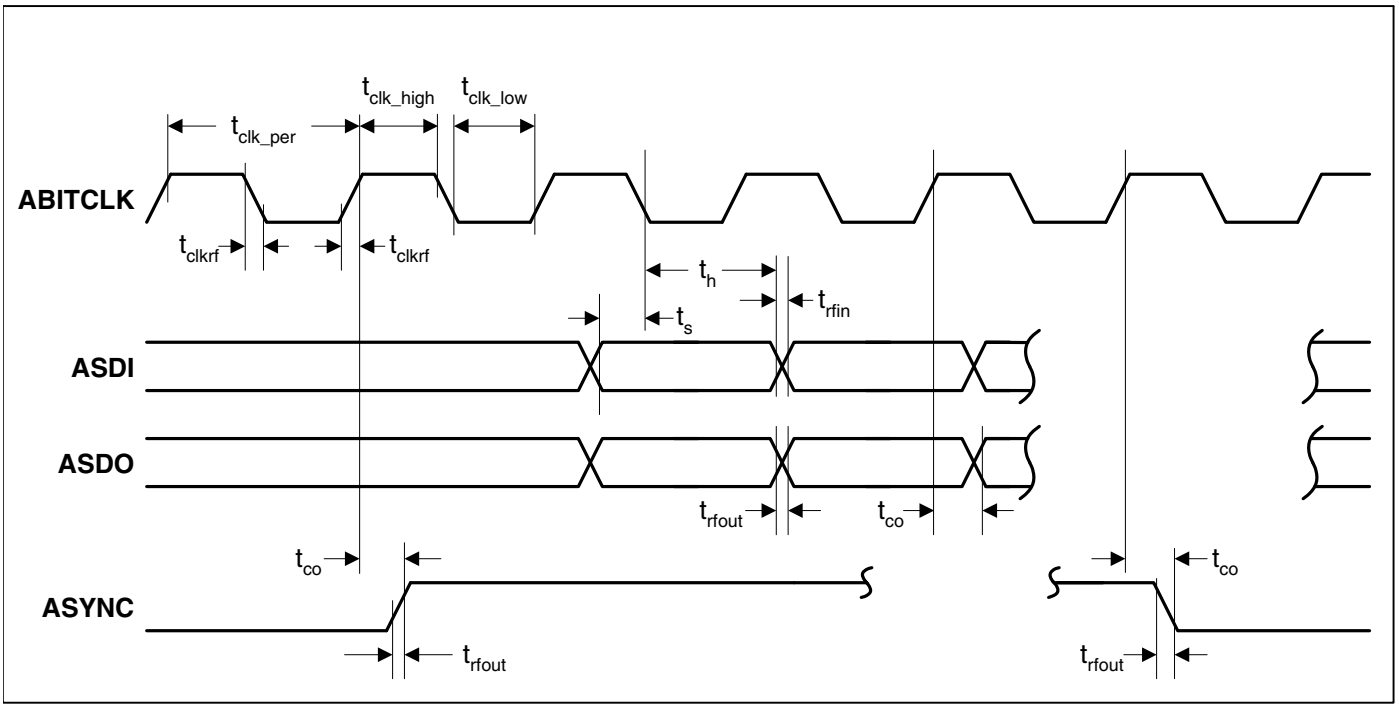
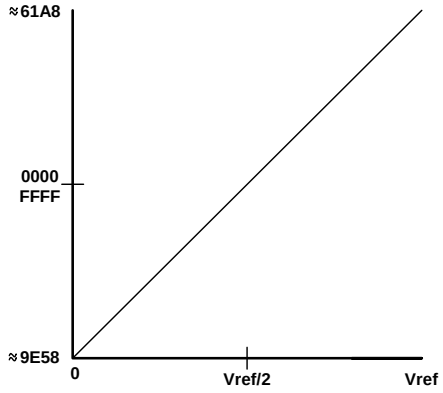


Figure 20. AC '97 Configuration Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 21. ADC Transfer Function

Using the ADC:

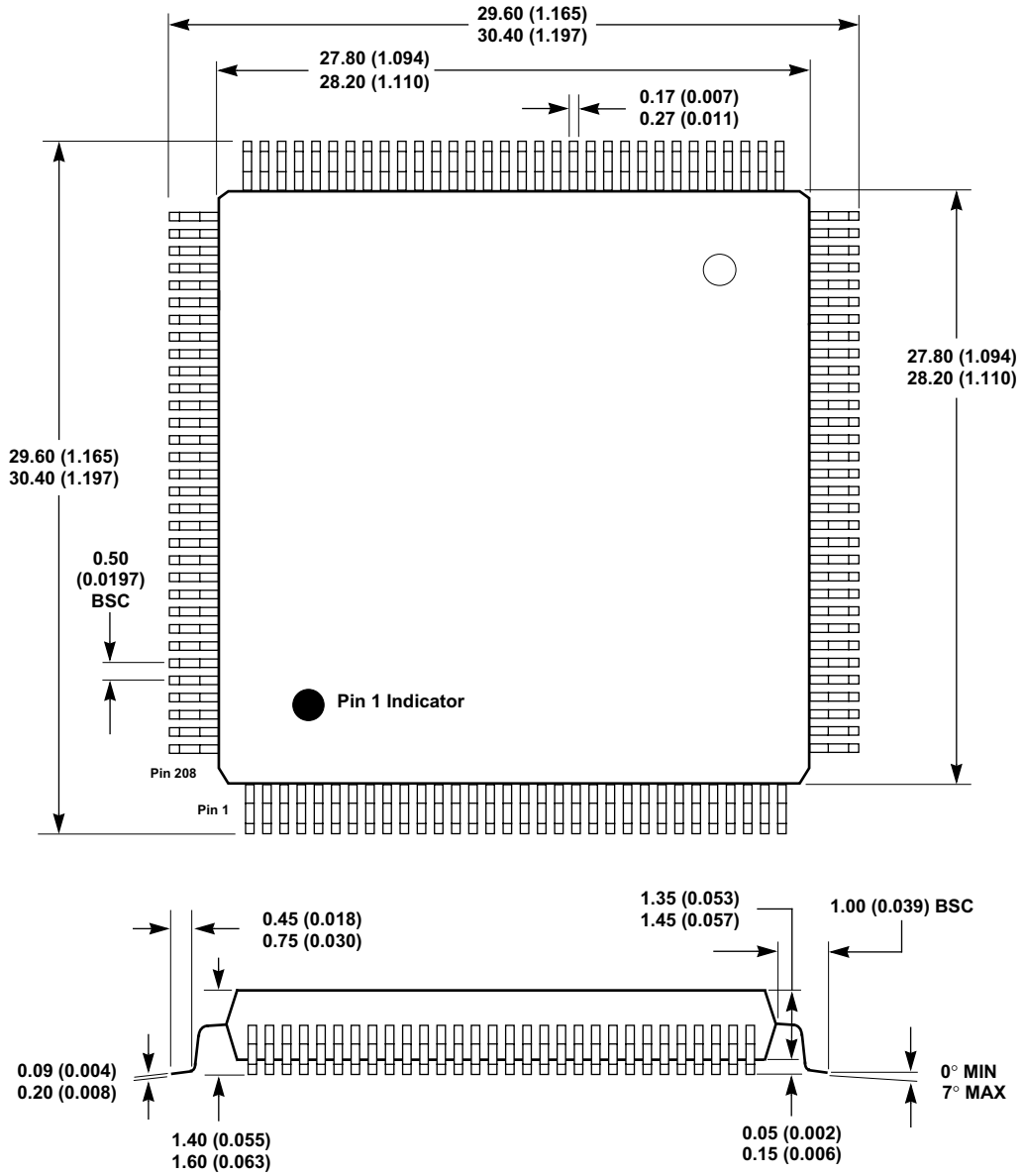
This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

208 Pin LQFP Package Outline

208-Pin LQFP (28 × 28 × 1.40-mm Body)



NOTES:

1) Dimensions are in millimeters, and controlling dimension is millimeter.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm (0.010 in).
3) Pin 1 identification may be either ink dot or dimple.
4) Package top dimensions can be smaller than bottom dimensions by 0.20 mm (0.008 in).
5) The 'lead width with plating' dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
6) Ejector pin marks in molding are present on every package.
7) Drawing above does not reflect exact package pin count.

208 Pin LQFP Pinout

The following table shows the 208 pin LQFP pinout.

- VDD_core is CVDD.
- VDD_ring is RVDD.
- NC means that the pin is not connected.

Pin List

The following Low-Profile Quad Flat Pack (LQFP) pin assignment table is sorted in order of pin.

Table P. Pin List in Numerical Order by Pin Number

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	CSn[7]	36	AD[5]	71	AD[9]	106	USBp[0]	141	EGPIO[10]	176	TXEN
2	CSn[6]	37	DA[12]	72	DA[1]	107	ABITCLK	142	EGPIO[9]	177	MIITXD[0]
3	CSn[3]	38	AD[4]	73	AD[8]	108	CTSn	143	EGPIO[8]	178	MIITXD[1]
4	CSn[2]	39	DA[11]	74	DA[0]	109	RXD[0]	144	EGPIO[7]	179	MIITXD[2]
5	CSn[1]	40	AD[3]	75	DSRn	110	RXD[1]	145	EGPIO[6]	180	MIITXD[3]
6	AD[25]	41	vdd_ring	76	DTRn	111	vdd_ring	146	EGPIO[5]	181	TXCLK
7	vdd_ring	42	gnd_ring	77	TCK	112	gnd_ring	147	EGPIO[4]	182	RXERR
8	gnd_ring	43	DA[10]	78	TDI	113	TXD[0]	148	EGPIO[3]	183	RXDVAL
9	AD[24]	44	AD[2]	79	TDO	114	TXD[1]	149	gnd_ring	184	MIIRXD[0]
10	SDCLK	45	DA[9]	80	TMS	115	CGPIO[0]	150	vdd_ring	185	MIIRXD[1]
11	AD[23]	46	AD[1]	81	vdd_ring	116	gnd_core	151	EGPIO[2]	186	MIIRXD[2]
12	vdd_core	47	DA[8]	82	gnd_ring	117	PLL_GND	152	EGPIO[1]	187	gnd_ring
13	gnd_core	48	AD[0]	83	BOOT[1]	118	XTALI	153	EGPIO[0]	188	vdd_ring
14	SDWEn	49	vdd_ring	84	BOOT[0]	119	XTALO	154	ARSTn	189	MIIRXD[3]
15	SDCSn[3]	50	gnd_ring	85	gnd_ring	120	PLL_VDD	155	TRSTn	190	RXCLK
16	SDCSn[2]	51	NC	86	NC	121	vdd_core	156	ASDI	191	MDIO
17	SDCSn[1]	52	NC	87	EECLK	122	gnd_ring	157	USBm[2]	192	MDC
18	SDCSn[0]	53	vdd_ring	88	EEDAT	123	vdd_ring	158	USBp[2]	193	RDn
19	vdd_ring	54	gnd_ring	89	ASYNC	124	RSTOn	159	WAITn	194	WRn
20	gnd_ring	55	AD[15]	90	vdd_core	125	PRSTn	160	EGPIO[15]	195	AD[16]
21	RASn	56	DA[7]	91	gnd_core	126	CSn[0]	161	gnd_ring	196	AD[17]
22	CASn	57	vdd_core	92	ASDO	127	gnd_core	162	vdd_ring	197	gnd_core
23	DQMn[1]	58	gnd_core	93	SCLK1	128	vdd_core	163	EGPIO[14]	198	vdd_core
24	DQMn[0]	59	AD[14]	94	SFRM1	129	gnd_ring	164	EGPIO[13]	199	HGPIO[2]
25	AD[22]	60	DA[6]	95	SSPRX1	130	vdd_ring	165	EGPIO[12]	200	HGPIO[3]
26	AD[21]	61	AD[13]	96	SSPTX1	131	ADC[4]	166	gnd_core	201	HGPIO[4]
27	vdd_ring	62	DA[5]	97	GRLED	132	ADC[3]	167	vdd_core	202	HGPIO[5]
28	gnd_ring	63	AD[12]	98	RDLED	133	ADC[2]	168	FGPIO[3]	203	gnd_ring
29	DA[15]	64	DA[4]	99	vdd_ring	134	ADC[1]	169	FGPIO[2]	204	vdd_ring
30	AD[7]	65	AD[11]	100	gnd_ring	135	ADC[0]	170	FGPIO[1]	205	AD[18]
31	DA[14]	66	vdd_ring	101	INT[3]	136	ADC_VDD	171	gnd_ring	206	AD[19]
32	AD[6]	67	gnd_ring	102	INT[1]	137	RTCXTALI	172	vdd_ring	207	AD[20]
33	DA[13]	68	DA[3]	103	INT[0]	138	RTCXTALO	173	CLD	208	SDCLKEN
34	vdd_core	69	AD[10]	104	RTSn	139	ADC_GND	174	CRS		
35	gnd_core	70	DA[2]	105	USBm[0]	140	EGPIO[11]	175	TXERR		

.

Table Q. Pin Description

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma		JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A		Main oscillator input
XTALO	PLL	A		Main oscillator output
VDD_PLL	PLL	P		Main oscillator power, 1.8V
GND_PLL	PLL	G		Main oscillator ground
RTCXTALI	RTC	A		RTC oscillator input
RTCXTALO	RTC	A		RTC oscillator output
WRn	EBUS	4ma		SRAM Write strobe out
RDn	EBUS	4ma		SRAM Read / OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma		Shared Address bus out
DA[15:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[1:0]	EBUS	8ma		Shared data mask out
SDCLK	SDRAM	8ma		SDRAM clock out
SDCLKEN	SDRAM	8ma		SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma		SDRAM chip selects out
RASn	SDRAM	8ma		SDRAM RAS out
CASn	SDRAM	8ma		SDRAM CAS out
SDWEn	SDRAM	8ma		SDRAM write enable out
ADC[4:0]	ADC	A		External Analog Measurement Input
VDD_ADC	ADC	P		ADC power, 3.3V
GND_ADC	ADC	G		ADC ground
USBp[2, 0]	USB	A		USB positive signals
USBm[2, 0]	USB	A		USB negative signals
TXD0	UART1	4ma		Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send / transmit enable
DSRn	UART1	I	PU	Data set ready / Data Carrier Detect
DTRn	UART1	4ma		Data Terminal Ready output
RTSn	UART1	4ma		Ready to send
TXD1	UART2	4ma		Transmit / IrDA output
RXD1	UART2	I	PU	Receive / IrDA input
MDC	EMAC	4ma		Management data clock
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	I	PU	Transmit clock in
MIITXD[3:0]	EMAC	4ma	PD	Transmit data out

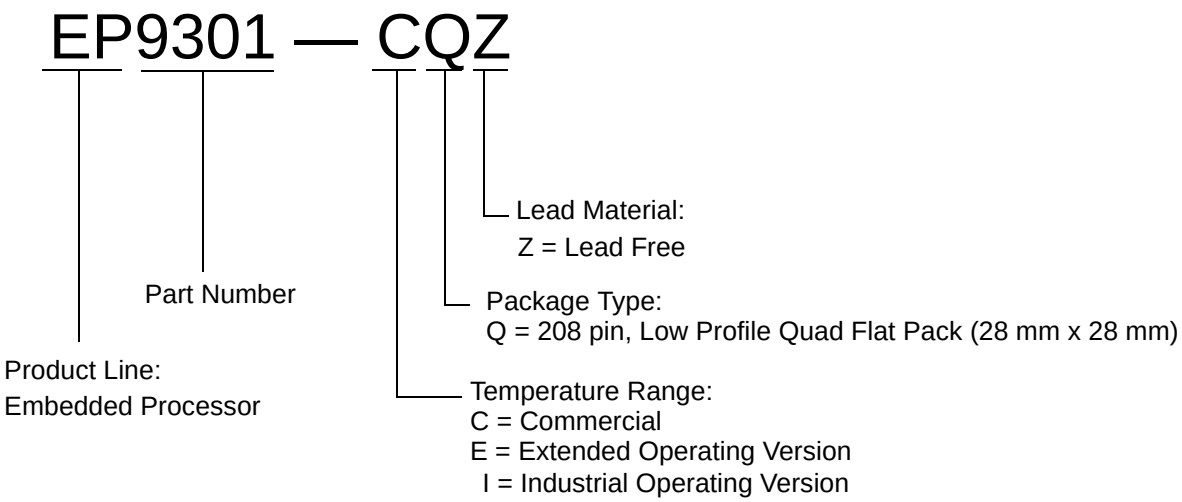
Table Q. Pin Description (Continued)

Pin Name	Block	Pad Type	Pull Type	Description
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma		Green LED
RDLED	LED	12ma		Red LED
EECLK	EEPROM	4ma	PU	EEPROM / Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM / Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma		AC97 reset
SCLK1	SPI1	I/O, 8ma	PD	SPI bit clock
SFRM1	SPI1	I/O, 8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma		SPI output
INT[3], INT[1:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma		User Reset in out - open drain
EGPIO[15:0]	GPIO	I/O, 4ma	PU	Enhanced GPIO
FGPIO[3:1]	GPIO	I/O, 8ma	PU	GPIO on Port F
HGPIO[5:2]	GPIO	I/O, 8ma	PU	GPIO on Port H
CGPIO[0]	GPIO	I/O, 8ma	PU	GPIO on Port C
CVDD	Power	P		Digital power, 1.8V
RVDD	Power	P		Digital power, 3.3V
CGND	Ground	G		Digital ground
RGND	Ground	G		Digital ground

ORDERING INFORMATION

The order numbers for the device are:

EP9301-CQZ	0°C to +70°C	208-pin LQFP	Lead Free
EP9301-IQZ	-40°C to +85°C	208-pin LQFP	Lead Free



Note: Go to the Cirrus Logic Internet site at http://www.cirrus.com to find contact information for your local sales representative.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**