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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9301-iqz

OVERVIEW

The EP9301 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Industrial controls
- Digital media servers
- Integrated home media gateways
- Digital audio jukeboxes
- Streaming audio players
- Set-top boxes
- Point-of-sale terminals
- Thin clients
- Biometric security systems
- GPS & fleet management systems
- Educational toys
- Industrial computers
- Industrial hand-held devices
- Voting machines
- Medical equipment

The EP9301 is one of a series of ARM920T-based devices. Other members of the family have different peripheral sets, a coprocessor, and different package configurations.

The ARM920T microprocessor core has a separate 16-kbyte, 64-way set-associative instruction and data caches.

The MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100 Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, AC'97 and I^2S audio. A two-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second), two UARTs, and a analog voltage measurement analog-to-digital converter (ADC) are included as well.

The EP9301 is a high-performance, low-power RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 166 MHz. The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 675 mW.

Table A. Change History

Revision	Date	Changes
1	October 2003	Initial Release.
2	February 2004	Update timing specifications.
3	July 2004	Update AC data.
4	July 2004	Add ADC data.
5	March 2005	Update with most-current characterization data.
F1	February 2010	Removed "Preliminary Data" statement from legal disclaimer. Removed lead-containing device part numbers. Increased minimum CVDD & VDD_PLL voltages from 1.65 V min. to 1.71 V min. Changed operating temperatures to 0 to 60°C commercial, -40 to 70°C industrial.
F2	March 2010	Increased commercial/industrial temperatures to 70/85 deg. C max.

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List of Figures

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Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16-kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- MMU for Linux®, Microsoft® Windows® CE and other operating systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP9301 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9301 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, FLASH)

The EP9301 features a unified memory address model where all memory devices are accessed over a common address/data bus. Memory accesses are performed via the Processor bus. The SRAM memory controller supports 8- and 16-bit devices and accommodates an internal boot ROM concurrently with 16-bit SDRAM memory.

- 1 to 4 banks of 16-bit, 66 MHz SDRAM
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[15:0]	Data Bus 15-0
DQMn[1:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read / OE Strobe
WAITn	SRAM Wait Input

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PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table J. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free-running down counters or as periodic timers for fixed-interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus a 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 54 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time-critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 54 interrupts from a variety of sources (such as UARTs, GPIO and ADC)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines INT[2:0] operate as active-high level-sensitive interrupts
- Any of the 19 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table K. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[3] and INT[1:0]	External Interrupts 2, 1, 0

Note: INT[2] is not bonded out.

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table L. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 16 EGPIO and the 3 FGPIO pins may each be configured individually as an output, an input or an interrupt input.

There are 10 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Ethernet MDIO
- Both LED Outputs
- EEPROM Clock and Data
- HGPIO[5:2]
- CGPIO[0]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn / DCDn
- 3 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table M. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[3:1]	Expanded General Purpose Input / Output Pins with Interrupts

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Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation (Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)		-	±10	mA
Output current per pin, DC		-	±50	mA
Digital Input voltage (Note 2)		-0.3	RVDD+0.3	V
Storage temperature		-40	+125	°C

Note: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	166	MHz
Processor Clock Speed - Industrial	FCLK	-	-	166	MHz
System Clock Speed - Commercial	HCLK	-	-	66	MHz
System Clock Speed - Industrial	HCLK	-	-	66	MHz

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Timings

Timing Diagram Conventions

This data sheet contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

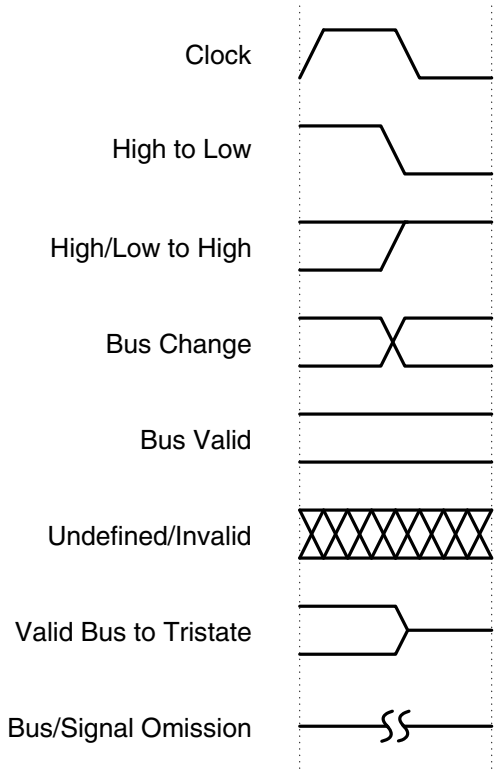

Figure 1. Timing Diagram Drawing Key

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements.

- T_A = 0 to 70° C
- CVDD = VDD_PLL = 1.8V
- RVDD = 3.3 V
- All grounds = 0 V
- Logic 0 = 0 V, Logic 1 = 3.3 V
- Output loading = 50 pF
- Timing reference levels = 1.5 V
- The Processor Bus Clock (HCLK) is programmable and is set by the user. The frequency is typically between 33 MHz and 100 MHz (92 MHz for industrial conditions).

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SDRAM Burst Read Cycle

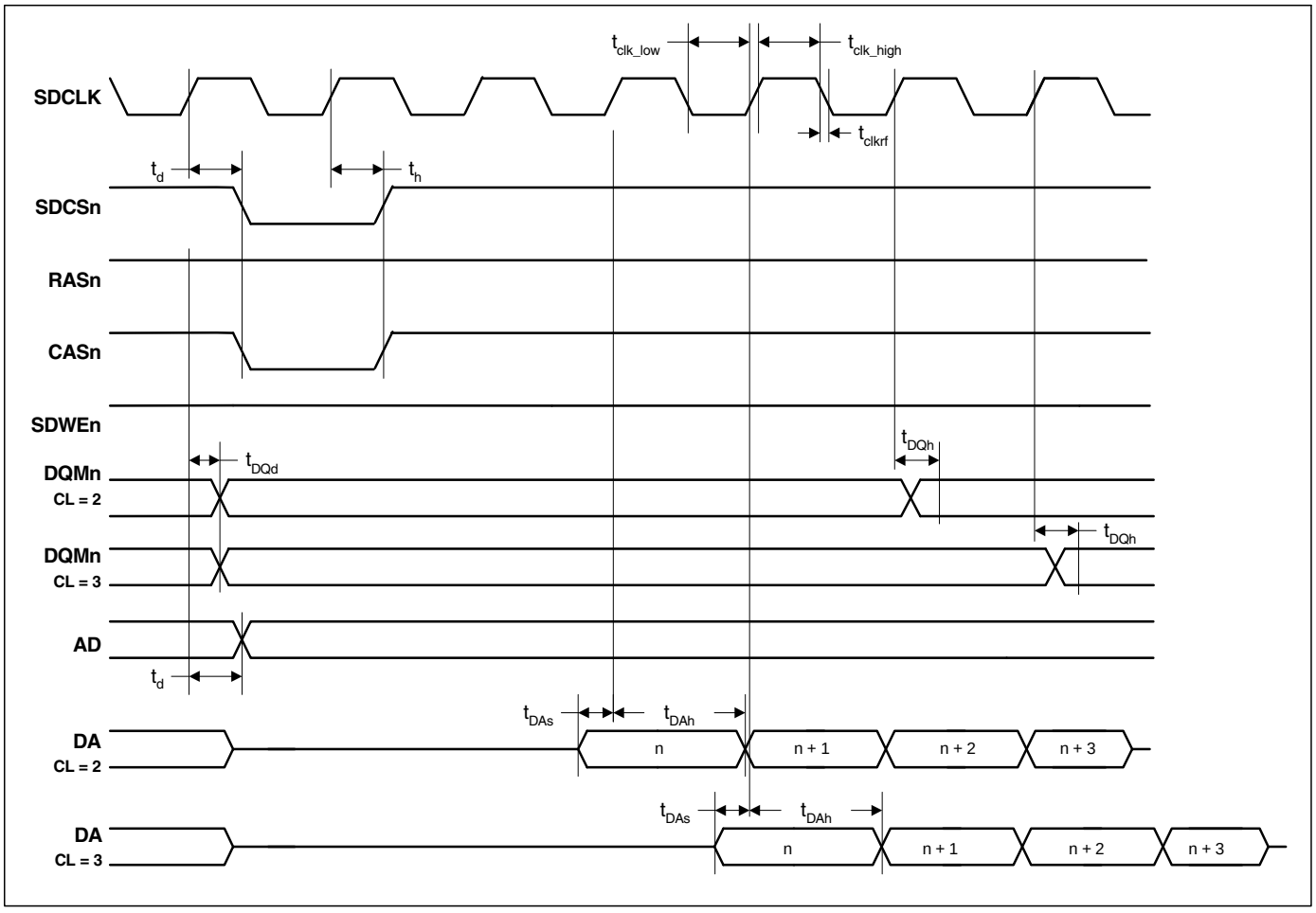

Figure 3. SDRAM Burst Read Cycle Timing Measurement

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Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

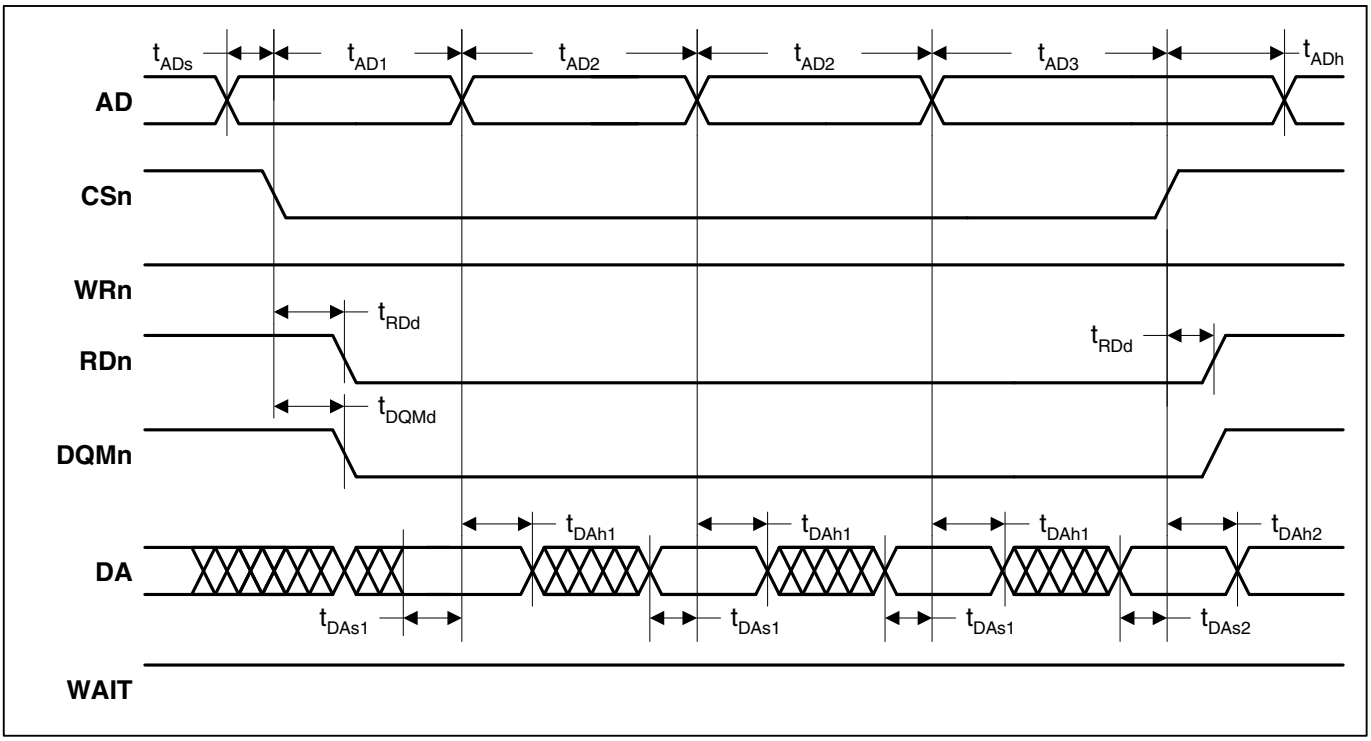

Figure 6. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

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Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

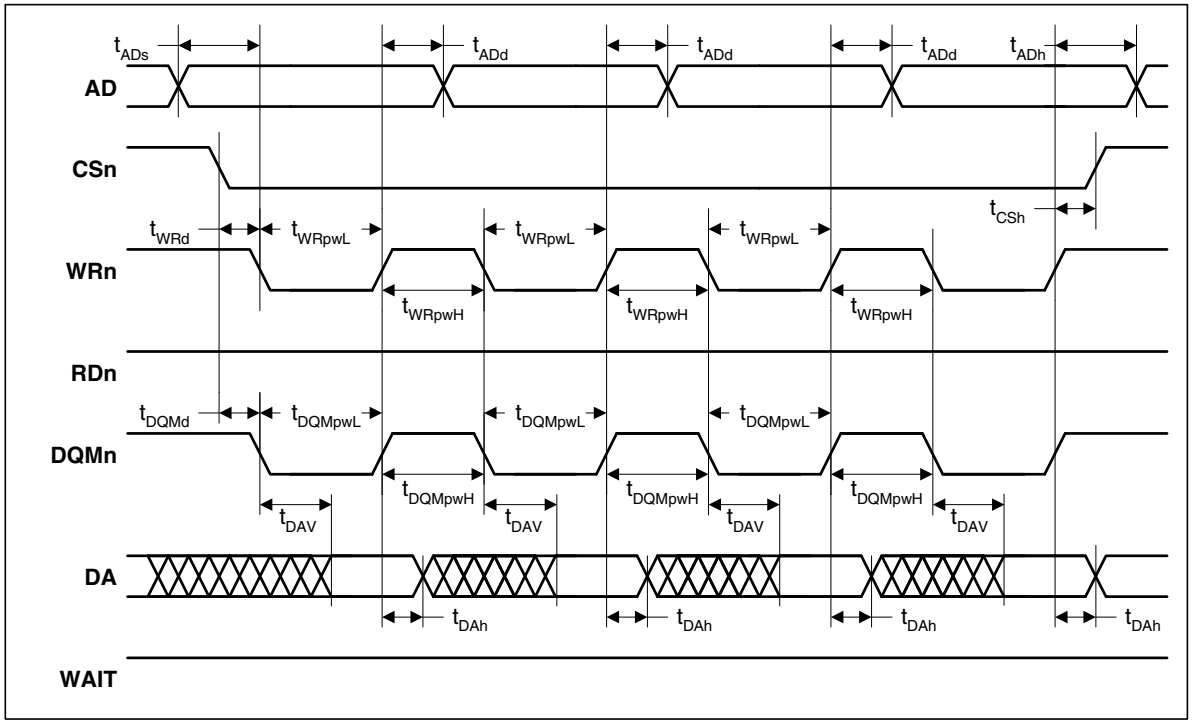

Figure 7. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

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Static Memory 32-bit Read on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to AD transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd2}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times ((2 \times WST1) + 3)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA to RDn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

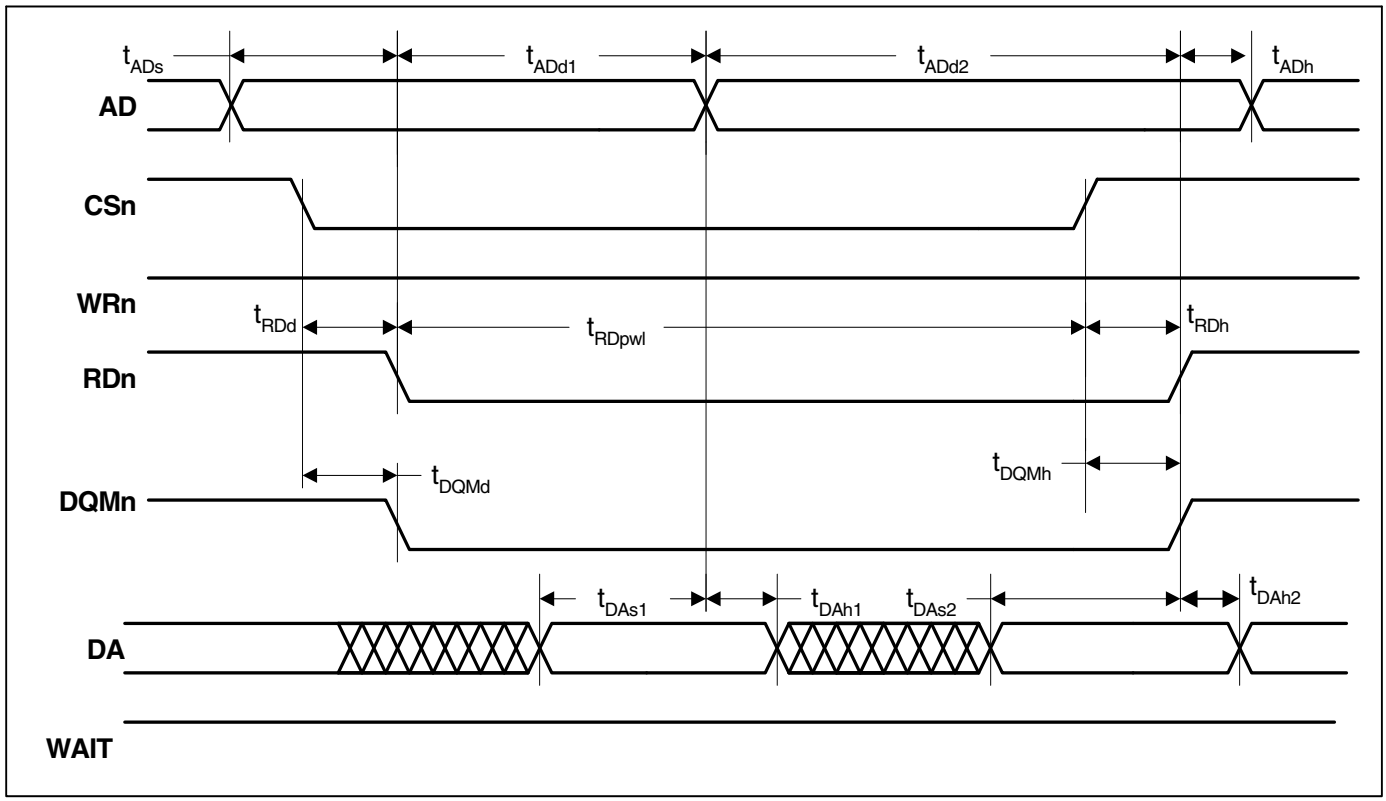

Figure 8. Static Memory Multiple Word Read 16-bit Cycle Timing Measurement

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Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

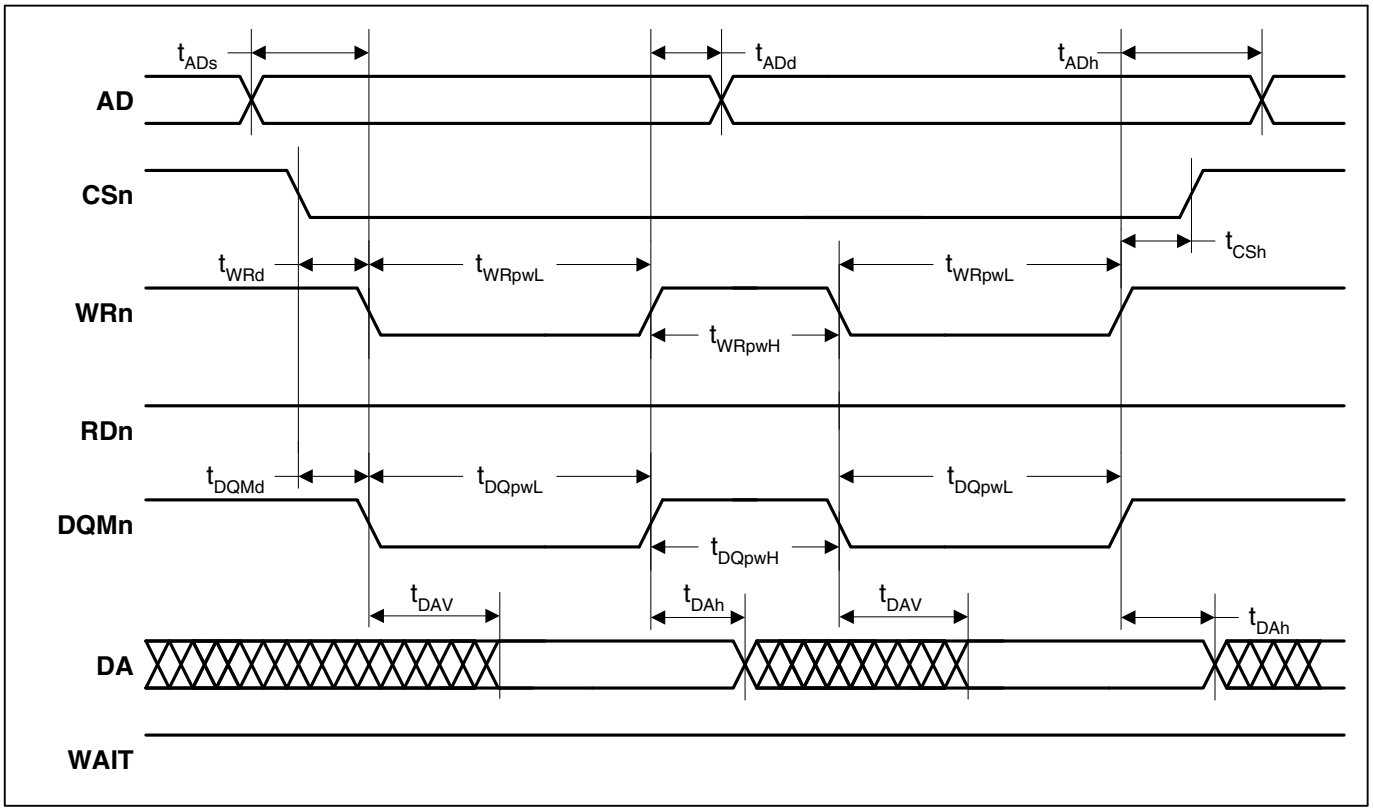

Figure 9. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

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Static Memory Turnaround Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSnX deassert to CSnY assert time	t_{BTcyc}	-	$t_{HCLK} \times (IDCY+1)$	-	ns

Notes: 1. X and Y represent any two chip select numbers.
2. IDCY occurs on read-to-write and write-to-read.
3. IDCY is honored when going from a asynchronous device (CSx) to a synchronous device (/SDCSy).

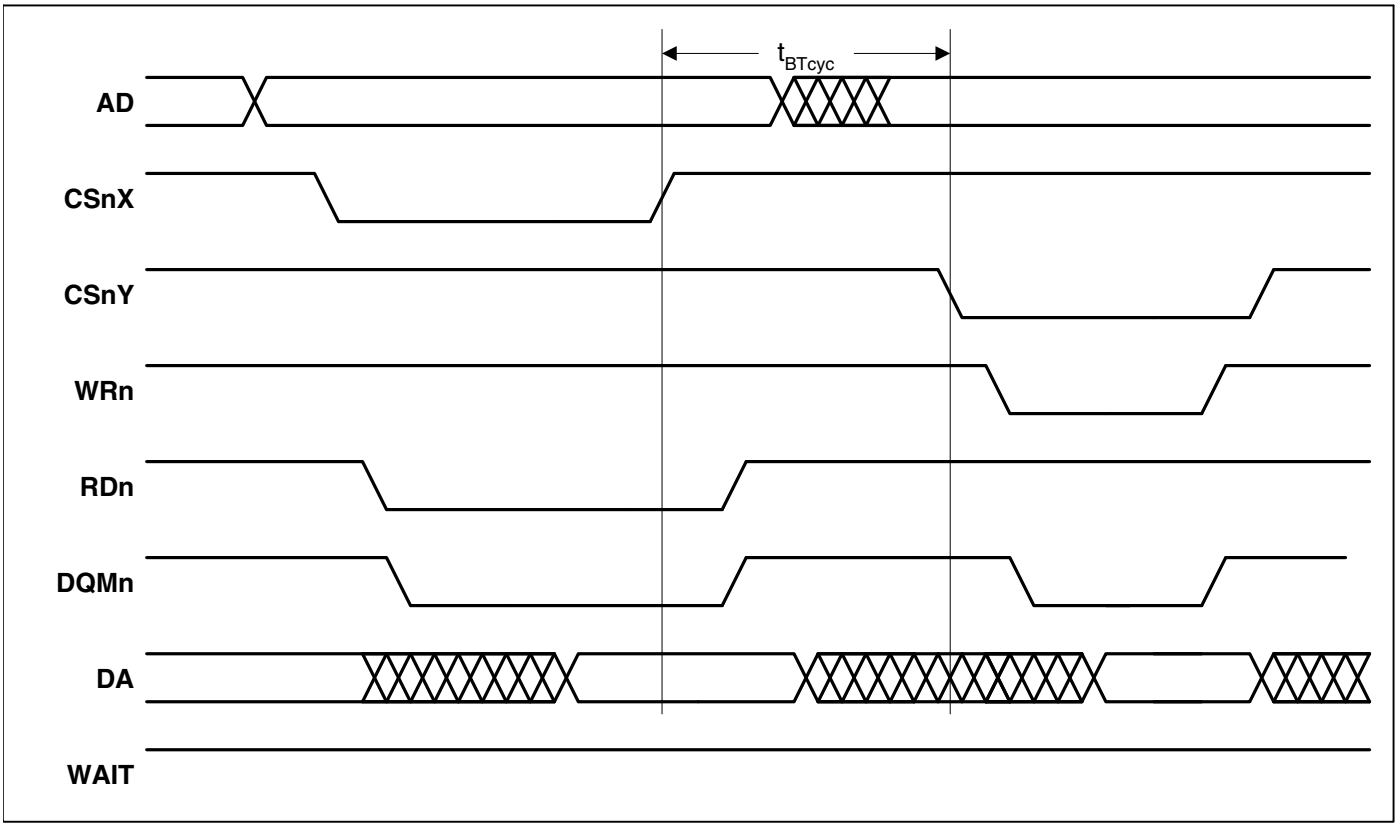

Figure 14. Static Memory Turnaround Cycle Timing Measurement

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Ethernet MAC Interface

Parameter	Symbol	Min		Typ		Max		Unit
		10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	
TXCLK cycle time	t_{TX_per}	-	-	400	40	-	-	ns
TXCLK high time	t_{TX_high}	140	14	200	20	260	26	ns
TXCLK low time	t_{TX_low}	140	14	200	20	260	26	ns
TXCLK to signal transition delay time	t_{TXd}	0	0	10	10	25	25	ns
TXCLK rise/fall time	t_{TXrf}	-	-	-	-	5	5	ns
RXCLK cycle time	t_{RX_per}	-	-	400	40	-	-	ns
RXCLK high time	t_{RX_high}	140	14	200	20	260	26	ns
RXCLK low time	t_{RX_low}	140	14	200	20	260	26	ns
RXDVAL / RXERR setup time	t_{RXs}	10	10	-	-	-	-	ns
RXDVAL / RXERR hold time	t_{RXh}	10	10	-	-	-	-	ns
RXCLK rise/fall time	t_{RXrf}	-	-	-	-	5	5	ns
MDC cycle time	t_{MDC_per}	-	-	400	400	-	-	ns
MDC high time	t_{MDC_high}	160	160	-	-	-	-	ns
MDC low time	t_{MDC_low}	160	160	-	-	-	-	ns
MDC rise/fall time	t_{MDCrf}	-	-	-	-	5	5	ns
MDIO setup time (STA sourced)	t_{MDIOs}	10	10	-	-	-	-	ns
MDIO hold time (STA sourced)	t_{MDIOh}	10	10	-	-	-	-	ns
MDC to MDIO signal transition delay time (PHY sourced)	t_{MDIOd}	-	-	-	-	300	300	ns

STA - Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium.

PHY - Ethernet physical layer interface.

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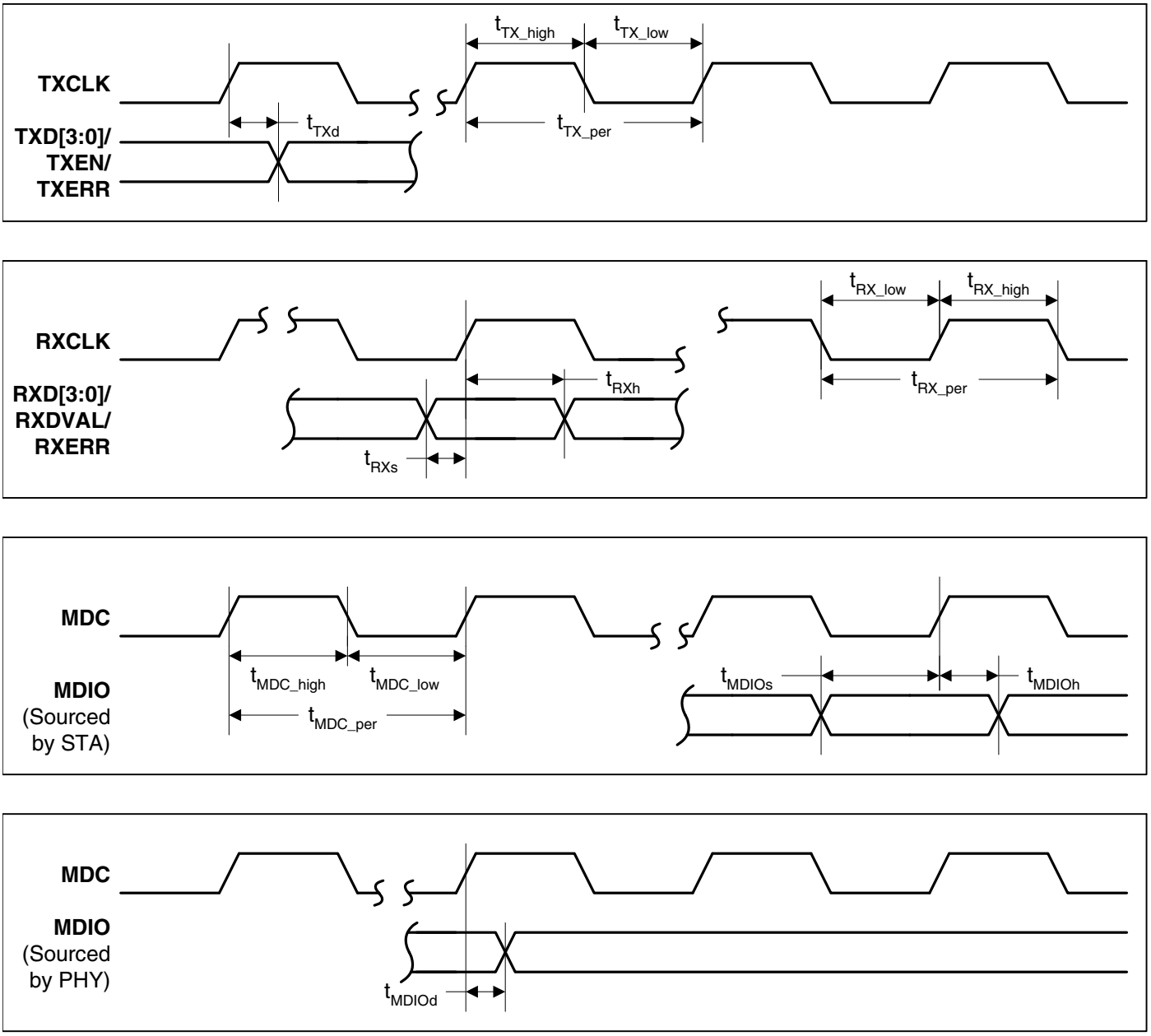

Figure 15. Ethernet MAC Timing Measurement

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Motorola SPI

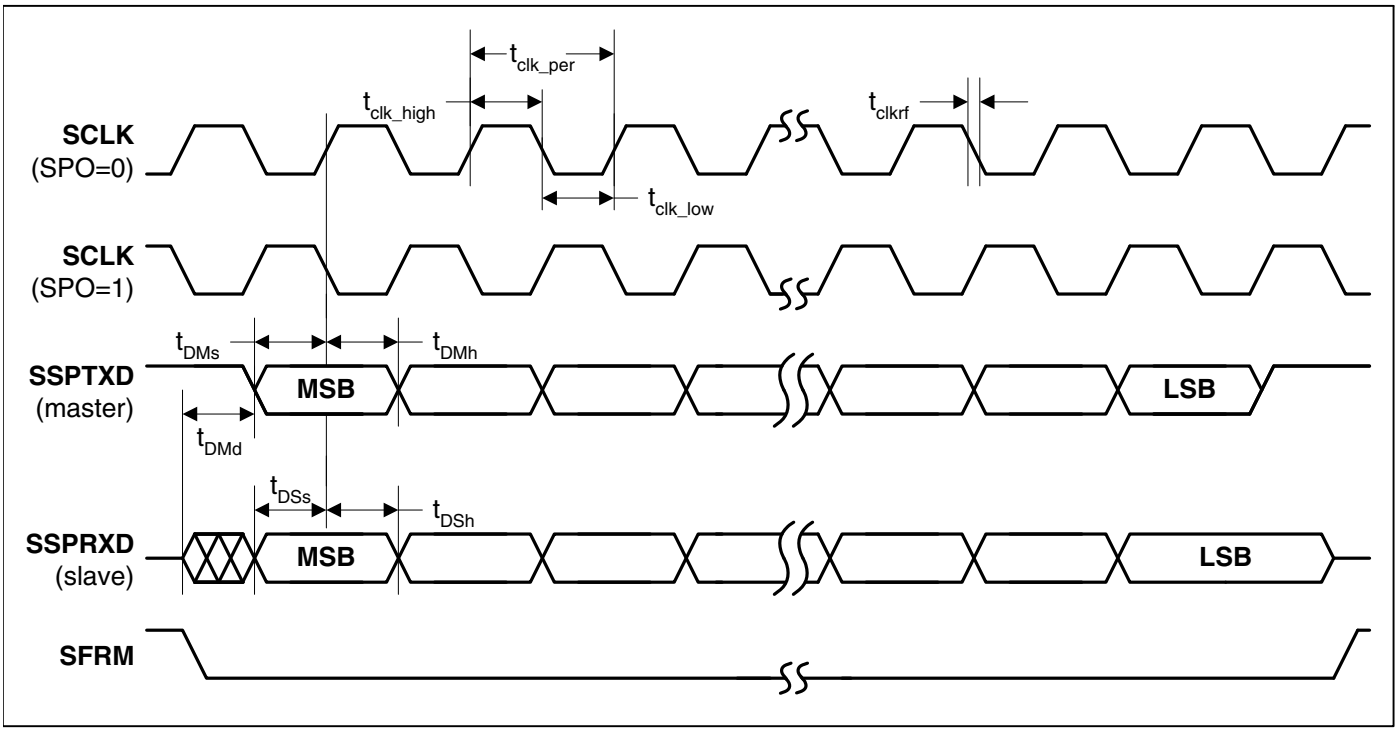

Figure 18. SPI Format with SPH=1 Timing Measurement

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Inter-IC Sound - I²S

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	t_{i2s_clk}	-	ns
SCLK high time	t_{clk_high}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK low time	t_{clk_low}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK rise/fall time	t_{clkrf}	1	4	8	ns
SCLK to LRCLK assert delay time	t_{LRd}	-	-	3	ns
Hold between SCLK assert then LRCLK deassert *or* Hold between LRCLK deassert then SCLK assert	t_{LRh}	0	-	-	ns
SDI to SCLK deassert setup time	t_{SDIs}	12	-	-	ns
SDI from SCLK deassert hold time	t_{SDIh}	0	-	-	ns
SCLK assert to SDO delay time	t_{SDOd}	-	-	9	ns
SDO from SCLK assert hold time	t_{SDOh}	1	-	-	ns

Note: t_{i2s_clk} is programmable by the user.

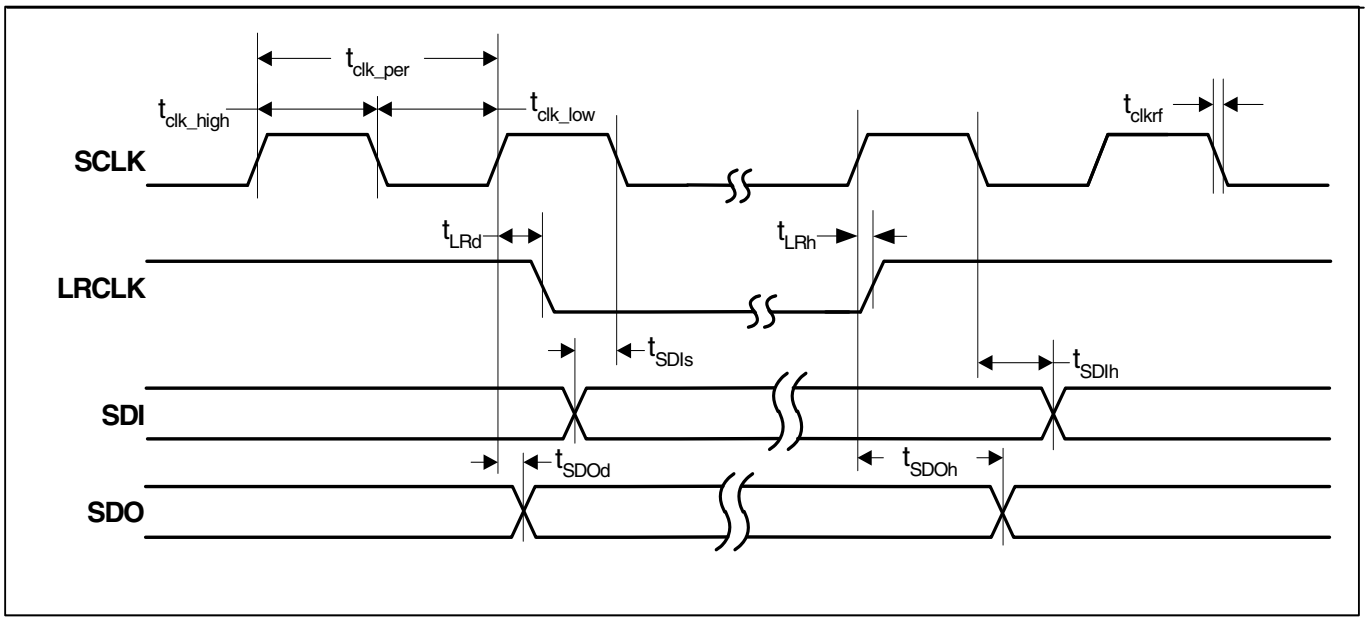

Figure 19. Inter-IC Sound (I²S) Timing Measurement

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AC'97

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_per}	-	81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	-	45	ns
ABITCLK input low time	t_{clk_low}	36	-	45	ns
ABITCLK input rise/fall time	t_{clkrf}	2	-	6	ns
ASDI setup to ABITCLK falling	t_s	10	-	-	ns
ASDI hold after ABITCLK falling	t_h	10	-	-	ns
ASDI input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDO / ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC / ASDO rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

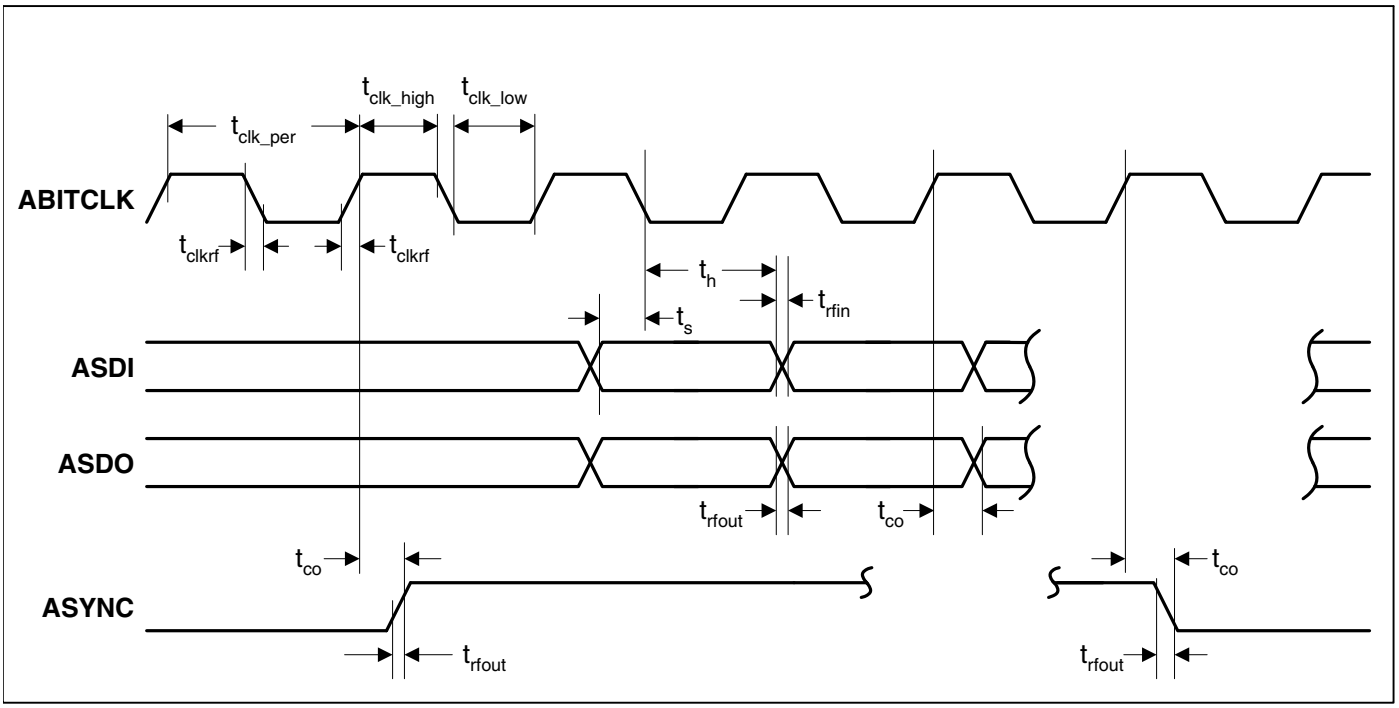

Figure 20. AC '97 Configuration Timing Measurement

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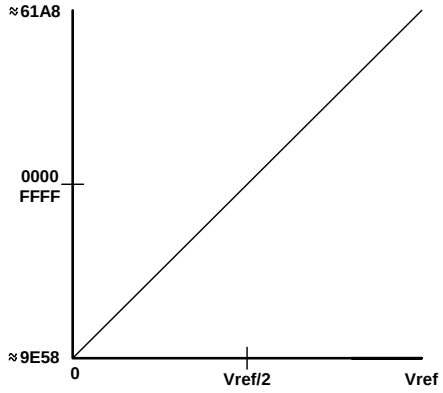
ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 21. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

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The following section focuses on the EP9301 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table Q) is a summary of all the EP9301 pin signals. The second table (Table R) illustrates the pin signal multiplexing and configuration options.

Table Q is a summary of the EP9301 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4mA output driver
- 8mA - Pin is an 8mA output driver
- 12mA - Pin is an 12mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply

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