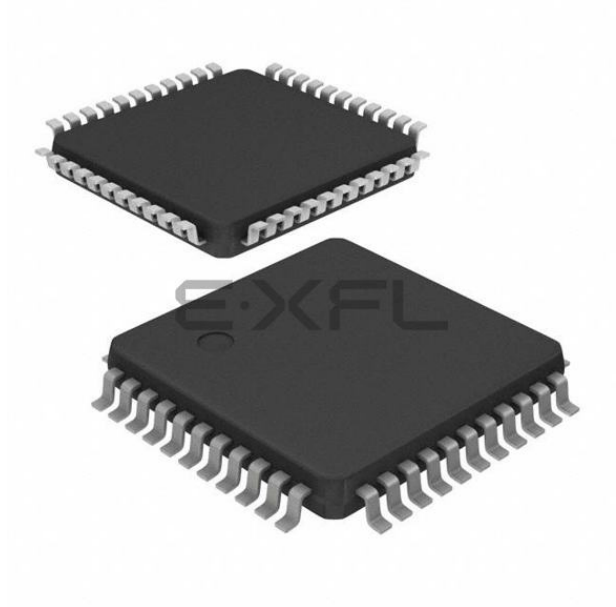

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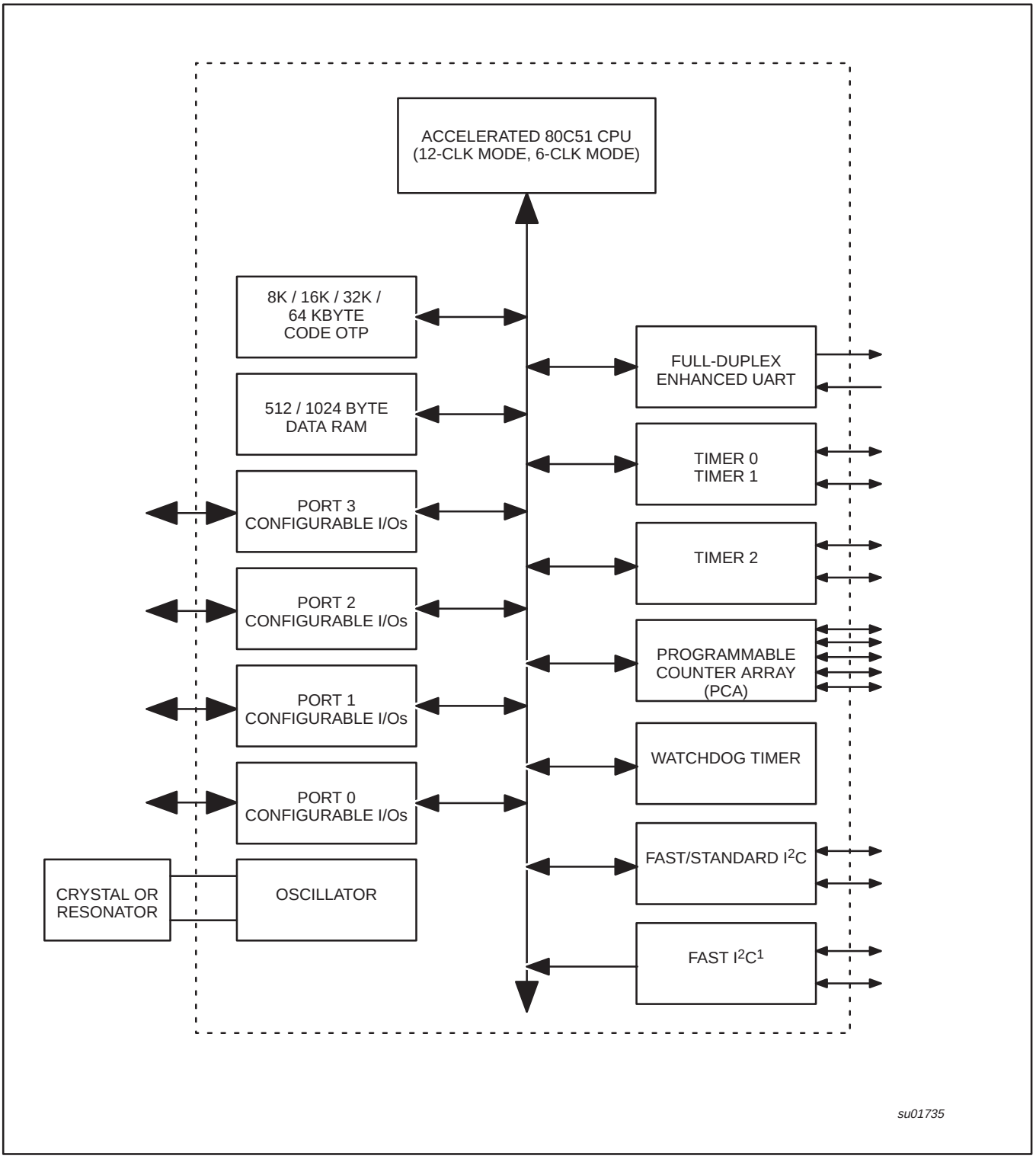
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c660x2bbd-157

BLOCK DIAGRAM 1



1. 2nd I²C on P8xC661X2 only.

SPECIAL FUNCTION REGISTERS (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1/ CEX4	T0/ CEX3	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#[1]	Power Control	87H	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	000000x0B
RCAP2H#	Timer 2 Capture High	CBH									00H
RCAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
S1CON	I2C Control	D8H	CR2	ENA1	STA	STO	SI	AA	CR1	CR0	00H
S1STA	I2C STATUS	D9H	SC4	SC3	SC2	SC1	SC0	0	0	0	F8H
S1DAT	I2C DATA	DAH									00H
S1ADR	I2C ADDRESS	DBH								GC	00H
S2CON[2]	Second I²C control	F8H	CR2	ENA1	STA	STO	SI	AA	CR1	CR0	00H
S2STA[2]	Second I²C	F1H	SC4	SC3	SC2	SC1	SC0	0	0	0	F8H
S2DAT[2]	Second I²C	F2H									00H
S2ADR[2]	Second I²C	F3H								GC	00H
S2IST[2]	Second I²C	F4H									
IP1[2]	Interrupt priority 1	E7H								PS2	00H
IP1H[2]		F7H								PS2H	00H
WDTRST	Watchdog Timer Reset	A6H									

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.
2. 8xC661X2 only.

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin LOW restarts the oscillator but bringing the pin back HIGH completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

LPEP

The EPROM array contains some analog circuits that are not required when V_{CC} is less than 3.6 V but are required for a V_{CC} greater than 3.6 V. The LPEP bit (AUXR.4), when set, will powerdown these analog circuits resulting in a reduced supply current. This bit should be set ONLY for applications that operate at a V_{CC} less than 4 V.

POWER-ON FLAG

The Power-On Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P8xC66xX2 rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE LOW while the device is in reset and $\overline{PSEN}$ is HIGH;
2. Hold ALE LOW as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled HIGH. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency in 12-clock mode (122 Hz to 8 MHz in 6-clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

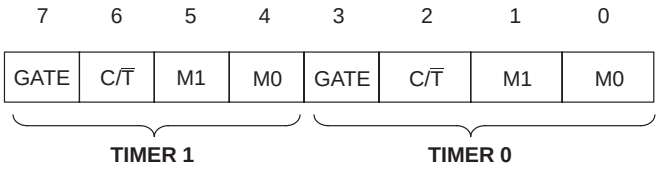
n = 2 in 6-clock mode
4 in 12-clock mode

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

TMOD Address = 89H Reset Value = 00H

Not Bit Addressable

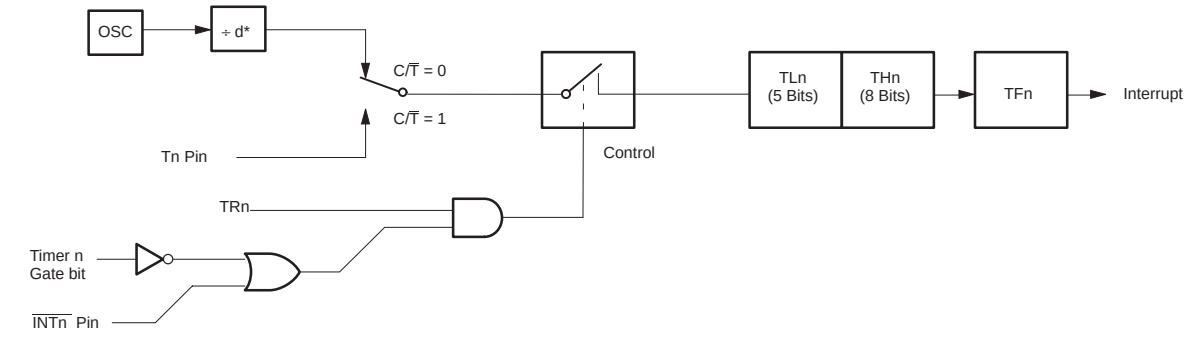


BIT	SYMBOL	FUNCTION
TMOD.3/ TMOD.7	GATE	Gating control when set. Timer/Counter "n" is enabled only while "$\overline{INTn}$" pin is high and "TRn" control pin is set. when cleared Timer "n" is enabled whenever "TRn" control bit is set.
TMOD.2/ TMOD.6	C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from "Tn" input pin).

M1	M0	OPERATING
0	0	8048 Timer: "TLn" serves as 5-bit prescaler.
0	1	16-bit Timer/Counter: "THn" and "TLn" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter: "THn" holds a value which is to be reloaded into "TLn" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

SU01580

Figure 2. Timer/Counter 0/1 Mode Control (TMOD) Register



*d = 6 in 6-clock mode; d = 12 in 12-clock mode.

SU01618

Figure 3. Timer/Counter 0/1 Mode 0: 13-Bit Timer/Counter

SCON Address = 98H Reset Value = 00H

Bit Addressable

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	$f_{OSC}/12$ (12-clock mode) or $f_{OSC}/6$ (6-clock mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$ (12-clock mode) or $f_{OSC}/32$ or $f_{OSC}/16$ (6-clock mode)
1	1	3	9-bit UART	variable

SM2 Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.

REN Enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8 The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

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Figure 7. Serial Port Control (SCON) Register

Baud Rate			f_{OSC}	SMOD	Timer 1		
Mode	12-clock mode	6-clock mode			C/$\overline{T}$	Mode	Reload Value
Mode 0 Max	1.67 MHz	3.34 MHz	20 MHz	X	X	X	X
Mode 2 Max	625 k	1250 k	20 MHz	1	X	X	X
Mode 1, 3 Max	104.2 k	208.4 k	20 MHz	1	0	2	FFH
Mode 1, 3	19.2 k	38.4 k	11.059 MHz	1	0	2	FDH
	9.6 k	19.2 k	11.059 MHz	0	0	2	FDH
	4.8 k	9.6 k	11.059 MHz	0	0	2	FAH
	2.4 k	4.8 k	11.059 MHz	0	0	2	F4H
	1.2 k	2.4 k	11.059 MHz	0	0	2	E8H
	137.5	275	11.986 MHz	0	0	2	1DH
	110	220	6 MHz	0	0	2	72H
	110	220	12 MHz	0	0	1	FEEBH

Figure 8. Timer 1 Generated Commonly Used Baud Rates

More About Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed a 1/12 the oscillator frequency (12-clock mode) or 1/6 the oscillator frequency (6-clock mode).

Figure 9 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is LOW during S3, S4, and S5 of every machine cycle, and HIGH during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.”

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are

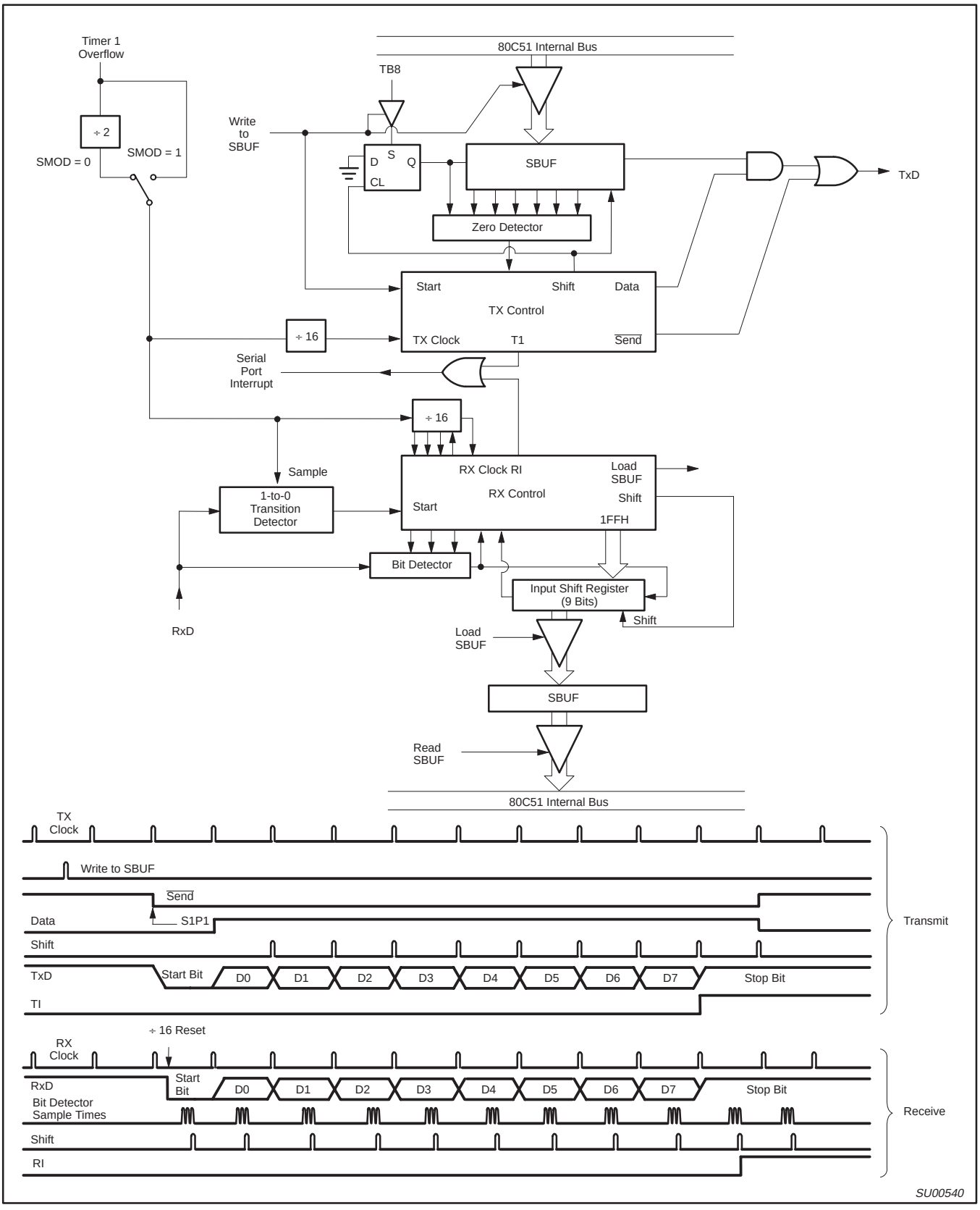

Figure 10. Serial Port Mode 1

SIO1 and SIO2, I2C Serial I/O

The I2C-bus is a simple bi-directional 2-wire bus to transfer information between devices connected to the bus. The main features of the bus are:

- Only two bus lines are required: a serial clock line (SCL) and a serial data line (SDA).
- Bi-directional data transfer between masters and slaves.
- Each device connected to the bus is software addressable by a unique address.
- Masters can operate as Master-transmitter or as Master-receiver.
- It is a true multi-master bus (no central master) and includes collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via the same serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Devices can be added to or removed from an I2C-bus system without affecting any other device on the bus.
- Fault diagnostics and debugging are simple; malfunctions can be immediately traced.

For more information see the Philips publication “The I2C-Bus Specification”, especially for detailed descriptions of the Fast and the Standard data-transfer modes. Also, refer to the data sheets for the 8xC552, the 8xC554, the 8xC557, and the 8xC65x.

The SIO1 I2C serial port interface has a selectable bi-directional data-transfer mode, either the 400Kbit/s Fast-mode or the 100Kbit/s Standard-mode. In the Fast-mode, the port performance and the register definitions are identical to those of the 8xC557 devices, and in the Standard-mode (the reset default), they are identical to those of the 8xC652, 8xC654, 8xC552, and 8xC554 devices.

The Fast-mode is functionally the same as the Standard-mode except for the bit rate selection (see Tables 7 and 8), the timing of the SCL and SDA signals (see the I2C electrical characteristics), and the output slew-rate control. The Fast-mode allows up to a four-fold bit-rate increase over that of the Standard-mode, and yet, it is downward compatible with the Standard-mode, i.e. it can be used in a 0 to 100Kbit/s bus system.

The SCL serial port for the clock line of the I2C bus is an alternate function of the P1.6 port pin, and the SDA serial port for the data line of the I2C bus is an alternate function of the P1.7 port pin. Consequently, these 2 port pins are open drain outputs (no pull-ups), and the output latches of P1.6 and P1.7 must be set to logic 1 in order to enable the SIO1 outputs.

The second I2C serial port of the 8xC661X2, SIO2, has the 400Kbit/s Fast data-transfer mode only and selectable slew-rate control of the output pins. It also has the same port performance and register definitions as those of the 8xC557. The SCL1 and SDA1 serial ports have dedicated pins with open-drain outputs and Schmitt-trigger inputs.

There is an analog circuit for controlling the turn-on and turn-off rates of the output pull-down (slew-rate control circuit) which is required to meet the electrical specifications of the Fast-mode under nominal conditions (5 V). To achieve the maximum slew-rates, the circuit must be disabled. For the SIO1 serial port, the slew-rate control circuits for both the SCL and SDA pins are disabled in the Standard mode (maximum slew-rate), and they are enabled in the Fast-mode. For the SIO2 serial port, the slew-rate control circuits for both pins are enabled by reset, but the Slew-Rate Disable bit (SRD bit) in the AUXR Register disables the slew-rate circuits for both the SCL1 and SDA1 pins when set for maximum slew-rates. This feature of the SIO2 slew-rate control is very useful for higher bus loads, higher temperatures and lower voltages that cause additional decreases in slew-rates.

All of the functional descriptions discussed below apply to both the SIO1 and the SIO2 I2C serial ports although the text may refer to the SIO1 only. See page 10 for the corresponding SIO2 register addresses.

The I2C on-chip logic performs a byte oriented data transfer, clock generation, address recognition and bus control arbitration, and interfaces to the external I2C-bus via the two port pins SCL and SDA. It meets the I2C-bus specification and supports all transfer modes (other than the low-speed mode) from-and-to the I2C-bus. The logic handles byte transfers autonomously. It also keeps track of serial transfers, and a status register (SxSTA) reflects the status of the SIOx logic and the I2C-bus.

The CPU interfaces to the logic of each of the two I2Cs via the following four Special Function Registers (where x=1,2):

- SxCON: Control register, bit addressable by the CPU.
- SxSTA: Status register whose contents may be used as a vector to service routines.
- SxDAT: Data shift register; the data byte is stable as long as the SI bit = 1 (SxCON.3).
- SxADR: Slave address register; its LSB enables / disables general call address recognition.

A typical I2C-bus configuration is shown in Figure 15, and Figure 16 shows how a data transfer is accomplished on the bus. Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I2C-bus:

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the I2C bus will not be released.

Modes of Operation: The on-chip SIO1 logic may operate in the following four modes:

1. Master Transmitter Mode:

   Serial data output through P1.7/SDA while P1.6/SCL outputs the serial clock. The first byte transmitted contains the slave address

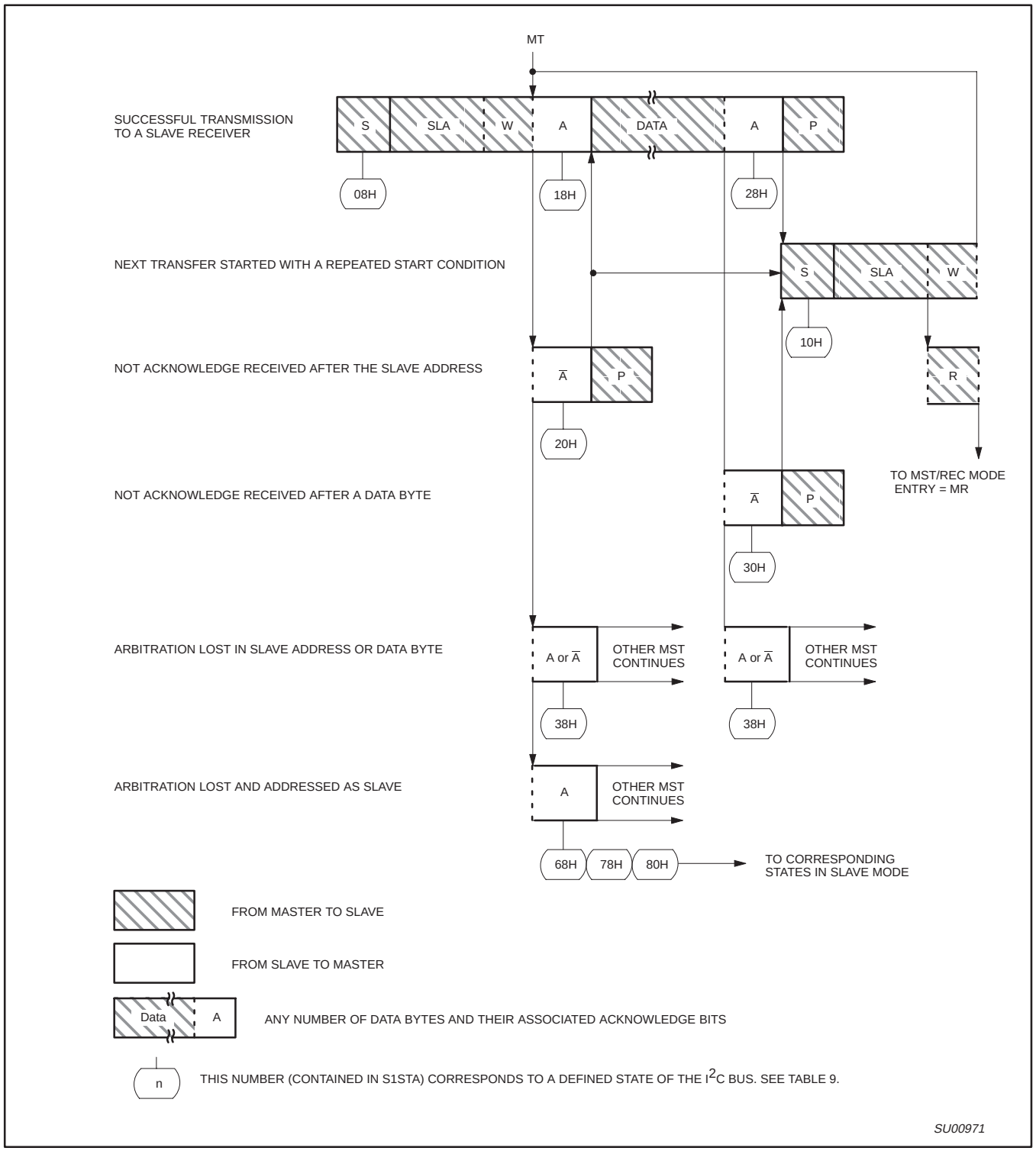

Figure 22. Format and States in the Master Transmitter Mode

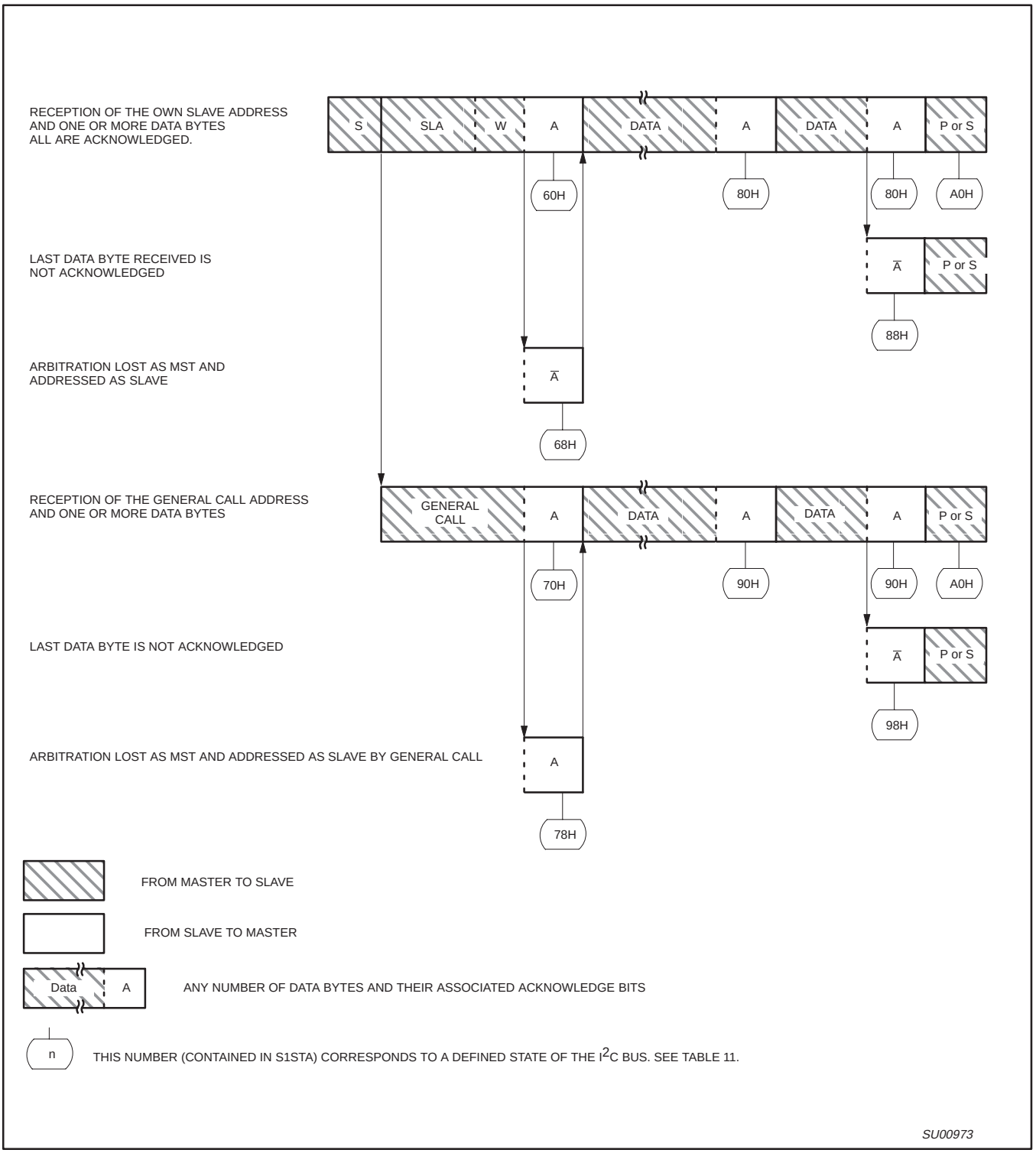

Figure 24. Format and States in the Slave Receiver Mode

Table 10. Master Receiver Mode

STATUS CODE (S1STA)	STATUS OF THE I²C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
08H	A START condition has been transmitted	Load SLA+R	X	0	0	X	SLA+R will be transmitted; ACK bit will be received
10H	A repeated START condition has been transmitted	Load SLA+R or	X	0	0	X	As above
		Load SLA+W	X	0	0	X	SLA+W will be transmitted; SIO1 will be switched to MST/TRX mode
38H	Arbitration lost in NOT ACK bit	No S1DAT action or	0	0	0	X	I²C bus will be released; SIO1 will enter a slave mode
		No S1DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free
40H	SLA+R has been transmitted; ACK has been received	No S1DAT action or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned
		no S1DAT action	0	0	0	1	Data byte will be received; ACK bit will be returned
48H	SLA+R has been transmitted; NOT ACK has been received	No S1DAT action or	1	0	0	X	Repeated START condition will be transmitted
		no S1DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		no S1DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset
50H	Data byte has been received; ACK has been returned	Read data byte or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned
		read data byte	0	0	0	1	Data byte will be received; ACK bit will be returned
58H	Data byte has been received; NOT ACK has been returned	Read data byte or	1	0	0	X	Repeated START condition will be transmitted
		read data byte or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset
		read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset

Table 11. Slave Receiver Mode (Continued)

STATUS CODE (S1STA)	STATUS OF THE I²C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX	No STDAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		No STDAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		No STDAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		No STDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

Table 12. Slave Transmitter Mode

STATUS CODE (S1STA)	STATUS OF THE I²C BUS AND SIO1 HARDWARE	APPLICATION SOFTWARE RESPONSE					NEXT ACTION TAKEN BY SIO1 HARDWARE
		TO/FROM S1DAT	TO S1CON				
			STA	STO	SI	AA	
A8H	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received
B0H	Arbitration lost in SLA+R/$\overline{W}$ as master; Own SLA+R has been received, ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
B8H	Data byte in S1DAT has been transmitted; ACK has been received	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received
		load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received
C0H	Data byte in S1DAT has been transmitted; NOT ACK has been received	No S1DAT action or	0	0	0	01	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.
C8H	Last data byte in S1DAT has been transmitted (AA = 0); ACK has been received	No S1DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address
		no S1DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1
		no S1DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free
		no S1DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if S1ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.

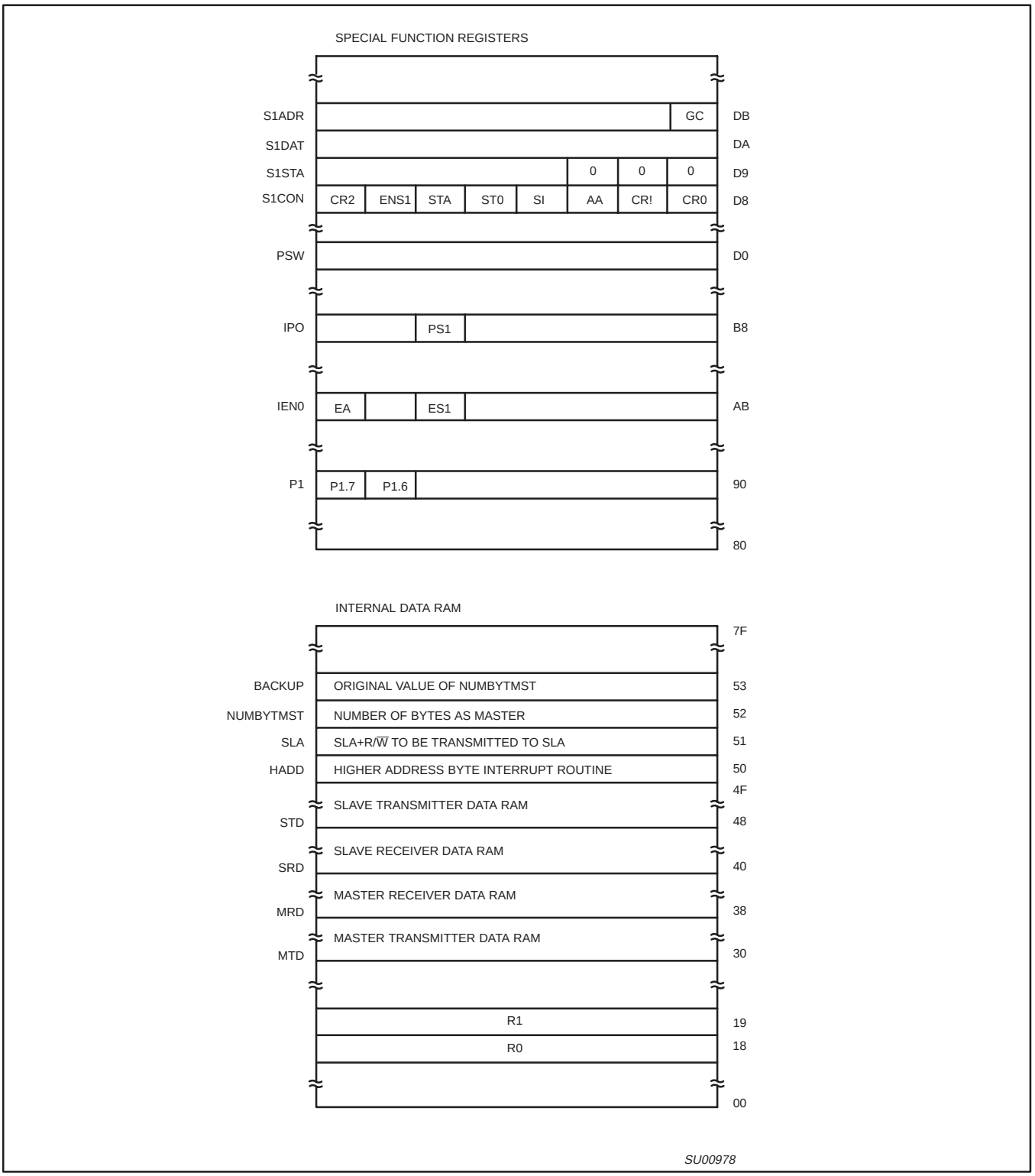

Figure 29. SIO1 Data Memory Map

```
                        !*************************************************************************************************
                        !*************************************************************************************************
                        ! MASTER RECEIVER STATE SERVICE ROUTINES
                        !*************************************************************************************************
                        !*************************************************************************************************

                        !-------------------------------------------------------------
                        ! STATE    : 40, Previous state was STATE 08 or STATE 10,
                        !            SLA+R have been transmitted, ACK received.
                        ! ACTION   : DATA will be received, ACK returned.
                        !-------------------------------------------------------------
                        .sect      mts40
                        .base      0x140

0140    75D8C5                                mov   S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                          ! clr  STA, STO, SI  set  AA
0143    D0D0                                  pop   psw
        32                                    reti

                        !-------------------------------------------------------------
                        ! STATE    : 48, SLA+R have been transmitted, NOT ACK received.
                        ! ACTION   : STOP condition will be generated.
                        !-------------------------------------------------------------
                        .sect      mts48
                        .base      0x148

0148    75D8D5          STOP:                 mov   S1CON,#ENS1_NOTSTA_STO_NOTSI_AA_CR0
                                                                          ! set  STO, clr  SI
014B    D0D0                                  pop   psw
014D    32                                    reti

                        !-------------------------------------------------------------
                        ! STATE    : 50, DATA have been received, ACK returned.
                        ! ACTION   : Read DATA of S1DAT.
                        !            DATA will be received, if it is last DATA
                                     then NOT ACK will be returned else ACK will be returned.
                        !-------------------------------------------------------------
                        .sect      mrs50
                        .base      0x150

0150    75D018                                mov   psw,#SELRB3
0153    A6DA                                  mov   @r0,S1DAT                   ! Read received DATA
0155    01C0                                  ajmp  REC1

                        .sect      mrs50s
                        .base      0xc0

00C0    D55205          REC1:                 djnz  NUMBYTMST,NOTLDAT2
00C3    75D8C1                                mov   S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_NOTAA_CR0
                                                                          ! clr  SI,AA
00C6    8003                                  sjmp  RETmr
00C8    75D8C5          NOTLDAT2:             mov   S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CR0
                                                                          ! clr  SI, set  AA
00CB    08              RETmr:                inc   r0
00CC    D0D0                                  pop   psw
00CE    32                                    reti

                        !-------------------------------------------------------------
                        ! STATE    : 58, DATA have been received, NOT ACK returned.
                        ! ACTION   : Read DATA of S1DAT and generate a STOP condition.
                        !-------------------------------------------------------------
                        .sect      mrs58
                        .base      0x158

0158    75D018                                mov   psw,#SELRB3
015B    A6DA                                  mov   @R0,S1DAT
015D    80E9                                  sjmp  STOP
```

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output unless the CPU needs to perform an off-chip memory access.

Reduced EMI Mode

AUXR (8EH)

7	6	5	4	3	2	1	0
–	–	SRD	–	Fast/ STD I²C	–	EXTRAM	AO

AUXR.0 AO

See more detailed description in Figure 48.

Dual DPTR

The dual DPTR structure (see Figure 34) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxxxxx0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
–	–	–	LPEP	GPS	0	–	DPS

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF2 bit is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF2 bit.

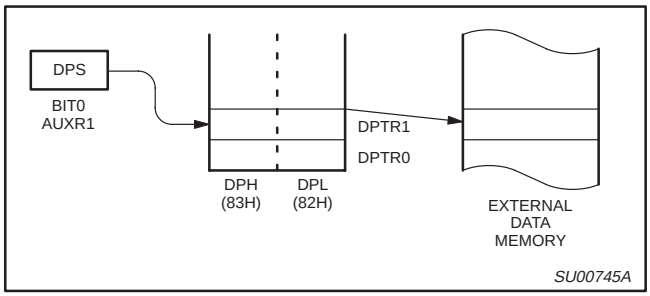

Figure 34.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the LOW or HIGH byte in an instruction which accesses the SFRs. See *Application Note AN458* for more details.

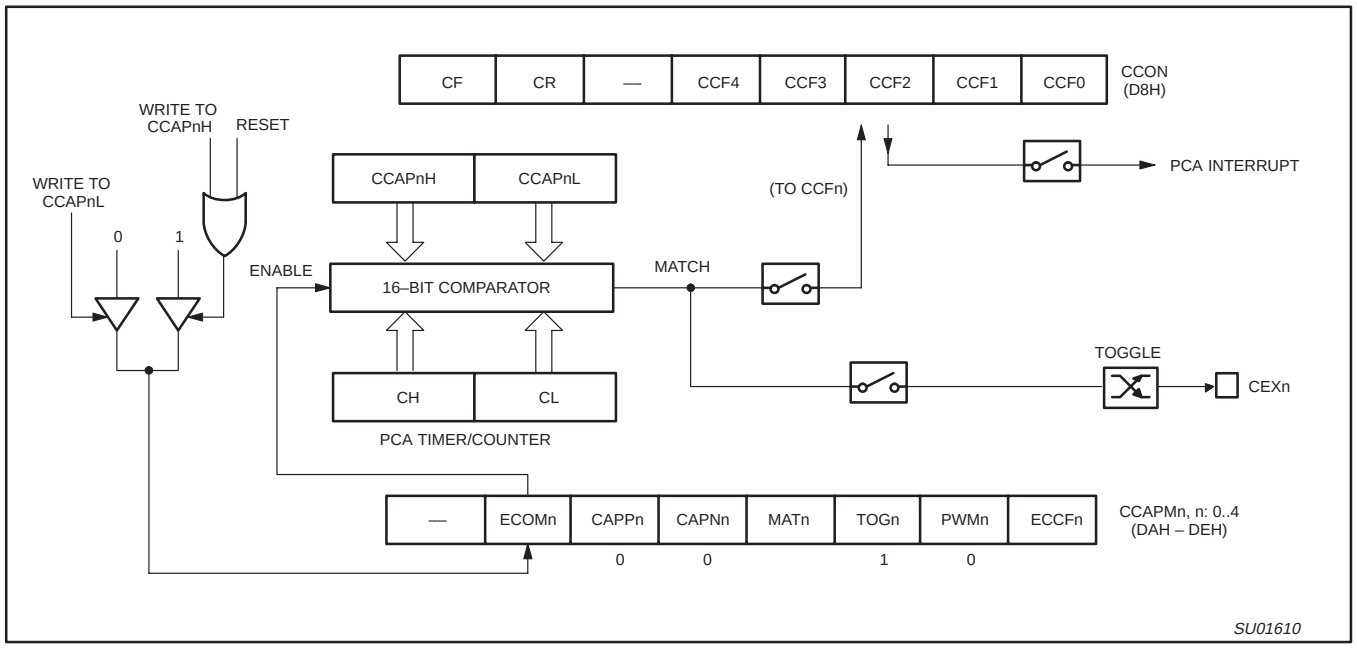

Figure 44. PCA High Speed Output Mode

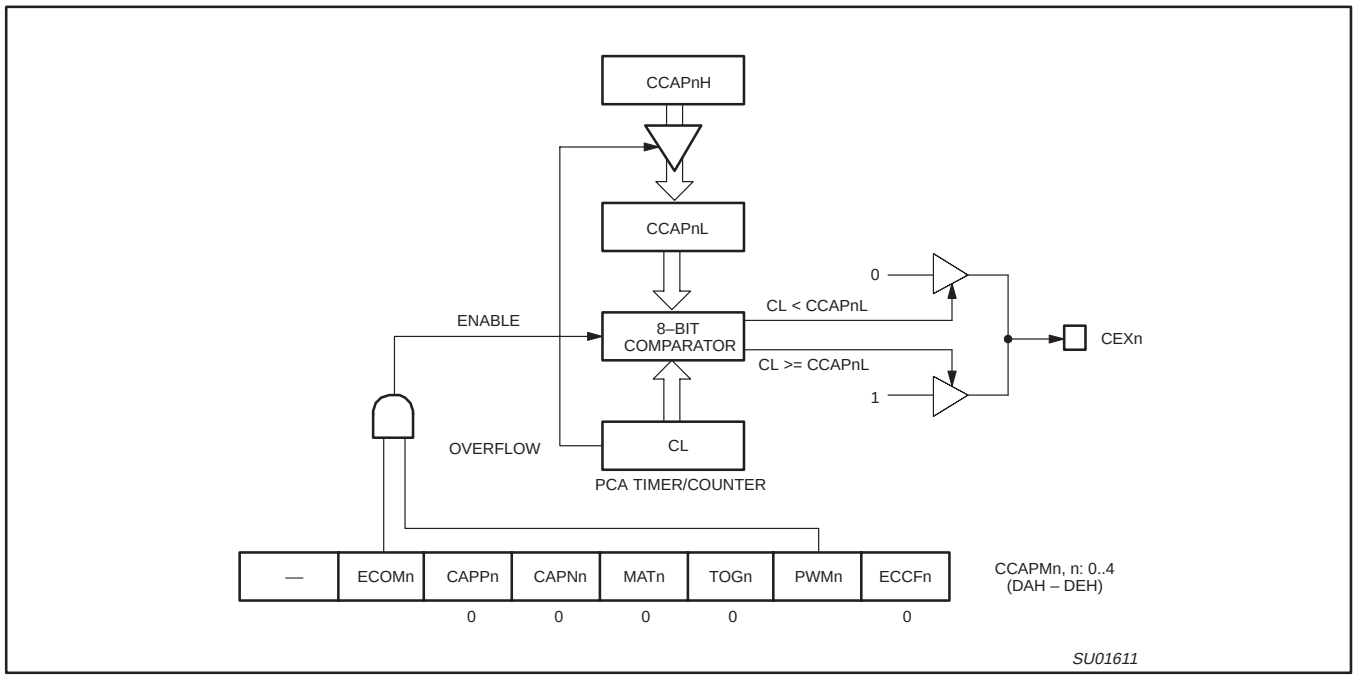

Figure 45. PCA PWM Mode

12. The input threshold voltage of SCL and SDA (SIO1) meets the I^2C specification, so an input voltage below 0.3 V_{DD} will be recognized as a logic 0 while an input voltage above 0.7 V_{DD} will be recognized as a logic 1.
13. Not 100% tested.

AC ELECTRICAL CHARACTERISTICS (6-CLOCK MODE, 5 V ±10% OPERATION)

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C ; V_{CC} = 5 V ±10%, V_{SS} = 0 V[1,2,3,4,5]

Symbol	Figure	Parameter	Limits		16 MHz Clock		Unit
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	55	Oscillator frequency	0	30			MHz
t_{LHLL}	50	ALE pulse width	t_{CLCL}–8		54.5		ns
t_{AVLL}	50	Address valid to ALE LOW	0.5 t_{CLCL} –13		18.25		ns
t_{LLAX}	50	Address hold after ALE LOW	0.5 t_{CLCL} –20		11.25		ns
t_{LLIV}	50	ALE LOW to valid instruction in		2 t_{CLCL} –35		90	ns
t_{LLPL}	50	ALE LOW to $\overline{PSEN}$ LOW	0.5 t_{CLCL} –10		21.25		ns
t_{PLPH}	50	$\overline{PSEN}$ pulse width	1.5 t_{CLCL} –10		83.75		ns
t_{PLIV}	50	$\overline{PSEN}$ LOW to valid instruction in		1.5 t_{CLCL} –35		58.75	ns
t_{PXIX}	50	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	50	Input instruction float after $\overline{PSEN}$		0.5 t_{CLCL} –10		21.25	ns
t_{AVIV}	50	Address to valid instruction in		2.5 t_{CLCL} –35		121.25	ns
t_{PLAZ}	50	$\overline{PSEN}$ LOW to address float		10		10	ns
Data Memory							
t_{RLRH}	51	$\overline{RD}$ pulse width	3 t_{CLCL} –20		167.5		ns
t_{WLWH}	52	$\overline{WR}$ pulse width	3 t_{CLCL} –20		167.5		ns
t_{RLDV}	51	$\overline{RD}$ LOW to valid data in		2.5 t_{CLCL} –35		121.25	ns
t_{RHDX}	51	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	51	Data float after $\overline{RD}$		t_{CLCL} –10		52.5	ns
t_{LLDV}	51	ALE LOW to valid data in		4 t_{CLCL} –35		215	ns
t_{AVDV}	51	Address to valid data in		4.5 t_{CLCL} –35		246.25	ns
t_{LLWL}	51, 52	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	1.5 t_{CLCL} –15	1.5 t_{CLCL} +15	78.75	108.75	ns
t_{AVWL}	51, 52	Address valid to $\overline{WR}$ LOW or $\overline{RD}$ LOW	2 t_{CLCL} –15		110		ns
t_{QVWX}	52	Data valid to $\overline{WR}$ transition	0.5 t_{CLCL} –25		6.25		ns
t_{WHQX}	52	Data hold after $\overline{WR}$	0.5 t_{CLCL} –15		16.25		ns
t_{QVWH}	52	Data valid to $\overline{WR}$ HIGH	3.5 t_{CLCL} –5		213.75		ns
t_{RLAZ}	51	$\overline{RD}$ LOW to address float		0		0	ns
t_{WHLH}	51, 52	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	0.5 t_{CLCL} –10	0.5 t_{CLCL} +10	21.25	41.25	ns
External Clock							
t_{CHCX}	55	High time	0.4 t_{CLCL}	$t_{CLCL} - t_{CLCX}$			ns
t_{CLCX}	55	Low time	0.4 t_{CLCL}	$t_{CLCL} - t_{CHCX}$			ns
t_{CLCH}	55	Rise time		5			ns
t_{CHCL}	55	Fall time		5			ns
Shift register							
t_{XLXL}	54	Serial port clock cycle time	6 t_{CLCL}		375		ns
t_{QVXH}	54	Output data setup to clock rising edge	5 t_{CLCL} –25		287.5		ns
t_{XHQX}	54	Output data hold after clock rising edge	t_{CLCL} –15		47.5		ns
t_{XHDX}	54	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	54	Clock rising edge to input data valid[6]		5 t_{CLCL} –133		179.5	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$=100 pF, load capacitance for all outputs = 80 pF
3. Interfacing the microcontroller to devices with float time up to 45ns is permitted. This limited bus contention will not cause damage to port 0 drivers.
4. Parts are guaranteed by design to operate down to 0 Hz.
5. Data shown in the table are the best mathematical models for the set of measured values obtained in tests. If a particular parameter calculated at a customer specified frequency has a negative value, it should be considered equal to zero.
6. Below 16 MHz this parameter is 4 t_{CLCL} – 133

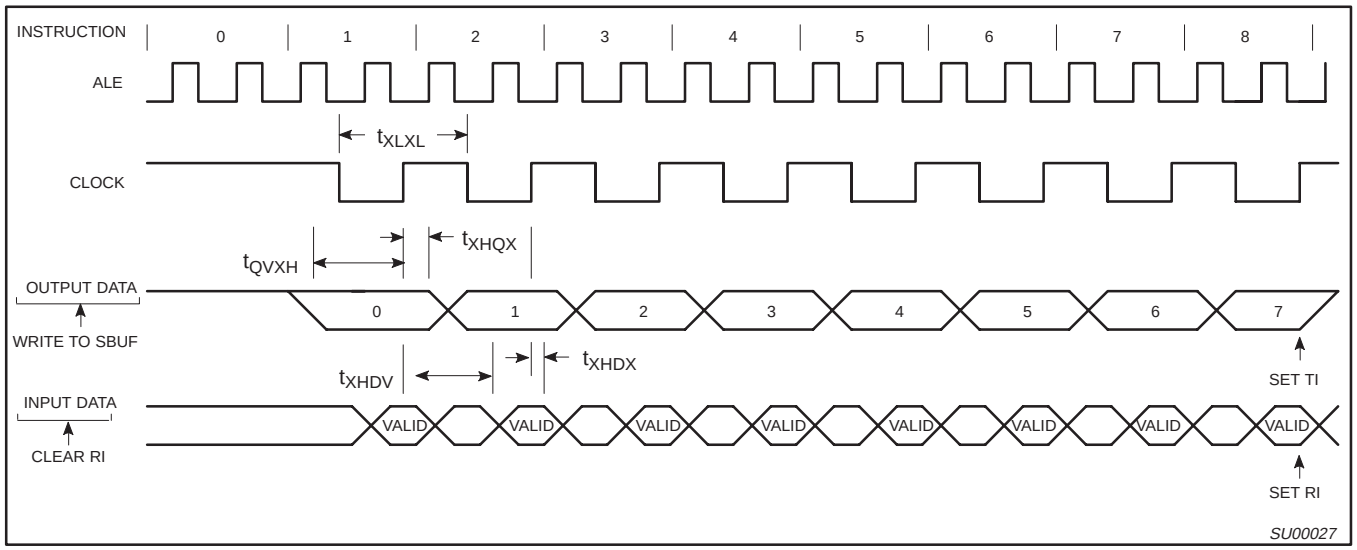

Figure 54. Shift Register Mode Timing

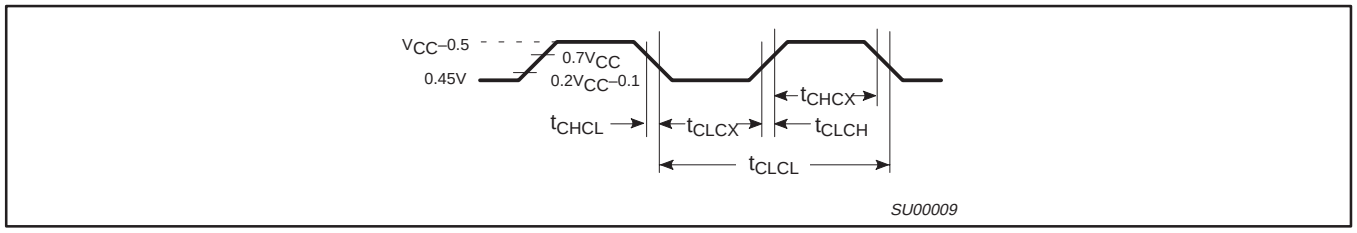

Figure 55. External Clock Drive

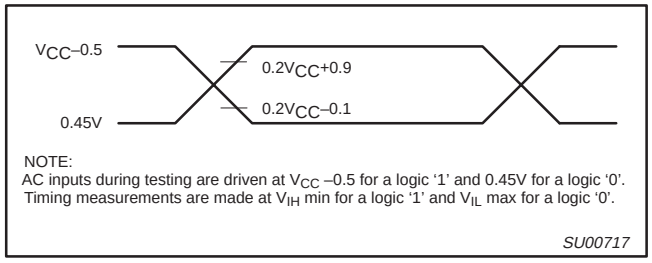

Figure 56. AC Testing Input/Output

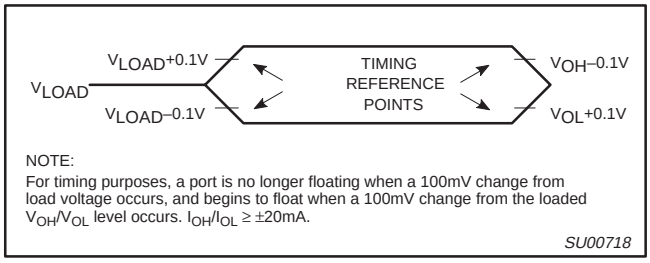

Figure 57. Float Waveform

Table 17. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6	P3.3
Read signature	1	0	1	1	0	0	0	0	X
Program code data	1	0	0*	V_{PP}	1	0	1	1	X
Verify code data	1	0	1	1	0	0	1	1	X
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0	X
Pgm security bit 1	1	0	0*	V_{PP}	1	1	1	1	X
Pgm security bit 2	1	0	0*	V_{PP}	1	1	0	0	X
Pgm security bit 3	1	0	0*	V_{PP}	0	1	0	1	X
Program to 6-clock mode	1	0	0*	V_{PP}	0	0	1	0	0
Verify 6-clock[4]	1	0	1	1	e	0	0	1	1
Verify security bits[5]	1	0	1	1	e	0	1	0	X

NOTES:
1. '0' = Valid LOW for that pin, '1' = valid HIGH for that pin.
2. V_{PP} = 12.75 V ±0.25 V.
3. V_{CC} = 5 V±10% during programming and verification.
4. Bit is output on P0.4 (1 = 12x, 0 = 6x).
5. Security bit one is output on P0.7.
   Security bit two is output on P0.6.
   Security bit three is output on P0.3.

* ALE/$\overline{PROG}$ receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while V_{PP} is held at 12.75 V. Each programming pulse is LOW for 100 µs (±10 µs) and HIGH for a minimum of 10 µs.

Table 18. Program Security Bits for EPROM Devices

PROGRAM LOCK BITS[1, 2]				PROTECTION DESCRIPTION
	SB1	SB2	SB3	
1	U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessible.

NOTES:
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

80C51 8-bit microcontroller family 16 KB OTP/ROM, 512B RAM, low voltage (2.7 to 5.5 V), low power, high speed (30/33 MHz), two 400KB I²C interfaces

P8xC660X2/661X2

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