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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	M16C/60
Core Size	16-Bit
Speed	15MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	20
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306s0fagp-u5

Block Diagram and PLC application Outline

Figure 1.1.1 is a block diagram of the M16C/6S group and PLC application Outline.

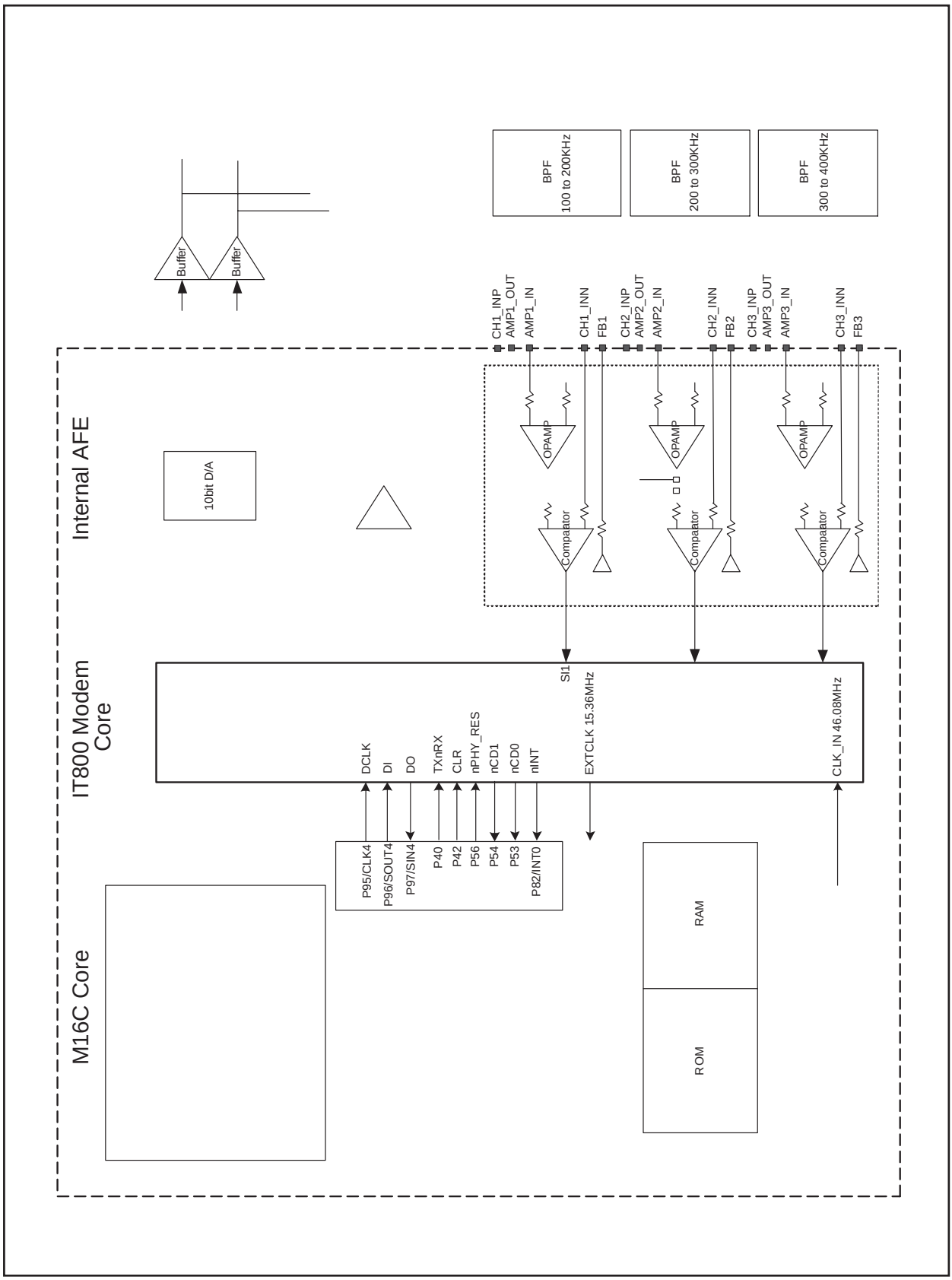
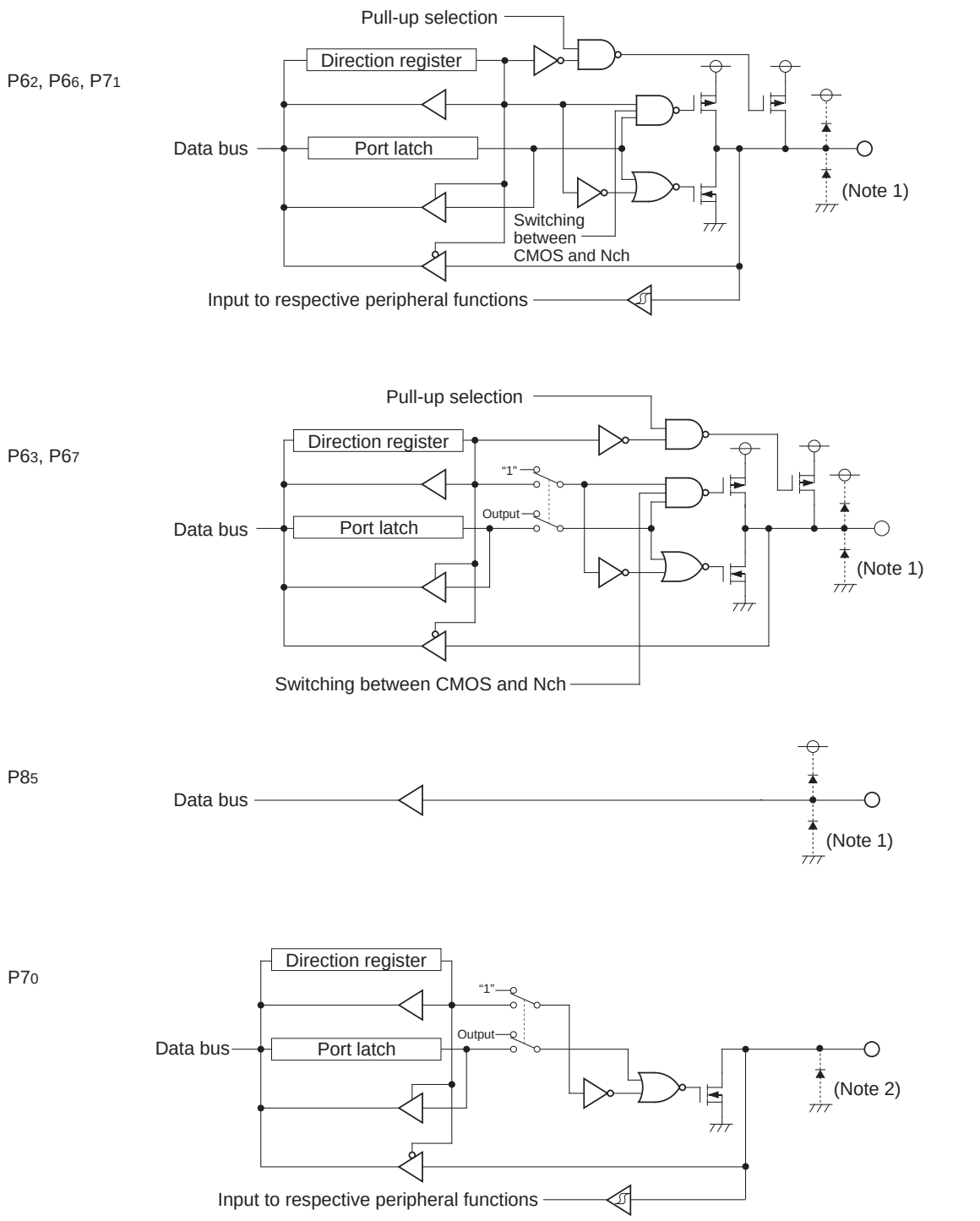


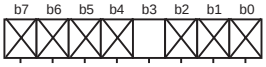
Figure 1.1.1. Block Diagram of Chip and PLC application Outline



Note 1: symbolizes a parasitic diode.
Make sure the input voltage on each port will not exceed Vcc.
Note 2: symbolizes a parasitic diode.

Figure 1.18.3. I/O Ports (3)

Pull-up control register 0 (Note 1)

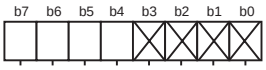


Symbol	Address	After reset
PUR0	$03FC_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
—— (b2-b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
PU03	$P1_4$ to $P1_7$ pull-up	0 : Not pulled high 1 : Pulled high (Note 2)	RW
—— (b7-b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—

Note 1: During memory extension and microprocessor modes, the pins are not pulled high although their corresponding register contents can be modified.
Note 2: The pin for which this bit is "1" (pulled high) and the direction bit is "0" (input mode) is pulled high.

Pull-up control register 1



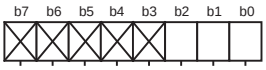
Symbol	Address	After reset(Note 5)
PUR1	$03FD_{16}$	00000000_2 00000010_2

Bit symbol	Bit name	Function	RW
—— (b3-b0)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
PU14	$P6_0$ to $P6_3$ pull-up	0 : Not pulled high 1 : Pulled high (Note 3)	RW
PU15	$P6_4$ to $P6_7$ pull-up		RW
PU16	$P7_2$ to $P7_3$ pull-up (Note 1)		RW
PU17	$P7_4$ to $P7_7$ pull-up		RW

Note 1: The $P7_0$ and $P7_1$ pins do not have pull-ups.
Note 2: During memory extension and microprocessor modes, the pins are not pulled high although the contents of these bits can be modified.
Note 3: The pin for which this bit is "1" (pulled high) and the direction bit is "0" (input mode) is pulled high.
Note 4: If the PM01 to PM00 bits are set to "01_2" (memory expansion mode) or "11_2" (microprocessor mode) in a program during single-chip mode, the PU11 bit becomes "1".
Note 5: The values after hardware reset 1 and 2 are as follows:
- 00000000_2 when input on CNVss pin is "L"
- 00000010_2 when input on CNVss pin is "H"

The values after software reset, watchdog timer reset and oscillation stop detection reset are as follows:
- 00000000_2 when PM 01 to PM00 bits of PM0 register are "00_2" (single-chip mode)
- 00000010_2 when PM 01 to PM00 bits of PM0 register are "01_2" (memory expansion mode) or "11_2" (microprocessor mode)

Pull-up control register 2



Symbol	Address	After reset
PUR2	$03FE_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
PU20	$P8_0$ to $P8_3$ pull-up	0 : Not pulled high 1 : Pulled high (Note 1)	RW
PU21	$P8_4$ to $P8_7$ pull-up (Note 2)		RW
PU22	$P9_0$ to $P9_3$ pull-up		RW
—— (b7-b3)	Nothing is assigned. In an attempt to write to these bits, write "0". The value, if read, turns out to be "0".		—

Note 1: The pin for which this bit is "1" (pulled high) and the direction bit is "0" (input mode) is pulled high.
Note 2: The $P8_5$ pin does not have pull-up.

Figure 1.18.8. PUR0 to PUR2 Registers

Timing Requirements

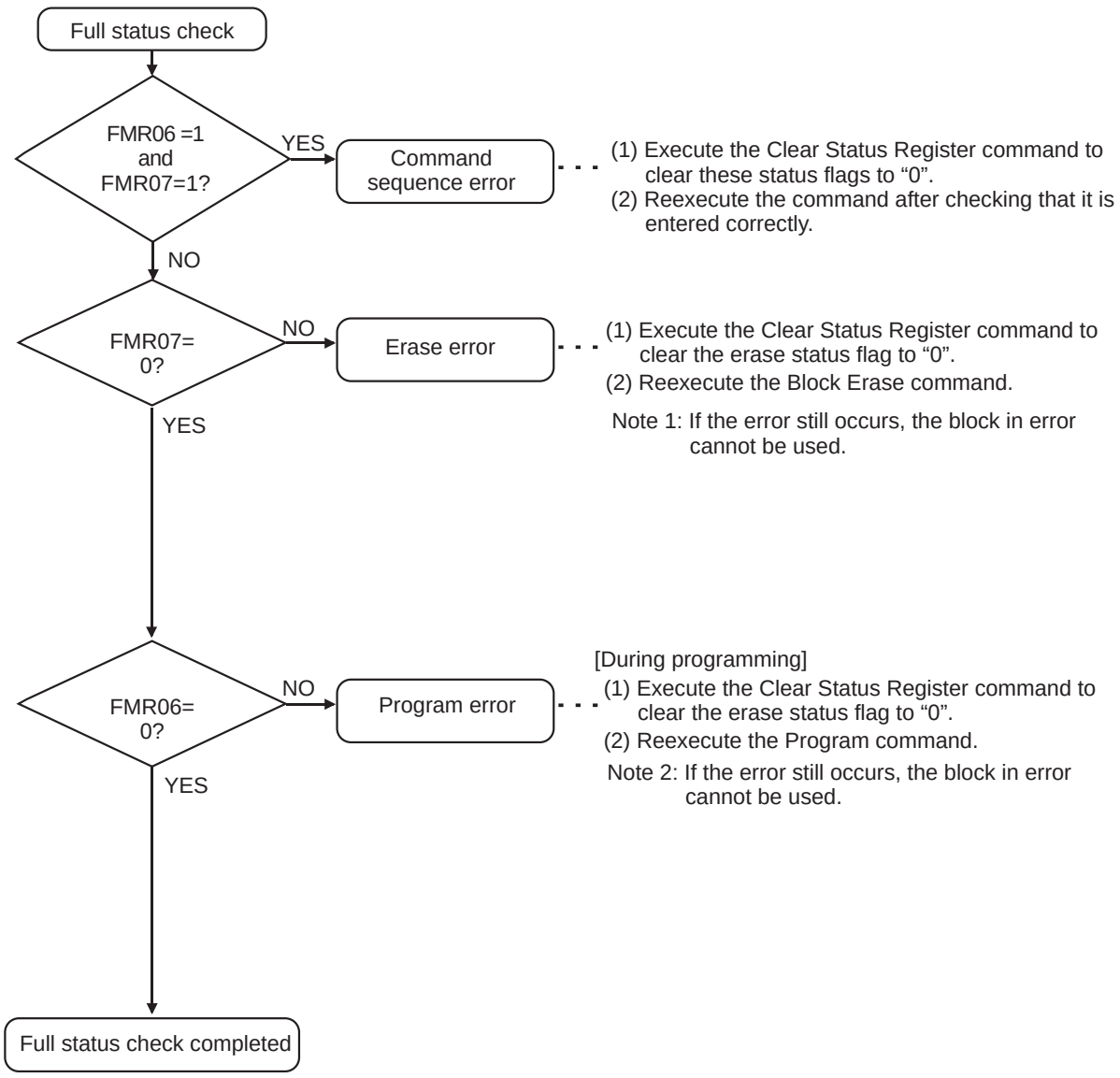
(V_{CC} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C/– 40 to 85°C/– 40 to 105°C unless otherwise specified)

Table 1.19.15. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	100		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.19.16. External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns



Note 3: If FMR06 or FMR07 = 1, neither the Program nor Block Erase command is accepted. Execute the Clear Status Register command before executing those commands.

Figure 1.21.6. Full Status Check and Handling Procedure for Each Error

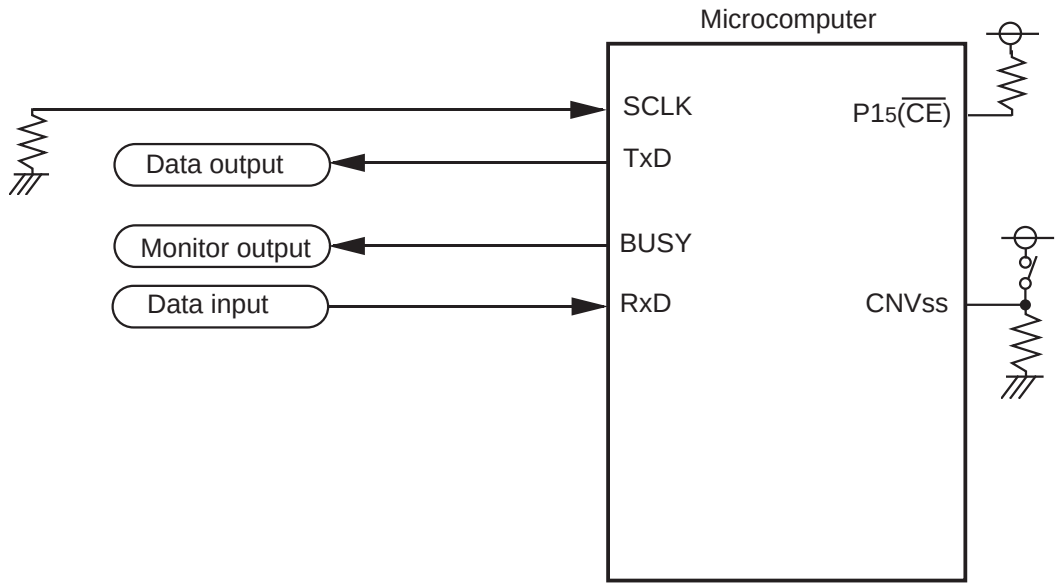
ID Code Check Function (D-version only, see Table 1.1.4 for D-version)

The ID code of “ALeRASE” in ASCII code is used for forced erase function. The ID code of “Protect” in ASCII code is used for standard serial I/O mode disable function. Table 1.22.1 lists Reserved Word of ID Code. All ID code storage addresses and data must match the combinations listed in Table 1.22.1. When the forced erase function or standard serial I/O mode disable function is not used, use another combination of ID codes.

Table 1.22.1. Reserved Word of ID Code

ID Code Storage Address		Reserved word of ID Code (ASCII)	
		ALeRASE	Protect
FFFDFh	ID1	41h (upper-case A)	50h (upper-case P)
FFFE3h	ID2	4Ch (upper-case L)	72h (lower-case r)
FFFEBh	ID3	65h (lower-case e)	6Fh (lower-case o)
FFFEFh	ID4	52h (upper-case R)	74h (lower-case t)
FFFF3h	ID5	41h (upper-case A)	65h (lower-case e)
FFFF7h	ID6	53h (upper-case S)	63h (lower-case c)
FFFFBh	ID7	45h (upper-case E)	74h (lower-case t)

All ID code storage addresses and data must match the combinations listed in Table 1.22.1.



(1) In this example, modes are switched between single-chip mode and standard serial input/output mode by controlling the CNVss input with a switch.

Figure 1.22.2. Circuit Application in Standard Serial I/o Mode 2

About DAC (Digital to Analog Converter)

DAC of built-in in M16C/6S is current output type 10 bit DAC. The standard level of output current can be set up by the external resistance linked to a built-in standard power supply. A DAC circuit and a load circuit are shown in Figure 1.23.2. The typical characteristic is shown in Table 1.23.1.

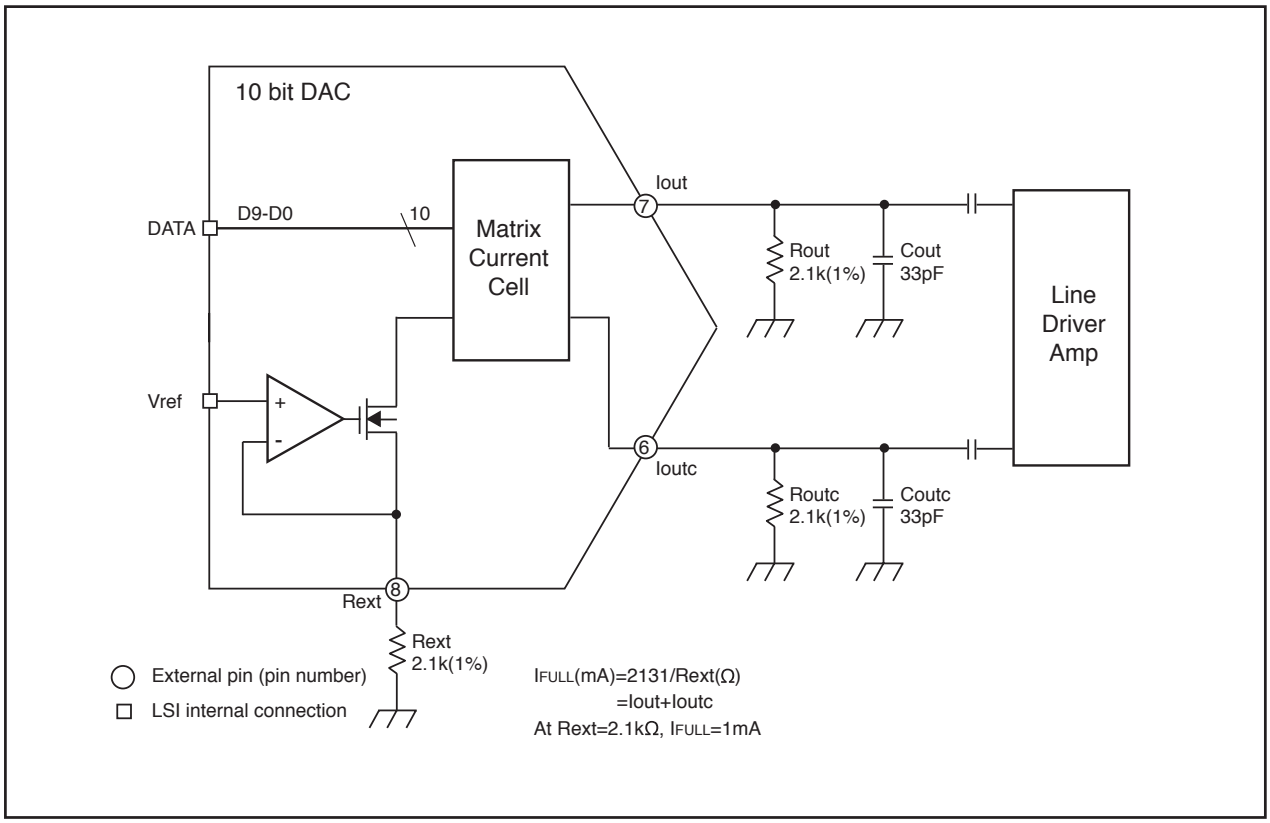


Figure 1.23.2 DAC (Digital to Analog Converter)

Table 1.23.1 DAC Electrical Characteristics (Vdd=3.3±0.3V, Ta = -20 to 85°C/-40 to 85°C/-40 to 105°C unless otherwise specified)

Parameter	Symbol	Condition	Electrical Characteristics			Unit
			Min	Typ	Max	
Standard voltage	Vref	Rext=2.1kΩ		0.3		V
Standard current	Iref	Rext=2.1kΩ		0.14		mA
External standard register	Rext			2.1		kΩ
DAC output register	Rout/Routc	Rext=2.1kΩ			2.0	kΩ
Full-scale current	IFULL	Rext=2.1kΩ	0.9	1	1.1	mA
Maximum output voltage	Voutmax	Rout/Routc=2.1kΩ			Vdd-1	V

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.