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#### Understanding Embedded - PLDs (Programmable Logic Devices)

Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

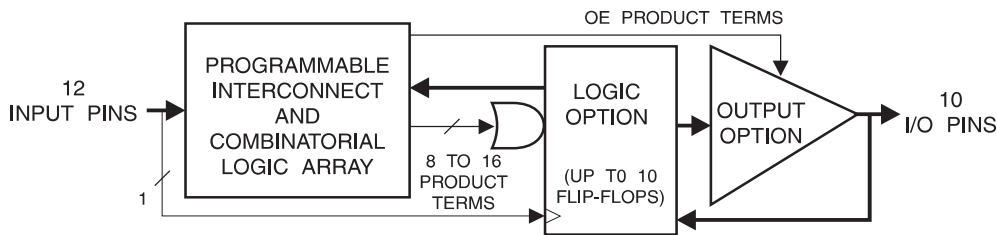
#### Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

#### Details

Product Status	Obsolete
Programmable Type	EE PLD
Number of Macrocells	10
Voltage - Input	5V
Speed	15 ns
Mounting Type	Through Hole
Package / Case	24-DIP (0.300", 7.62mm)
Supplier Device Package	24-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf22v10c-15pc">https://www.e-xfl.com/product-detail/microchip-technology/atf22v10c-15pc</a>

**Figure 1-1. Logic Diagram**

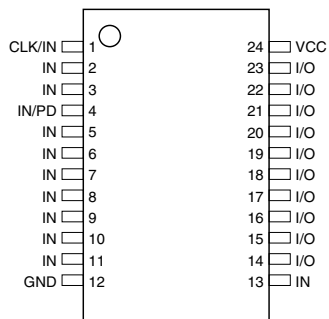


## 2. Pin Configurations

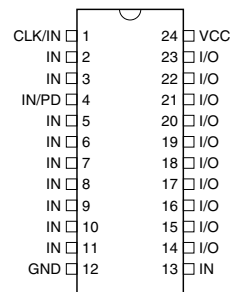
**Table 2-1. Pin Configurations (All Pinouts Top View)**

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
GND	Ground
VCC	+5V Supply
PD	Power-down

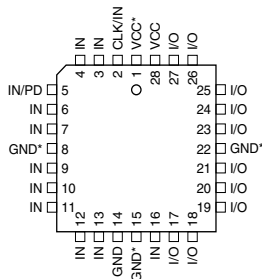
**Figure 2-1. TSSOP**



**Figure 2-2. DIP/SOIC**



**Figure 2-3. PLCC/LCC**



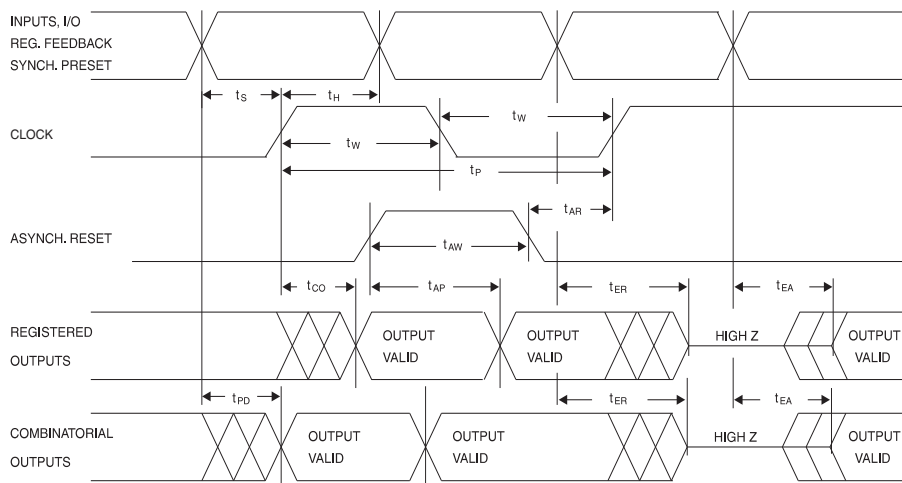
Note: For all PLCCs (except "-5"), pins 1, 8, 15 and 22 can be left unconnected. However, if they are connected, superior performance will be achieved

## 4.1 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units	
$I_{IL}$	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL} \text{ (Max)}$			-10.0	$\mu\text{A}$	
$I_{IH}$	Input or I/O High Leakage Current	$3.5 \leq V_{IN} \leq V_{CC}$			10.0	$\mu\text{A}$	
$I_{CC}$	Power Supply Current, Standby	$V_{CC} = \text{Max},$ $V_{IN} = \text{Max},$ Outputs Open	C-5, 7, 10	Com.	85.0	130.0	mA
			C-10	Ind.	90.0	140.0	mA
			C-15	Ind.	65.0	115.0	mA
			CQ-15	Ind.	35.0	70.0	mA
$I_{CC2}$	Clocked Power Supply Current	$V_{CC} = \text{Max},$ Outputs Open, $f = 15\text{MHz}$	C-5, 7, 10	Com.		150.0	mA
			C-10	Ind., Mil.		160.0	mA
			C-15	Ind.	70.0	125	mA
			C-15	Mil.		160.0	mA
$I_{PD}$	Power Supply Current, PD Mode	$V_{CC} = \text{Max}$	Com.	10.0	500.0	$\mu\text{A}$	
		$V_{IN} = 0, \text{Max}$	Ind.	10.0	650.0	$\mu\text{A}$	
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5\text{V}$			-130.0	mA	
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		2.0		$V_{CC}+0.75$	V	
$V_{OL}$	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = \text{Min}$	$I_{OL} = 16\text{mA}$	Com., Ind.		0.5	V
			$I_{OL} = 12\text{mA}$	Mil.		0.5	V
$V_{OH}$	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = \text{Min}$	$I_{OH} = -4.0\text{mA}$		2.4		V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec

## 4.2 AC Waveforms <sup>(1)</sup>



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified

## 4.3 AC Characteristics<sup>(1)</sup>

Symbol	Parameter	-5		-7		-10		-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD</sub>	Input or Feedback to Combinatorial Output	1.0	5.0	3.0	7.5	3.0	10.0	3.0	15.0	ns
t <sub>CO</sub>	Clock to Output	1.0	4.0	2.0	4.5 <sup>(2)</sup>	2.0	6.5	2.0	8.0	ns
t <sub>CF</sub>	Clock to Feedback		2.5		2.5		2.5		2.5	ns
t <sub>S</sub>	Input or Feedback Setup Time	3.0		3.5		4.5		10.0		ns
t <sub>H</sub>	Hold Time	0		0		0		0		ns
f <sub>MAX</sub>	External Feedback 1/(t <sub>S</sub> + t <sub>CO</sub> )	142.0		125.0 <sup>(3)</sup>		90.0		55.5		MHz
	Internal Feedback 1/(t <sub>S</sub> + t <sub>CF</sub> )	166.0		142.0		117.0		80.0		MHz
	No Feedback 1/(t <sub>WH</sub> + t <sub>WL</sub> )	166.0		166.0		125.0		83.3		MHz
t <sub>W</sub>	Clock Width (t <sub>WL</sub> and t <sub>WH</sub> )	3.0		3.0		3.0		6.0		ns
t <sub>EA</sub>	Input or I/O to Output Enable	2.0	6.0	3.0	7.5	3.0	10.0	3.0	15.0	ns
t <sub>ER</sub>	Input or I/O to Output Disable	2.0	5.0	3.0	7.5	3.0	9.0	3.0	15.0	ns
t <sub>AP</sub>	Input or I/O to Asynchronous Reset of Register	3.0	7.0	3.0	10.0	3.0	12.0	3.0	20.0	ns
t <sub>AW</sub>	Asynchronous Reset Width	5.5		7.0		8.0			15.0	ns
t <sub>AR</sub>	Asynchronous Reset Recovery Time	4.0		5.0		6.0			10.0	ns
t <sub>SP</sub>	Setup Time, Synchronous Preset	4.0		4.5		6.0			10.0	ns
t <sub>SPR</sub>	Synchronous Preset to Clock Recovery Time	4.0		5.0		8.0			10.0	ns

- Notes:
1. See ordering information for valid part numbers
  2. 5.5ns for DIP package devices
  3. 111MHz for DIP package devices

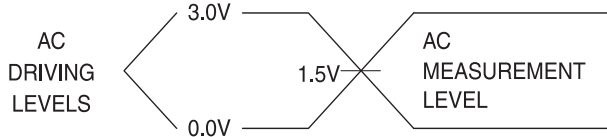
## 4.4 Power-down AC Characteristics<sup>(1)(2)(3)</sup>

Symbol	Parameter	-5		-7		-10		-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IVDH}$	Valid Input before PD High	5.0		7.5		10.0		15.0		ns
$t_{GVDH}$	Valid $\overline{OE}$ before PD High	0		0		0		0		ns
$t_{CVDH}$	Valid Clock before PD High	0		0		0				ns
$t_{DHIX}$	Input Don't Care after PD High		5.0		7.0		10.0		15.0	ns
$t_{DHGX}$	$\overline{OE}$ Don't Care after PD High		5.0		7.0		10.0		15.0	ns
$t_{DHXC}$	Clock Don't Care after PD High		5.0		7.0		10.0		15.0	ns
$t_{DLIV}$	PD Low to Valid Input		5.0		7.5		10.0		15.0	ns
$t_{DLGV}$	PD Low to Valid $\overline{OE}$		15.0		20.0		25.0		30.0	ns
$t_{DLCV}$	PD Low to Valid Clock		15.0		20.0		25.0		30.0	ns
$t_{DLOV}$	PD Low to Valid Output		20.0		25.0		30.0		35.0	ns

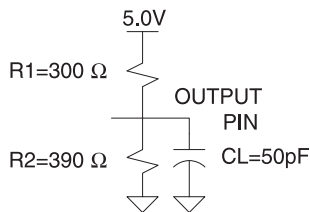
- Notes:
1. Output data is latched and held
  2. High-Z outputs remain high-Z
  3. Clock and input transitions are ignored

## 4.5 Input Test Waveforms

### 4.5.1 Input Test Waveforms and Measurement Levels



### 4.5.2 Commercial Output Test Loads



## 4.6 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1MHz, T = 25°C<sup>(1)</sup>)

	Typ	Max	Units	Conditions
$C_{IN}$	5	8	pF	$V_{IN} = 0V$
$C_{OUT}$	6	8	pF	$V_{OUT} = 0V$

- Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested

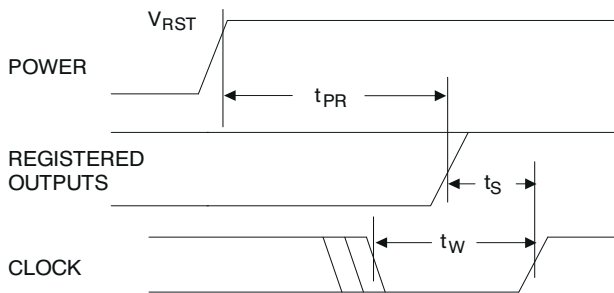
## 4.7 Power-up Reset

The registers in the Atmel® ATF22V10Cs are designed to reset during power-up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic, and starts below 0.7V
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high
3. The clock must remain stable during  $t_{PR}$

**Figure 4-1.** Power-up Reset Timing



## 4.8 Preload of Registered Outputs

The ATF22V10C registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

## 5. Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

## 6. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

## 7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See “CMOS PLD Programming Hardware and Software Support” for information on software/programming.

**Table 7-1.** Programming/Erasing

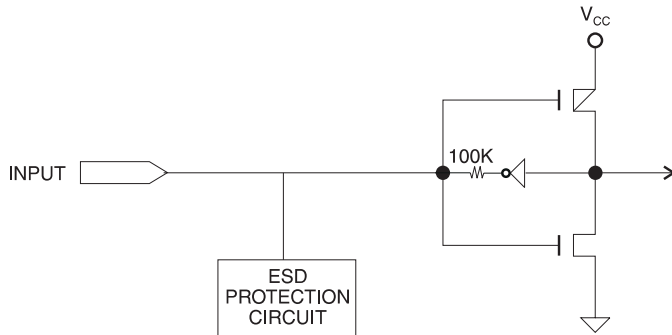
Parameter	Description	Typ	Max	Units
$t_{PR}$	Power-up Reset Time	600	1,000	ns
$V_{RST}$	Power-up Reset Voltage	3.8	4.5	V

## 8. Input and I/O Pin-keeper Circuits

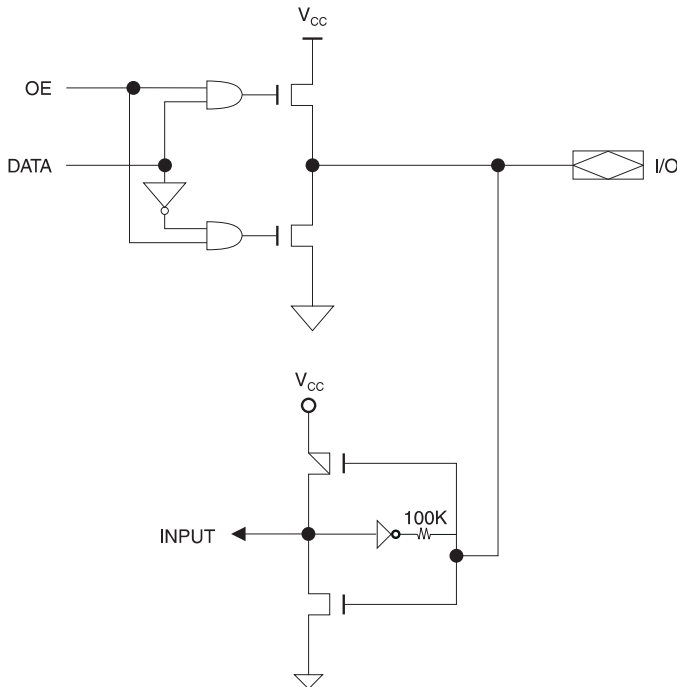
The Atmel® ATF22V10C contains internal input and I/O pin-keeper circuits. These circuits allow each ATF22V10C pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps to ensure that all logic array inputs are at known valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40µA.

**Figure 8-1.** Input Diagram



**Figure 8-2.** I/O Diagram



## 9. Power-down Mode

The Atmel® ATF22V10C includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin (Pin 4 on the DIP/SOIC packages and Pin 5 on the PLCC package). When the PD pin is high, the device supply current is reduced to less than 100mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in an undetermined state at the onset of power-down will remain at the same state. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

PD pin configuration is controlled by the design file, and appears as a separate fuse bit in the JEDEC file. When the power-down feature is not specified in the design file, the IN/PD pin will be configured as a regular logic input.

Note: Some programmers list the 22V10 JEDEC compatible 22V10C (no PD used) separately from the non-22V10 JEDEC compatible 22V10CEX (with PD used)

## 10. Compiler Mode Selection

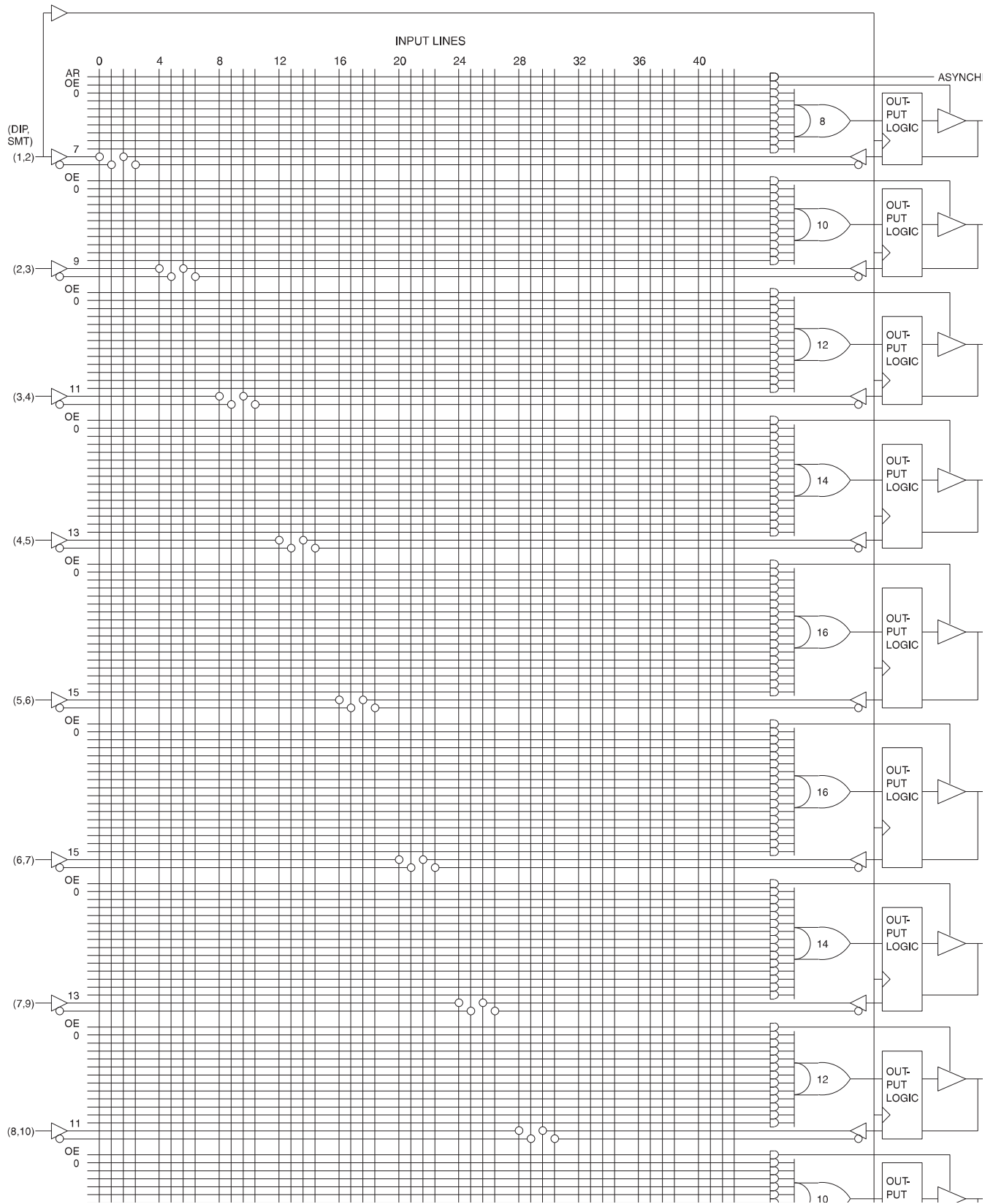
**Table 10-1.** Compiler Mode Selection

	<b>PAL Mode (5828 Fuses)</b>	<b>GAL Mode (5892 Fuses)</b>	<b>Power-down Mode<sup>(1)</sup> (5893 Fuses)</b>
Synario	ATF22V10C (DIP) ATF22V10C (PLCC)	ATTF22V10C DIP (UES) ATF22C10C PLCC (UES)	ATF22V10C DIP (PWD) ATF22V10C PLCC (PWD)
WINCUPPL	P22V10 P22V10LCC	G22V10 G22V10LCC	G22V10CP G22V10CPLCC

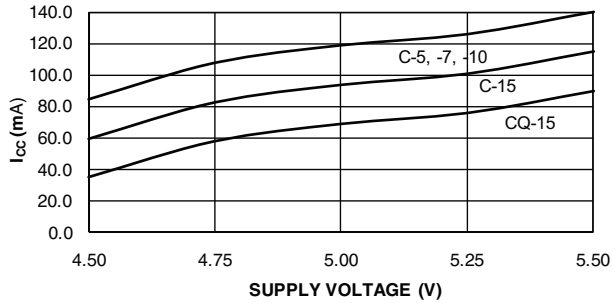
Note: 1. These device types will create a JEDEC file which when programmed in Atmel ATF22V10C devices will enable the power-down mode feature. All other device types have the feature disabled



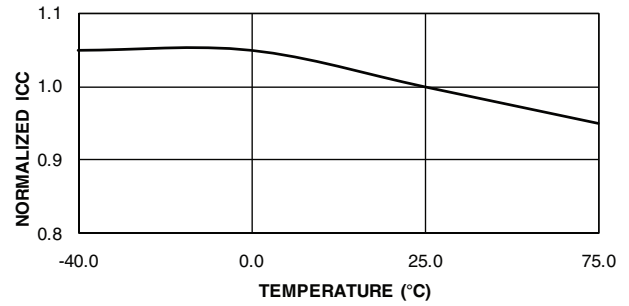
# 11. Functional Logic Diagram



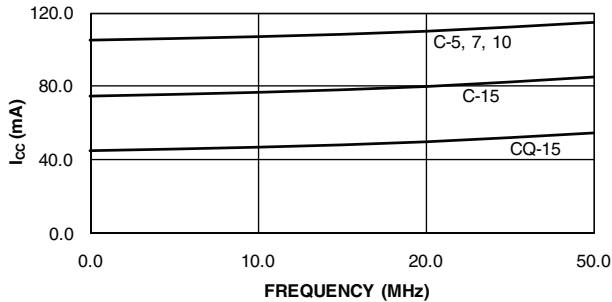
**ATMEL ATF22V10C/CQ SUPPLY CURRENT VS. SUPPLY VOLTAGE ( $T_A = 25^\circ\text{C}$ )**



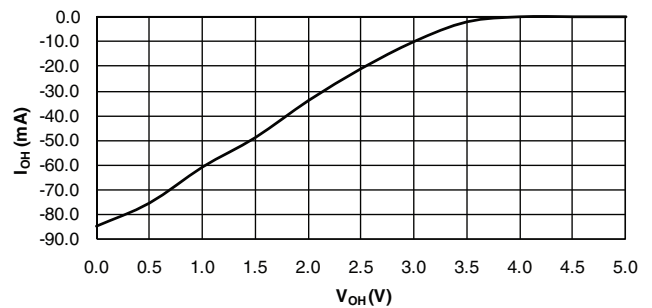
**ATMEL ATF22V10C/CQ NORMALIZED  $I_{CC}$  VS. TEMPERATURE**



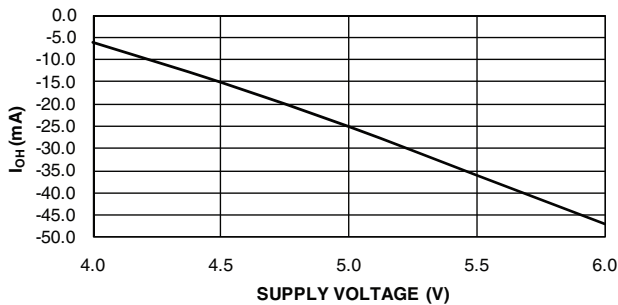
**ATMEL ATF22V10C/CQ SUPPLY CURRENT VS. INPUT FREQUENCY ( $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ )**



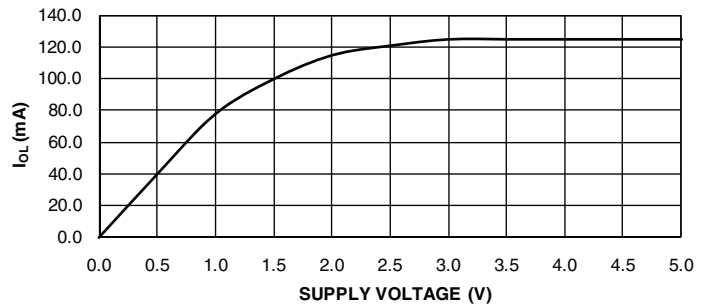
**ATMEL ATF22V10C/CQ OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE ( $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ )**



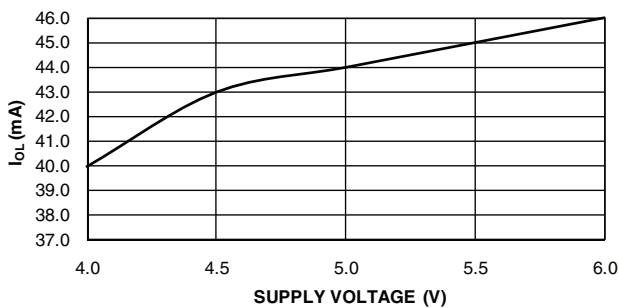
**ATMEL ATF22V10C/CQ OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE ( $V_{OH} = 2.4\text{V}$ )**



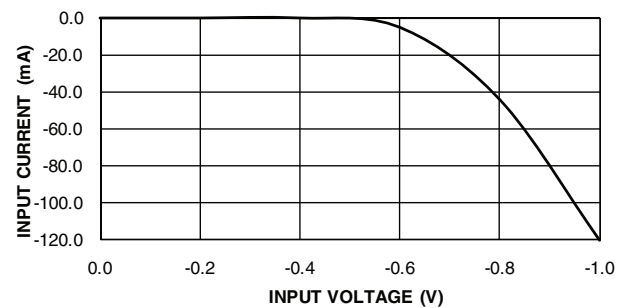
**ATMEL ATF22V10C/CQ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ( $V_{OL} = 0.5\text{V}$ )**

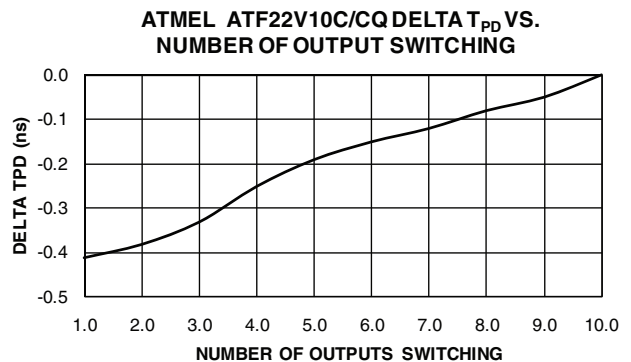
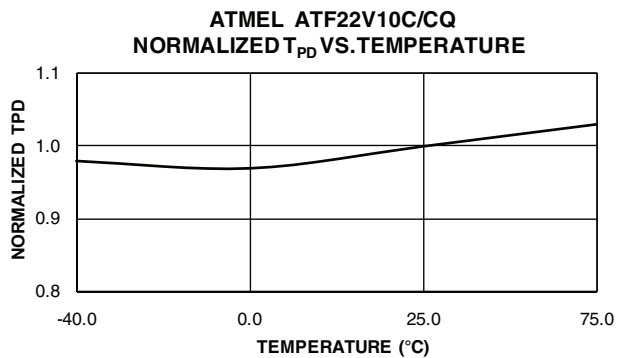
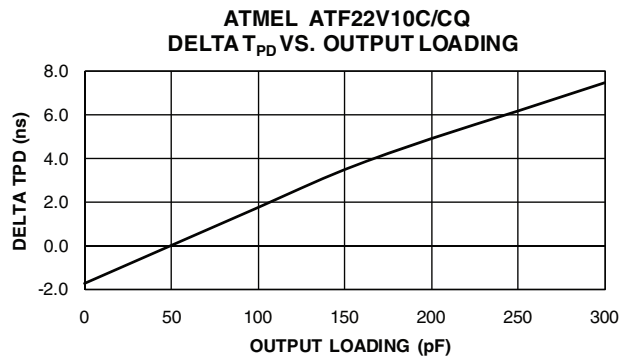
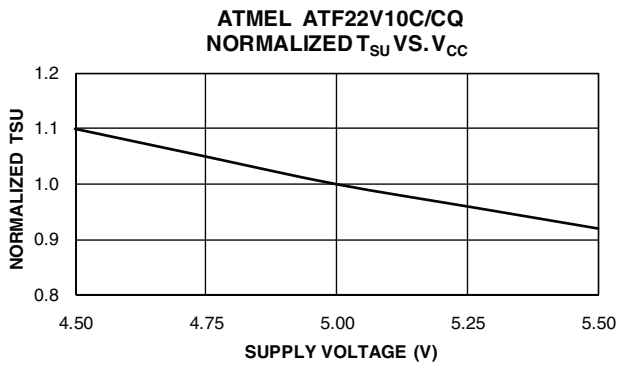
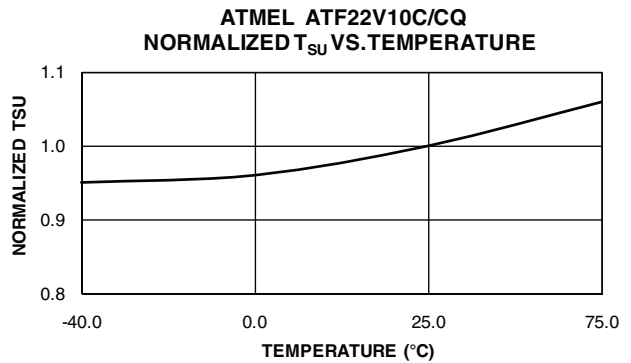
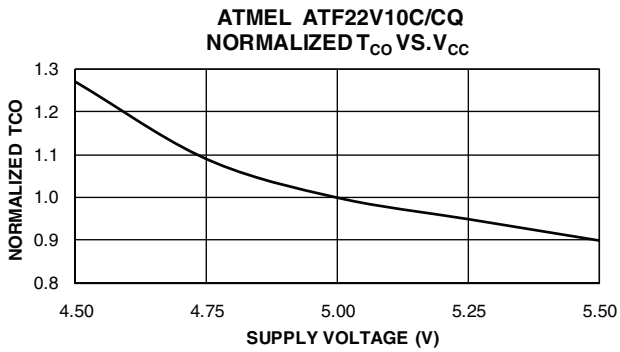
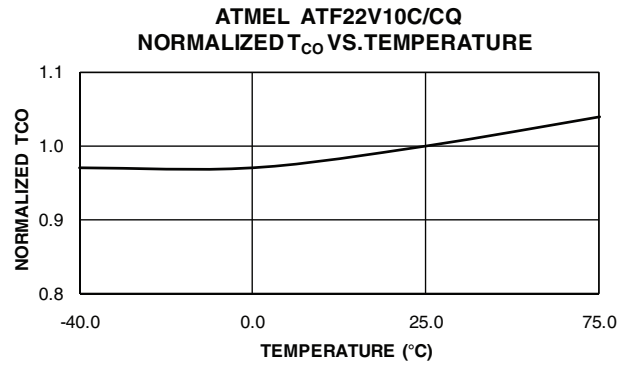
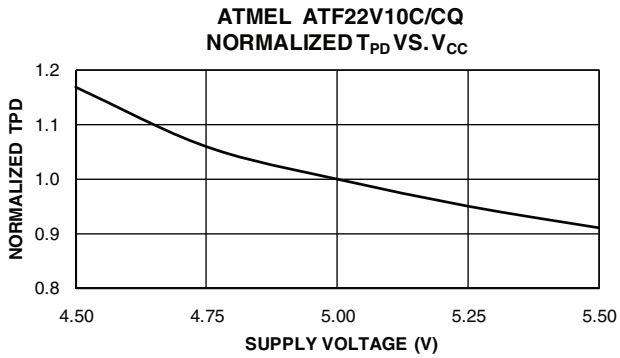


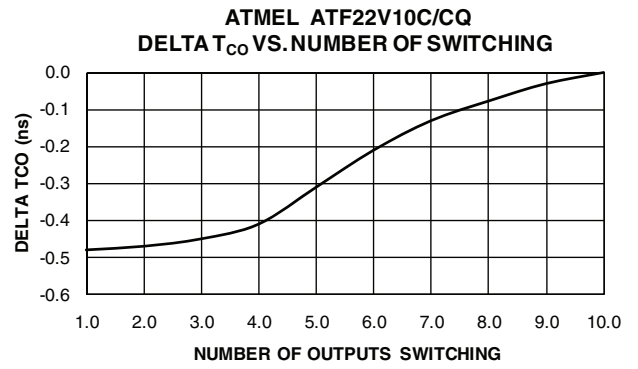
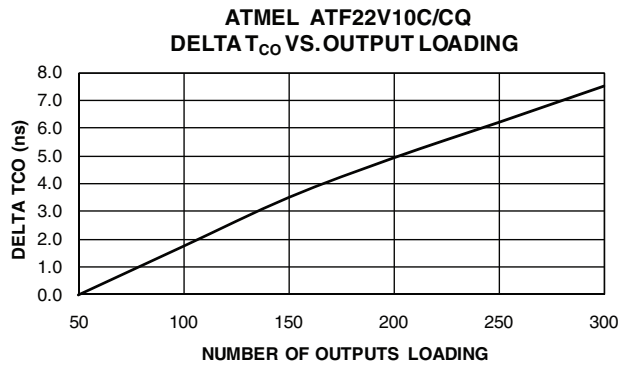
**ATMEL ATF22V10C/CQ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ( $V_{OL} = 0.5\text{V}$ )**



**ATMEL ATF22V10C/CQ INPUT CLAMP CURRENT VS. INPUT VOLTAGE ( $V_{CC} = 5\text{V}, T_A = 35^\circ\text{C}$ )**







## 12. Ordering Information

### 12.1 Atmel ATF22V10C(Q) Green Package Options (Pb/Halide-free/RoHS Compliant)

t <sub>PD</sub> (ns)	t <sub>S</sub> (ns)	t <sub>CO</sub> (ns)	Ordering Code	Package	Operation Range
5	3	4	ATF22V10C-5JX	28J	Commercial (0°C to 70°C)
7.5	3.5	4.5	ATF22V10C-7PX	24P3	Commercial (0°C to 70°C)
			ATF22V10C-7SX	24S	
7.5	3.5	4.5	ATF22V10C-7JU	28J	Industrial (-40°C to 85°C)
10	4.5	6.5	ATF22V10C-10JU	28J	Industrial (-40°C to 85°C)
			ATF22V10C-10PU	24P3	
			ATF22V10C-10SU	24S	
			ATF22V10C-10XU	24X	
15	10	8	ATF22V10C-15JU	28J	Industrial (-40°C to 85°C)
			ATF22V10C-15PU	24P3	
			ATF22V10CQ-15JU	28J	Industrial (-40°C to 85°C)

### 12.2 Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down-grade one speed grade from the industrial-grade to the commercial-grade device (e.g. 7ns PX = 10ns PU) and de-rate power by 30%.

### 12.3 Military Package Options (Lead-based)<sup>(1)</sup>

t <sub>PD</sub> (ns)	t <sub>S</sub> (ns)	t <sub>CO</sub> (ns)	Ordering Code	Package	Operation Range
10	4.5	6.5	ATF22V10C-10GM/883	24D3	Military (-55°C to 125°C) Class B, Fully Compliant
			ATF22V10C-10NM/883	28L	
			5962-8984116LA	24D3	
			5962-89841163A	28L	
15	10	8	ATF22V10C-15GM/883	24D3	Military (-55°C to 125°C) Class B, Fully Compliant
			ATF22V10C-15NM/883	28L	
			5962-8984115LA	24D3	
			5962-89841153A	28L	

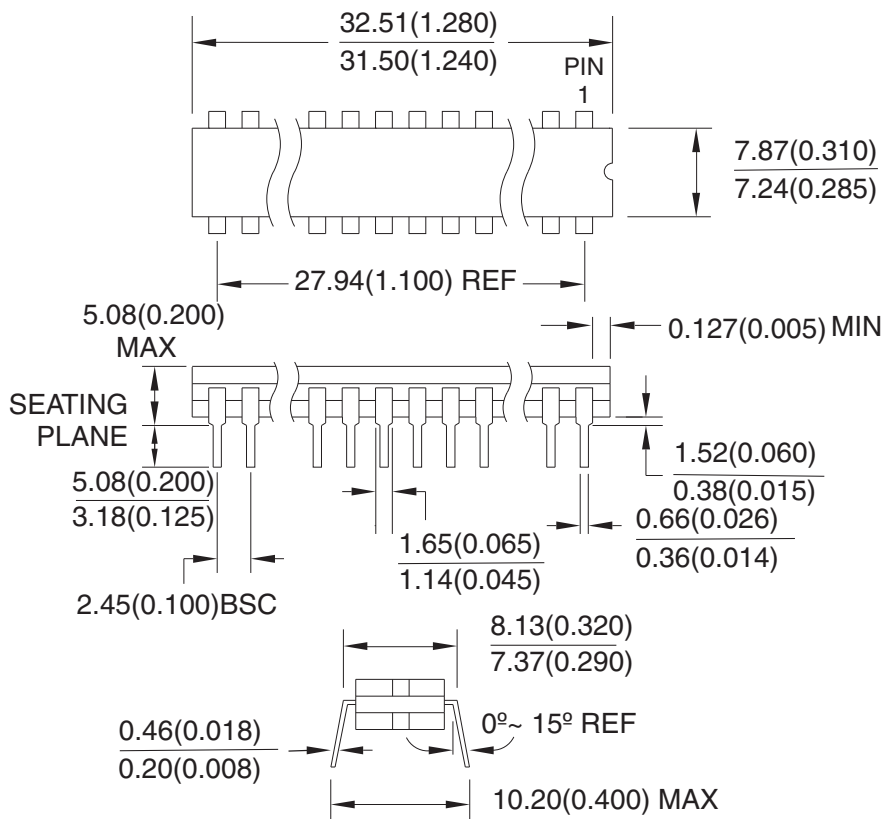
Notes: 1. Military/DSCC parts meet the DSCC drawing specifications

Package Type	
<b>24D3</b>	24-lead, 0.300" Wide, Non-windowed Ceramic Dual Inline Package (CERDIP)
<b>24P3</b>	24-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>24S</b>	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
<b>24X</b>	24-lead, 4.4mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
<b>28J</b>	28-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>28L</b>	28-lead, Ceramic Leadless Chip Carrier (LCC)


13. Packaging Information

13.1 24D3 – CERDIP

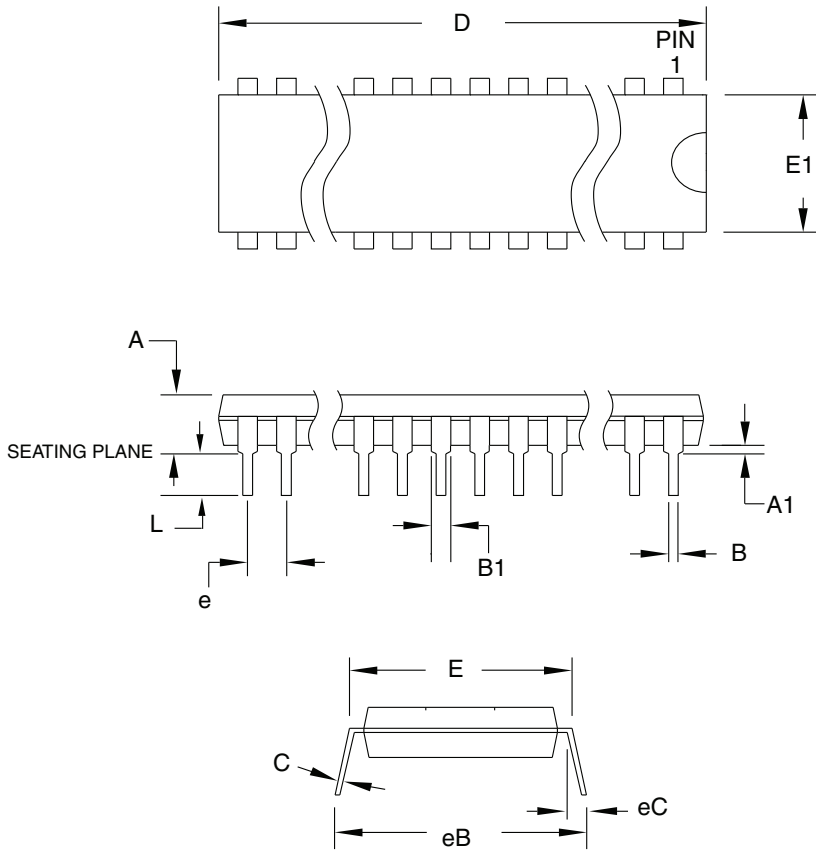
Dimensions in Millimeters and (Inches).  
 Controlling dimension: Inches.  
 MIL-STD 1835 D-9 Config A (Glass Sealed)



10/21/03

 <b>Package Drawing Contact:</b> packagedrawings@atmel.com	<b>TITLE</b> 24D3, 24-lead, 0.300" Wide. Non-windowed, Ceramic Dual Inline Package (Cerdip)	<b>DRAWING NO.</b> 24D3	<b>REV.</b> B

### 13.2 24P3 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	31.623	–	32.131	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.651	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-001, Variation AF
  2. Dimensions D and E1 do not include mold Flash or Protrusion  
Mold Flash or Protrusion shall not exceed 0.25mm (0.010")

6/1/04



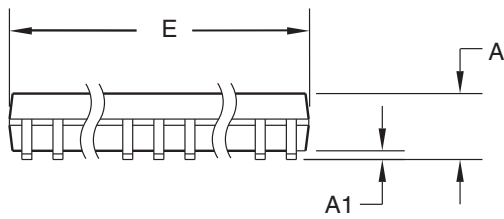
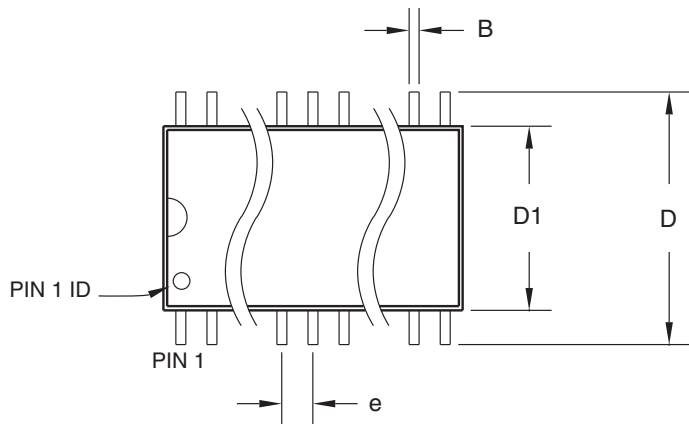
**Package Drawing Contact:**  
packagedrawings@atmel.com

**TITLE**  
**24P3**, 24-lead (0.300"/7.62mm Wide) Plastic Dual  
Inline Package (PDIP)

**DRAWING NO.**  
24P3

**REV.**  
D

## 13.3 24S – SOIC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	2.65	
A1	0.10	–	0.30	
D	10.00	–	10.65	
D1	7.40	–	7.60	
E	15.20	–	15.60	
B	0.33	–	0.51	
L	0.40	–	1.27	
L1	0.23	–	0.32	
e	1.27 BSC			

06/17/2002



**Package Drawing Contact:**  
packagedrawings@atmel.com

**TITLE**  
24S, 24-lead (0.300" body) Plastic Gull Wing Small  
Outline (SOIC)

**DRAWING NO.**

24S

**REV.**

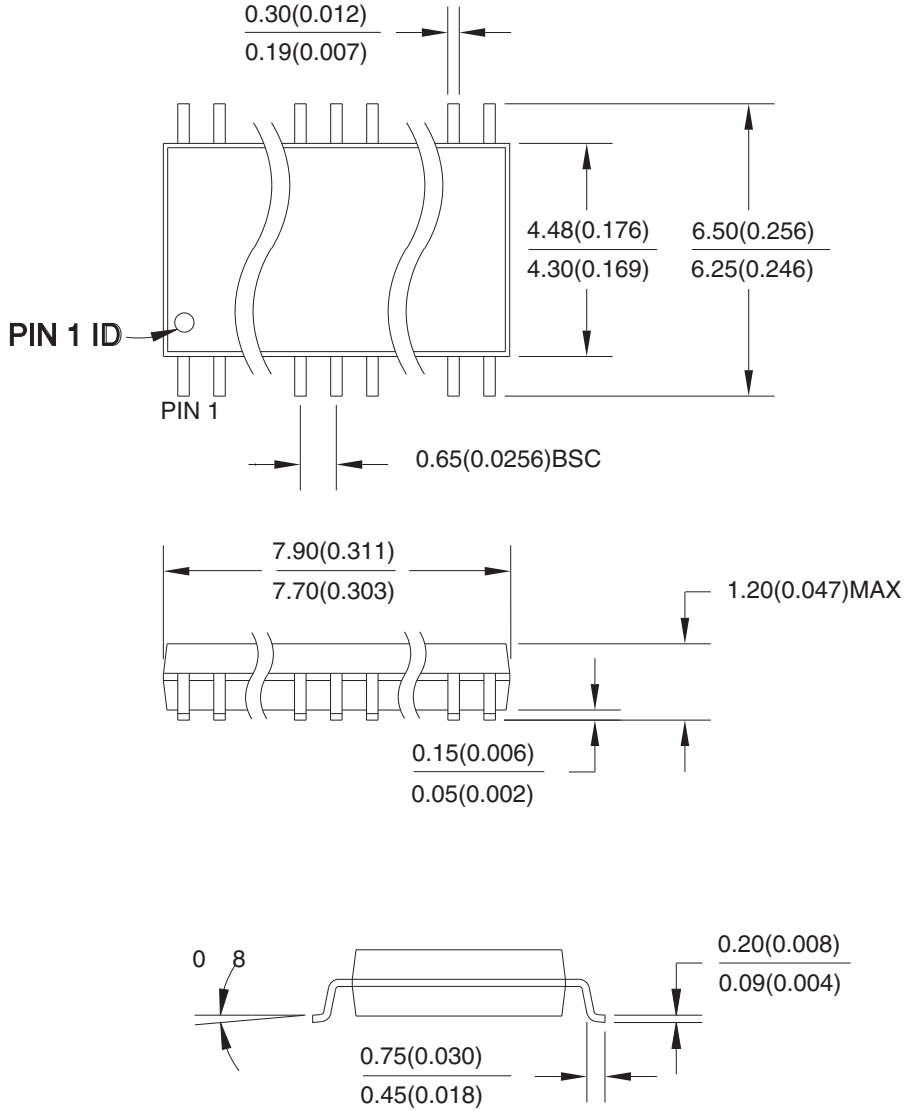
B





### 13.4 24X – TSSOP

Dimensions in Millimeter and (Inches)\*  
 JEDEC STANDARD MO-153 AD  
 Controlling dimension: millimeters



04/11/2001



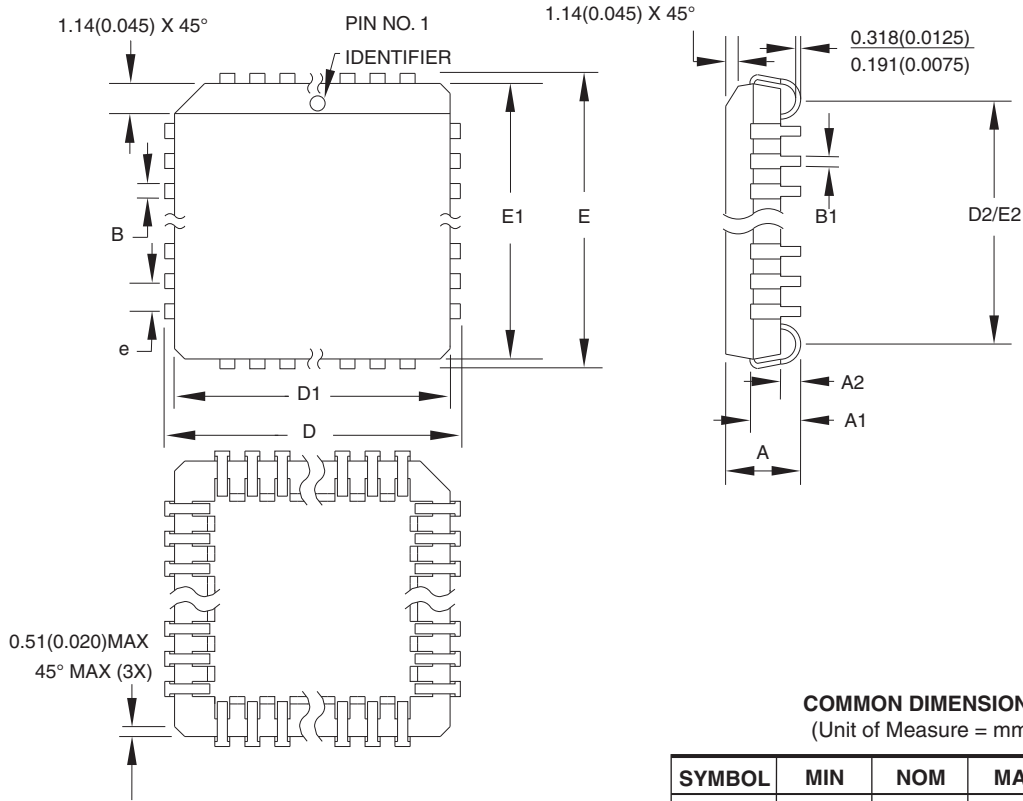
**Package Drawing Contact:**  
 packagedrawings@atmel.com

**TITLE**  
 24X, 24-lead (4.4mm body width) Plastic Thin Shrink  
 Small Outline Package (TSSOP)

**DRAWING NO.**  
 24X

**REV.**  
 A

## 13.5 28J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	12.319	–	12.573	
D1	11.430	–	11.582	Note 2
E	12.319	–	12.573	
E1	11.430	–	11.582	Note 2
D2/E2	9.906	–	10.922	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB
  2. Dimensions D1 and E1 do not include mold protrusion  
Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line
  3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01



**Package Drawing Contact:**  
packagedrawings@atmel.com

**TITLE**

**28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)**

**DRAWING NO.**

28J

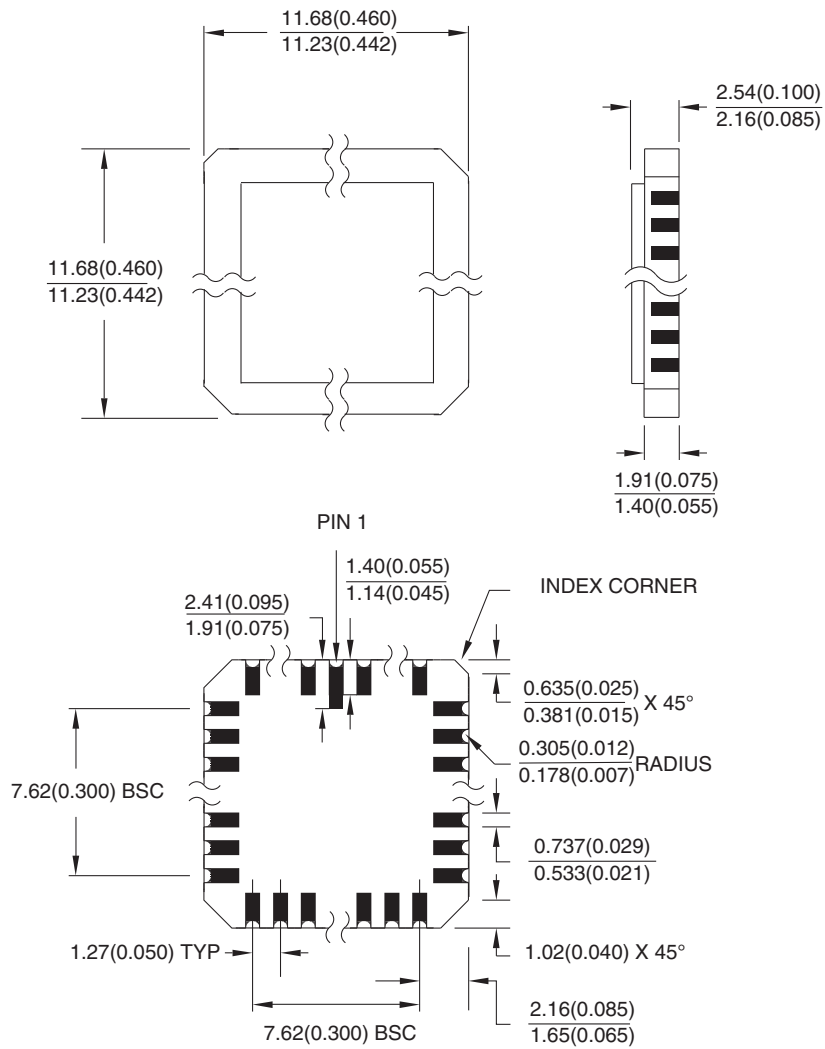
**REV.**

B



### 13.6 28L – LCC

Dimensions in Millimeters and (Inches).  
 Controlling dimension: Inches.  
 MIL-STD 1835 C-4



10/21/03

	<b>Package Drawing Contact:</b> packagedrawings@atmel.com	<b>TITLE</b> 28L, 28-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC)	<b>DRAWING NO.</b> 28L	<b>REV.</b> B
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## 14. Revision History

Doc. Rev.	Date	Comments
0735U	05/2010	Updated C-15 military device $I_{CC}$ limit Revised the maximum power supply current in PD mode for commercial- and industrial-grade devices from 100 $\mu$ A to 500 $\mu$ A and 100 $\mu$ A to 650 $\mu$ A maximum, respectively C-15 and CQ-15 Commercial part removed from <a href="#">Table 4-1</a> . Removed Mil from $I_{CC}$ , C-15 (Ind.) parts $I_{CC2}$ at 15mhz Max changed from 90mA to 125mA
0735T	05/2009	Added military-grade packages and removed leaded parts
0735S	08/2008	Added new green part
0735R	06/2008	Updated Green package options



## Headquarters

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### Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: (+1) (408) 441-0311  
Fax: (+1) (408) 487-2600  
[www.atmel.com](http://www.atmel.com)

## International

---

### Atmel Asia Limited

Unit 01-5 & 16, 19F  
BEA Tower, Millennium City 5  
418 Kwun Tong Road  
Kwun Tong, Kowloon  
HONG KONG  
Tel: (+852) 2245-6100  
Fax: (+852) 2722-1369

### Atmel Munich GmbH

Business Campus  
Parkring 4  
D-85748 Garching b. Munich  
GERMANY  
Tel: (+49) 89-31970-0  
Fax: (+49) 89-3194621

### Atmel Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
JAPAN  
Tel: (+81) (3) 3523-3551  
Fax: (+81) (3) 3523-7581

## Product Contacts

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### Technical Support

[PLD@atmel.com](mailto:PLD@atmel.com)

### Sales Contact

[www.atmel.com/contacts](http://www.atmel.com/contacts)

### Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

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