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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc200lc2an

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2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC200 Features – Advanced Line

- ARM® Cortex™-M0 core
 - Runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code
 - 4 KB flash for ISP loader
 - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128 KB system, fixed 4 KB data flash for the 32 KB and 64 KB system
 - Supports 2-wired ICP update through SWD/ICE interface
 - Supports fast parallel programming mode by external programmer
- SRAM Memory
 - 8K/16K bytes embedded SRAM
 - Supports PDMA mode
- PDMA (Peripheral DMA)
 - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
 - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed oscillator for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
 - Supports one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-pull output
 - ◆ Open-drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable
 - I/O pin configured as interrupt source with edge/level setting

2.2 NuMicro™ NUC220 Features – USB Line

- ARM® Cortex™-M0 core
 - Runs up to 50 MHz
 - One 24-bit system timer
 - Supports low power sleep mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
 - 32K/64K/128K bytes Flash for program code
 - 4 KB flash for ISP loader
 - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
 - 512 byte page erase for flash
 - Configurable data flash address and size for 128 KB system, fixed 4 KB data flash for the 32 KB and 64 KB system
 - Supports 2-wired ICP update through SWD/ICE interface
 - Supports fast parallel programming mode by external programmer
- SRAM Memory
 - 8K/16K bytes embedded SRAM
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- PDMA (Peripheral DMA)
 - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
 - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
 - Flexible selection for different applications
 - Built-in 22.1184 MHz high speed oscillator for system operation
 - ◆ Trimmed to $\pm 1\%$ at $+25\text{ }^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$
 - ◆ Trimmed to $\pm 3\%$ at $-40\text{ }^{\circ}\text{C} \sim +85\text{ }^{\circ}\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
 - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
 - Supports one PLL, up to 50 MHz, for high performance system operation
 - External 4~24 MHz high speed crystal input for USB and precise timing operation
 - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
 - Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-pull output
 - ◆ Open-drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable
 - I/O pin configured as interrupt source with edge/level setting
- Timer



3.2.2.3 NuMicro™ NUC220LxxAN LQFP 48-pin

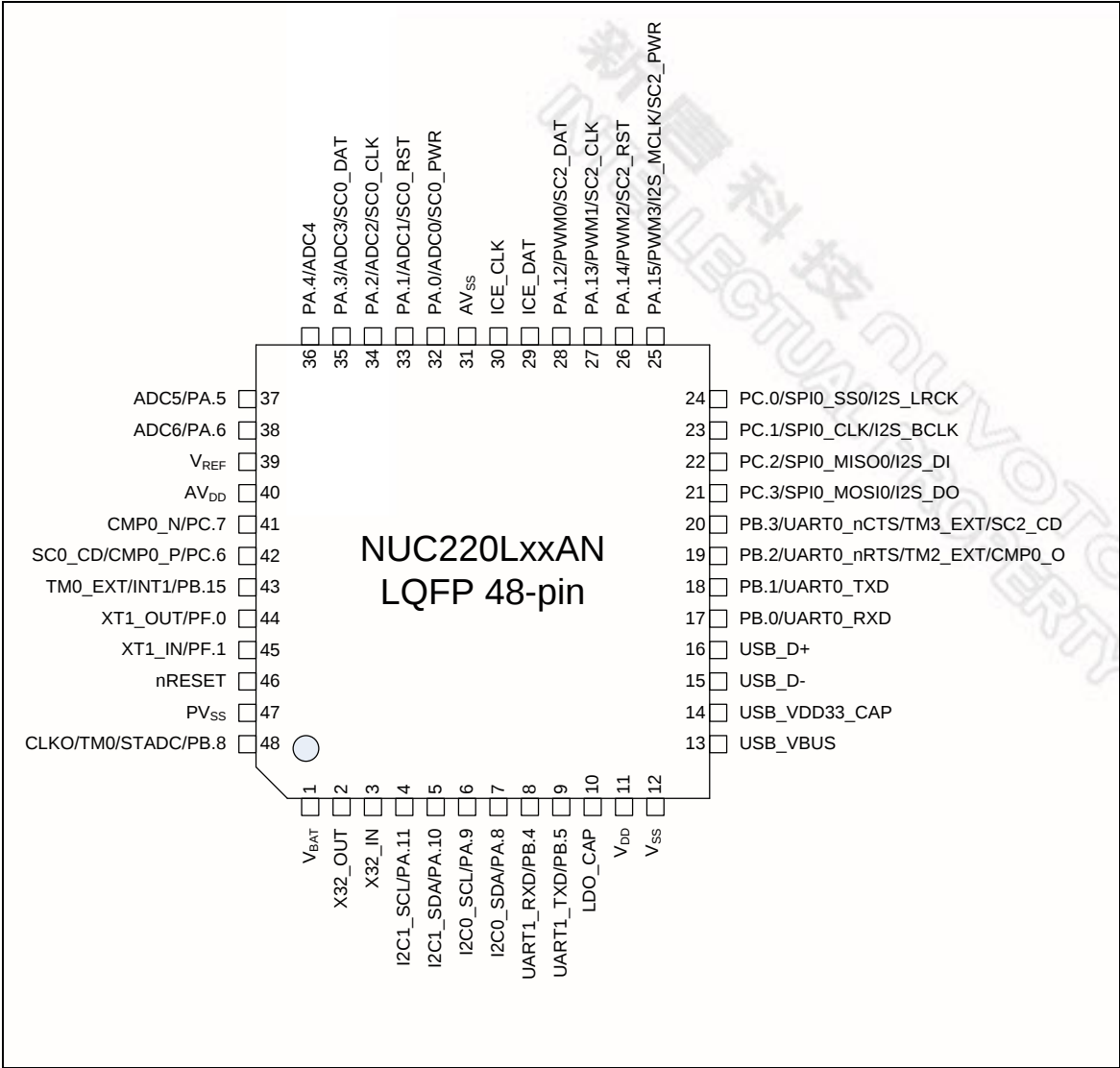


Figure 3-7 NuMicro™ NUC220LxxAN LQFP 48-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC0_CD	I	SmartCard0 card detect pin.
89	55		PC.15	I/O	General purpose digital I/O pin.
			CMP1_N	AI	Comparator1 negative input pin.
90	56		PC.14	I/O	General purpose digital I/O pin.
			CMP1_P	AI	Comparator1 positive input pin.
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			INT1	I	External interrupt1 input pin.
			TM0_EXT	I	Timer0 external capture input pin.
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V _{SS}	P	Ground pin for digital circuit.
96	62		V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2_DAT	I/O	PS2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2_CLK	I/O	PS2 clock pin.
99	63	47	PV _{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.
			CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power.

3.3.2 NuMicro™ NUC220 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			INT0	I	External interrupt0 input pin.
			SPI3_SS1	I/O	2 nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			CMP1_O	O	Comparator1 output pin.
6	3	1	V _{BAT}	P	Power supply by batteries for RTC.
7	4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
8	5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I ² C1 clock pin.
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1_SDA	I/O	I ² C1 data input/output pin.
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0_SCL	I/O	I ² C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0_SDA	I/O	I ² C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPI3_SS0	I/O	1 st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPI3_CLK	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.
			SPI3_MISO0	I/O	1 st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	I/O	General purpose digital I/O pin.
			SPI3_MOSI0	I/O	1 st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	I/O	General purpose digital I/O pin.
			SPI3_MISO1	I/O	2 nd SPI3 MISO (Master In, Slave Out) pin.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			SC1_RST	O	SmartCard1 reset pin.
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			SC1_CLK	I/O	SmartCard1 clock pin.
78			PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			SC1_CLK	O	SmartCard1 clock pin.
			SPI2_SS1	I/O	2 nd SPI2 slave select pin.
79	51	39	V _{REF}	AP	Voltage reference input for ADC.
80	52	40	AV _{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPI2_SS0	I/O	1 st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPI2_CLK	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			SPI2_MISO0	I/O	1 st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			SPI2_MOSI0	I/O	1 st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			SPI2_MISO1	I/O	2 nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	I/O	General purpose digital I/O pin.
			SPI2_MOSI1	I/O	2 nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	I/O	General purpose digital I/O pin.
			CMP0_N	AI	Comparator0 negative input pin.
			SC1_CD	I	SmartCard1 card detect pin.
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			CMP0_P	AI	Comparator0 positive input pin.
			SC0_CD	I	SmartCard0 card detect pin.

5.2.6.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ NUC200 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-2 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt Description
0 ~ 15	-	-	-	System exceptions
16	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt
17	1	WDT_INT	WDT	Watchdog Timer interrupt
18	2	EINT0	GPIO	External signal interrupt from PB.14 pin
19	3	EINT1	GPIO	External signal interrupt from PB.15 pin
20	4	GPAB_INT	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]/ PF[3:0]
22	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	PWMB_INT	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	TMR0_INT	TMR0	Timer 0 interrupt
25	9	TMR1_INT	TMR1	Timer 1 interrupt
26	10	TMR2_INT	TMR2	Timer 2 interrupt

IRQ23_SRC	INT_BA+0x5C	R	IRQ23 (USB) interrupt source identity	0XXXXX_XXXX
IRQ24_SRC	INT_BA+0x60	R	IRQ24 (PS/2) interrupt source identity	0XXXXX_XXXX
IRQ25_SRC	INT_BA+0x64	R	IRQ25 (ACMP) interrupt source identity	0XXXXX_XXXX
IRQ26_SRC	INT_BA+0x68	R	IRQ26 (PDMA) interrupt source identity	0XXXXX_XXXX
IRQ27_SRC	INT_BA+0x6C	R	IRQ27 (I ² S) interrupt source identity	0XXXXX_XXXX
IRQ28_SRC	INT_BA+0x70	R	IRQ28 (PWRWU) interrupt source identity	0XXXXX_XXXX
IRQ29_SRC	INT_BA+0x74	R	IRQ29 (ADC) interrupt source identity	0XXXXX_XXXX
IRQ30_SRC	INT_BA+0x78	R	IRQ30 (IRCT) interrupt source identity	0XXXXX_XXXX
IRQ31_SRC	INT_BA+0x7C	R	IRQ31 (RTC) interrupt source identity	0XXXXX_XXXX
NMI_SEL	INT_BA+0x80	R/W	NMI source interrupt select control register	0x0000_0000
MCU_IRQ	INT_BA+0x84	R/W	MCU interrupt request source register	0x0000_0000

5.3.4 Peripherals Clock

The peripherals clock can be selected as different clock source depends on the clock source select control registers (CLKSEL1, CLKSEL2 and CLKSEL3).

5.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
 - ◆ Internal 10 kHz low speed oscillator clock
 - ◆ External 32.768 kHz low speed crystal clock
- Peripherals Clock (when IP adopt external 32.768 kHz low speed crystal oscillator or 10 kHz low speed oscillator as clock source)

5.5 General Purpose I/O (GPIO)

5.5.1 Overview

The NuMicro™ NUC200 series has up to 80 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 80 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 K Ω for V_{DD} is from 5.0 V to 2.5 V.

5.5.2 Features

- Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
 - ◆ If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
 - ◆ If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

5.9 Serial Peripheral Interface (SPI)

5.9.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro™ NUC200 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable serial clock function for special applications and 2-bit Transfer mode to connect 2 off-chip slave devices at the same time. This controller also supports the PDMA function to access the data buffer and also supports Dual I/O Transfer mode.

5.9.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Two slave select lines in Master mode
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Variable output serial clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 transceiver control is implemented using the nRTS control signal from an asynchronous serial port to enable the RS-485 transceiver. In RS-485 mode, many characteristics of the receiving and transmitting are same as UART.

5.13.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (nCTS, nRTS) and programmable nRTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports nCTS wake-up function (UART0 and UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- UART0/UART1 can through DMA channels to receive/transmit data
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
 - Programmable data bit length, 5-, 6-, 7-, 8-bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
 - Supports 3-/16-bit duration for normal mode
- LIN function mode
 - Supports LIN master/slave mode
 - Supports programmable break generation function for transmitter
 - Supports break detect function for receiver
- RS-485 function mode.
 - Supports RS-485 9-bit mode
 - Supports hardware or software direct enable control provided by nRTS pin

5.15 I²S Controller (I²S)

5.15.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 8-word deep FIFO for read path and write path respectively and is capable of handling 8-, 16-, 24- and 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

5.15.2 Features

- Operated as either Master or Slave
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports Mono and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two PDMA requests, one for transmitting and the other for receiving

5.19 Smart Card Host Interface (SC)

5.19.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

5.19.2 Features

- ISO7816-3 T=0, T=1 compliant
- EMV2000 compliant
- Supports up to three ISO7816-3 ports
- Separates receive/ transmit 4 byte entry buffer for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 266 ETU)
- One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error retry number limitation function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detecting the card removal

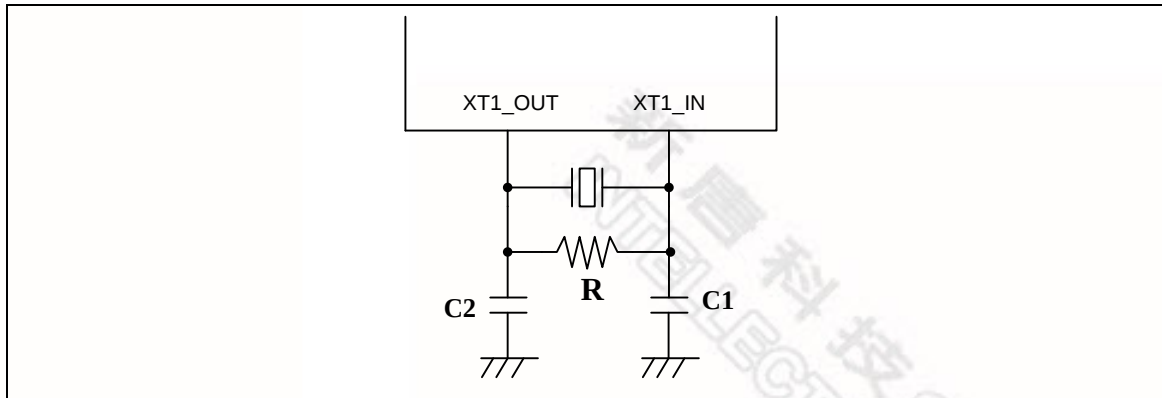


Figure 6-1 Typical Crystal Application Circuit

6.3.3 External 32.768 kHz Low Speed Crystal Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Operation Temperature	-	-40	-	85	°C
Operation Current	32.768KHz at $V_{DD}=5V$		1.5		μA
Clock Frequency	External crystal	-	32.768	-	kHz

6.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; $V_{DD} = 5V$	-1	-	+1	%
	-40°C ~ +85°C; $V_{DD} = 2.5V \sim 5.5V$	-3	-	+3	%
Operation Current	$V_{DD} = 5V$	-	500	-	uA

6.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; $V_{DD} = 5V$	-30	-	+30	%

6.4.6 Temperature Sensor Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage ^[1]		2.5	-	5.5	V
Operation Temperature		-40	-	85	°C
Current Consumption		6.4	-	10.5	μA
Gain			-1.76		mV/°C
Offset Voltage	Temp=0 °C		720		mV

Note: Internal operation voltage comes from internal LDO.

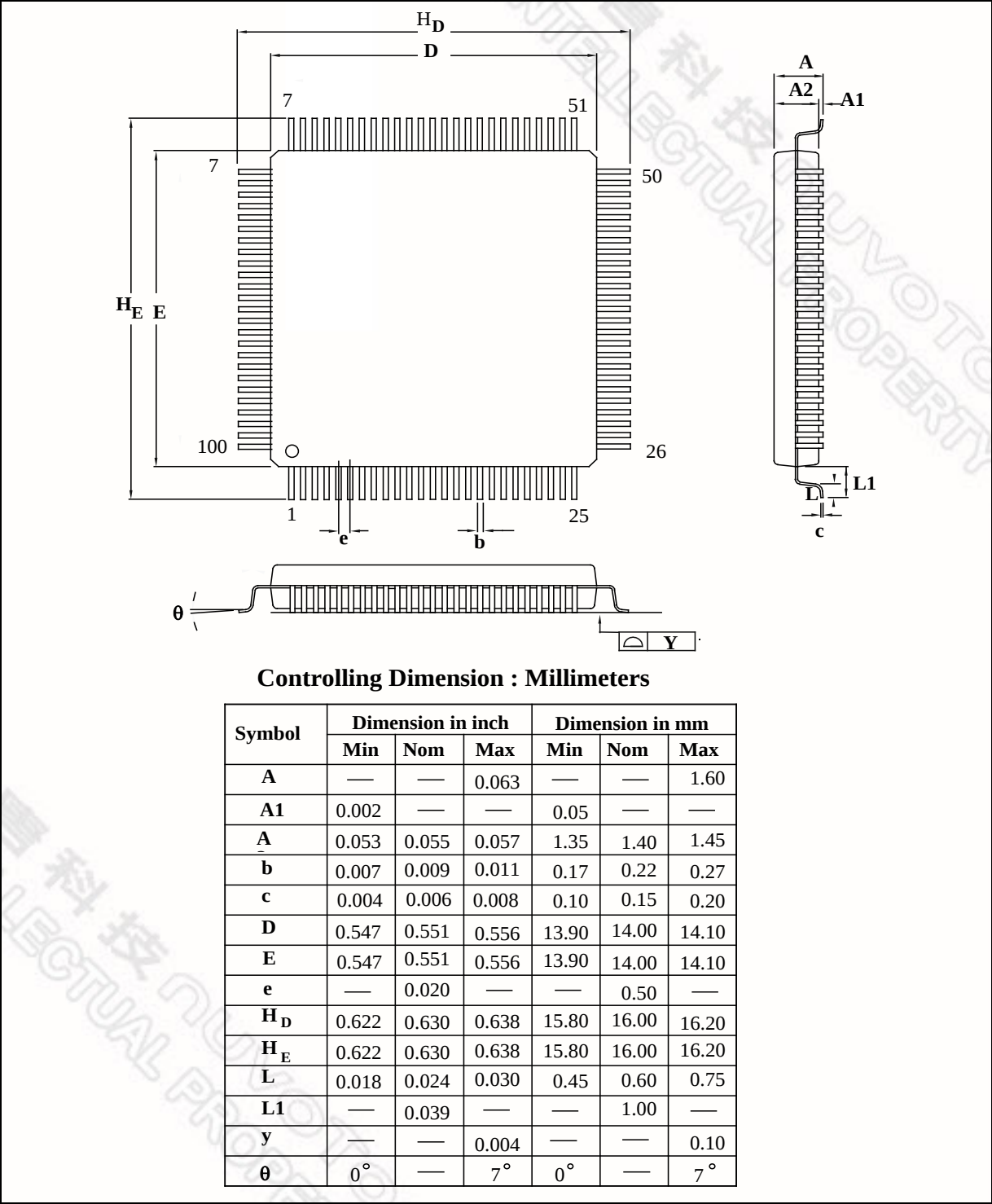
6.4.7 Comparator Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV_{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	°C
Operation Current	$V_{DD}=3.0$ V	-	20	40	μA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	$V_{DDA}-0.1$	V
Input Common Mode Range	-	0.1	-	$V_{DDA}-1.2$	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM = 1.2 V and VDIFF = 0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM= $V_{DD}-1.2$ 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ $V_{DD}-1.2$ V	-	±10	-	mV
Wake-up Time	CINP = 1.3 V CINN = 1.2 V	-	-	2	μs



7 PACKAGE DIMENSIONS

7.1 100-pin LQFP (14x14x1.4 mm footprint 2.0 mm)



8 REVISION HISTORY

Revision	Date	Description
V1.00	June 07, 2012	Initial release

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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