Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc200ve3an

- Compliant to ISO-7816-3 T=0, T=1
- Supports up to three ISO-7816-3 ports
- Separate receive / transmit 4 bytes entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 266 ETU)
- One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error limit function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detecting the card removal

- 96-bit unique ID (UID)

- One built-in temperature sensor with 1℃ resolution

- Brown-out Detector

  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option

- Low Voltage Reset

  - Threshold voltage level: 2.0 V

- Operating Temperature: -40℃ ~ 85℃

- Packages:

  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

- Supports PDMA mode

- Analog Comparator

    - Up to two analog comparators
    - External input or internal Band-gap voltage selectable at negative node
    - Interrupt when compare result change
    - Supports Power-down wake-up

- Smart Card Host (SC)

    - Compliant to ISO-7816-3 T=0, T=1
    - Supports up to three ISO-7816-3 ports
    - Separate receive / transmit 4 bytes entry FIFO for data payloads
    - Programmable transmission clock frequency
    - Programmable receiver buffer trigger level
    - Programmable guard time selection (11 ETU ~ 266 ETU)
    - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
    - Supports auto inverse convention function
    - Supports transmitter and receiver error retry and error limit function
    - Supports hardware activation sequence process
    - Supports hardware warm reset sequence process
    - Supports hardware deactivation sequence process
    - Supports hardware auto deactivation sequence when detecting the card removal

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- One built-in temperature sensor with 1℃ resolution

- Brown-out Detector

    - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
    - Supports Brown-out Interrupt and Reset option

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    - Threshold voltage level: 2.0 V

- Operating Temperature: -40℃ ~ 85℃

- Packages:

    - All Green package (RoHS)
    - LQFP 100-pin / 64-pin / 48-pin

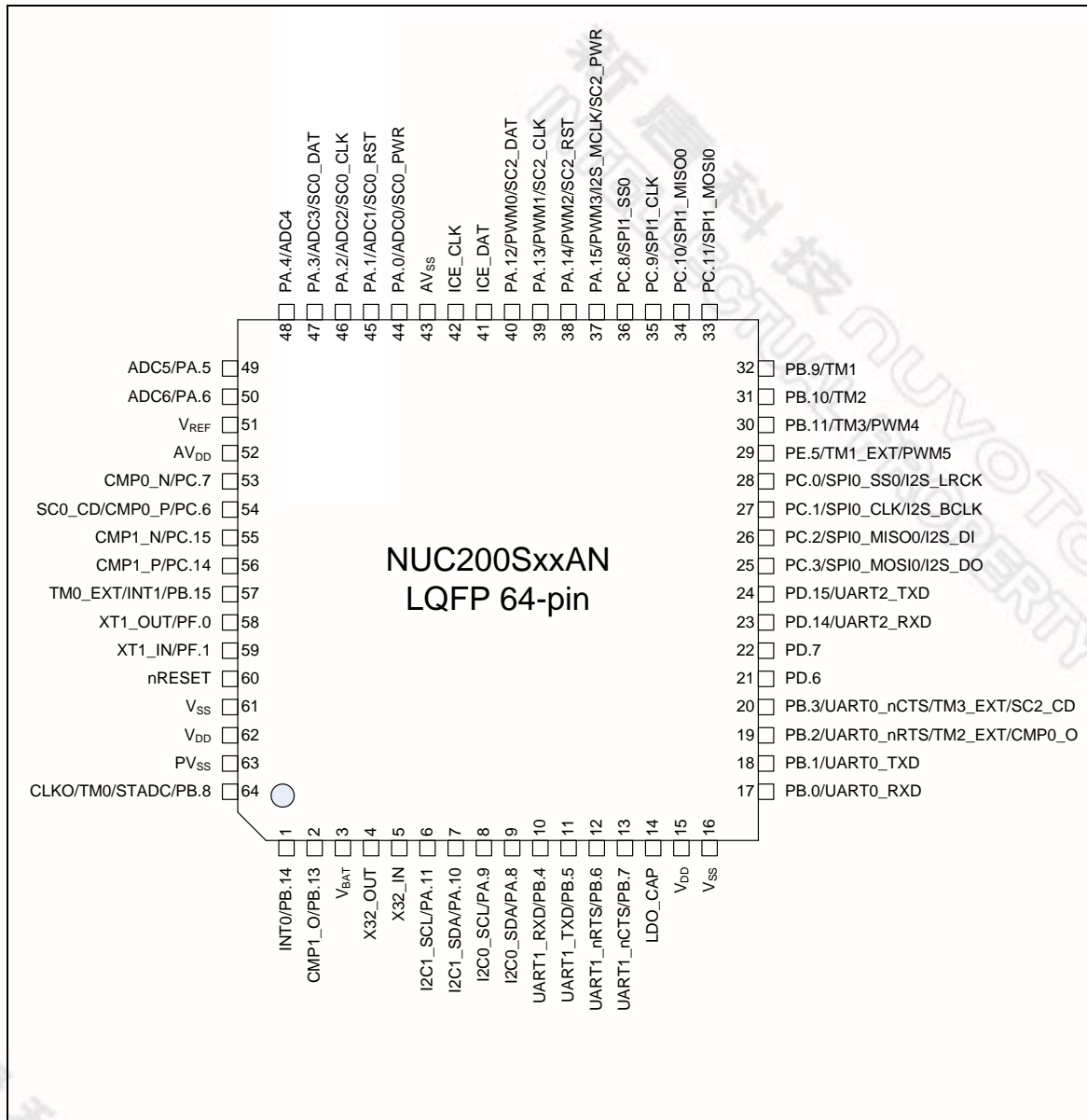### 3.2.1.2 *NuMicro™ NUC200RxxAN LQFP 64-pin*

Figure 3-3 NuMicro™ NUC200SxxAN LQFP 64-pin Diagram

3.3 Pin Description

3.3.1 NuMicro™ NUC200 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			INT0	I	External interrupt0 input pin.
			SPI3_SS1	I/O	2nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			CMP1_O	O	Comparator1 output pin.
6	3	1	V_{BAT}	P	Power supply by batteries for RTC.
7	4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
8	5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I^2C1 clock pin.
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1_SDA	I/O	I^2C1 data input/output pin.
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0_SCL	I/O	I^2C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0_SDA	I/O	I^2C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPI3_SS0	I/O	1st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPI3_CLK	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.
			SPI3_MISO0	I/O	1st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	I/O	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
35	20	16	PB.3	I/O	General purpose digital I/O pin.
			UART0_nCTS	I	Clear to Send input pin for UART0.
			TM3_EXT	I	Timer3 external capture input pin.
			SC2_CD	I	SmartCard2 card detect pin.
36	21		PD.6	I/O	General purpose digital I/O pin.
37	22		PD.7	I/O	General purpose digital I/O pin.
38	23		PD.14	I/O	General purpose digital I/O pin.
			UART2_RXD	I	Data receiver input pin for UART2.
39	24		PD.15	I/O	General purpose digital I/O pin.
			UART2_TXD	O	Data transmitter output pin for UART2.
40			PC.5	I/O	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			SPI0_MISO1	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
42	25	17	PC.3	I/O	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
			I2S_DO	O	I^{2}S data output.
43	26	18	PC.2	I/O	General purpose digital I/O pin.
			SPI0_MISO0	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
			I2S_DI	I	I^{2}S data input.
44	27	19	PC.1	I/O	General purpose digital I/O pin.
			SPI0_CLK	I/O	SPI0 serial clock pin.
			I2S_BCLK	I/O	I^{2}S bit clock pin.
45	28	20	PC.0	I/O	General purpose digital I/O pin.
			SPI0_SS0	I/O	1st SPI0 slave select pin.
			I2S_LRCK	I/O	I^{2}S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47	29	21	PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.
			TM1_EXT	I	Timer1 external capture input pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
48	30	22	PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31	23	PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPI0_SS1	I/O	2nd SPI0 slave select pin.
50	32	24	PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS1	I/O	2nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			SPI1_MOSI1	I/O	2nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			SPI1_MISO1	I/O	2nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			SPI1_MOSI0	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			SPI1_MISO0	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			SPI1_SS0	I/O	1st SPI1 slave select pin.
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC1_PWR	O	SmartCard1 power pin.
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			SC1_RST	O	SmartCard1 reset pin.
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			SC1_CLK	I/O	SmartCard1 clock pin.
78			PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			SC1_DAT	O	SmartCard1 data pin.
			SPI2_SS1	I/O	2nd SPI2 slave select pin.
79	51	39	V_{REF}	AP	Voltage reference input for ADC.
80	52	40	AV_{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPI2_SS0	I/O	1st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPI2_CLK	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			SPI2_MISO0	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			SPI2_MOSI0	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			SPI2_MISO1	I/O	2nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	I/O	General purpose digital I/O pin.
			SPI2_MOSI1	I/O	2nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	I/O	General purpose digital I/O pin.
			CMP0_N	AI	Comparator0 negative input pin.
			SC1_CD	I	SmartCard1 card detect pin.
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			CMP0_P	AI	Comparator0 positive input pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC0_CD	I	SmartCard0 card detect pin.
89	55		PC.15	I/O	General purpose digital I/O pin.
			CMP1_N	AI	Comparator1 negative input pin.
90	56		PC.14	I/O	General purpose digital I/O pin.
			CMP1_P	AI	Comparator1 positive input pin.
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			INT1	I	External interrupt1 input pin.
			TM0_EXT	I	Timer0 external capture input pin.
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V_{SS}	P	Ground pin for digital circuit.
96	62		V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2_DAT	I/O	PS2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2_CLK	I/O	PS2 clock pin.
99	63	47	PV_{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.
			CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power.

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2.3 System Power Distribution

In this chip, the power distribution is divided into four segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.

- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

- USB transceiver power from USB_VBUS offers the power for operating the USB transceiver.

- Battery power from V_{BAT} supplies the RTC and external 32.768 kHz crystal.

The outputs of internal voltage regulators, LDO_CAP and USB_VDD33_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 5-2 shows the power distribution of NuMicro™ NUC200; Figure 5-3 shows the power distribution of NuMicro™ NUC220.
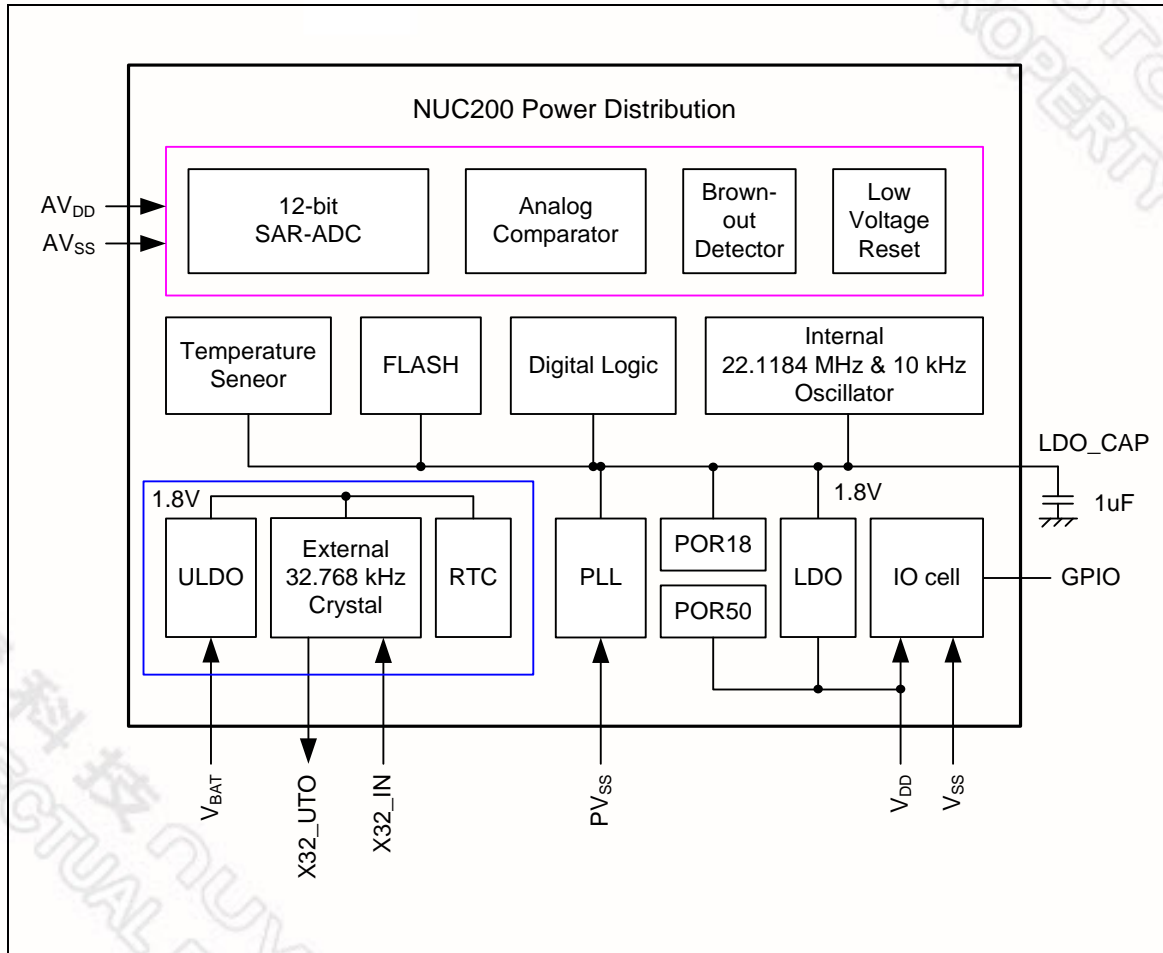

Figure 5-2 NuMicro™ NUC200 Power Distribution Diagram

27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**SPI2_INT**	SPI2	SPI2 interrupt
33	17	**SPI3_INT**	SPI3	SPI3 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**Reserved**	-	-
37	21	**Reserved**	-	-
38	22	**SC012_INT**	SC0/1/2	SC0, SC1 and SC2 interrupt
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**ACMP_INT**	ACMP	Analog Comparator-0 or Comaprator-1 interrupt
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**I2S_INT**	I^2S	I^2S interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**IRCT_INT**	IRC	IRC TRIM interrupt
47	31	**RTC_INT**	RTC	Real time clock interrupt

Table 5-3 System Interrupt Map

5.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.
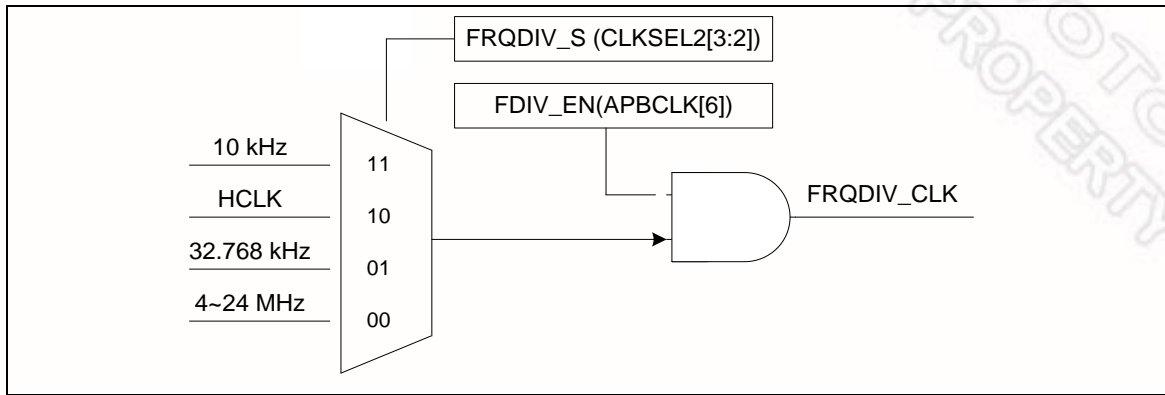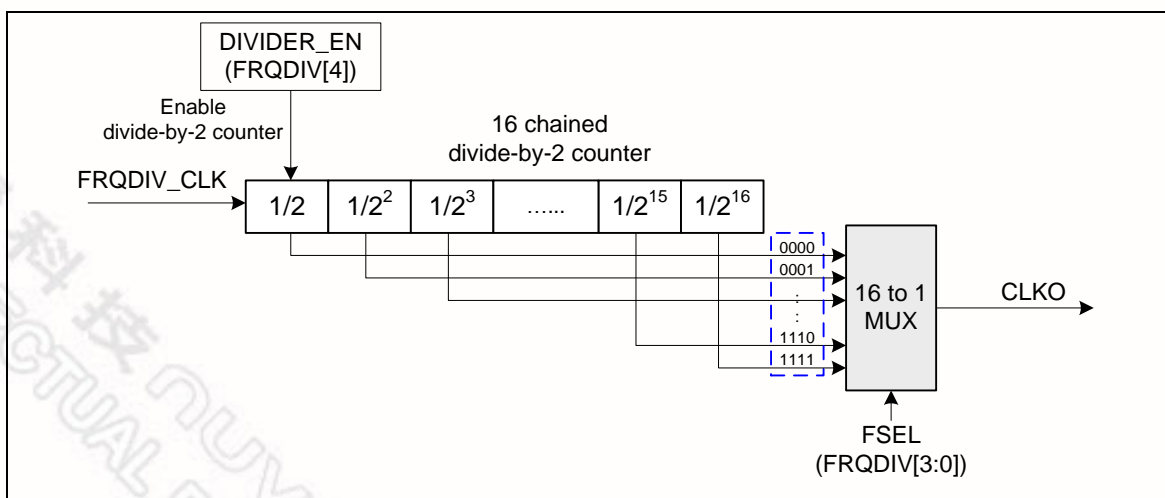

Figure 5-8 Clock Source of Frequency Divider

Figure 5-9 Frequency Divider Block Diagram

5.6.2   Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode

- Bidirectional data transfer between masters and slaves

- Multi-master bus (no central master)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus

- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer

- A built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.

- External pull-up resistors needed for high output

- Programmable clocks allowing for versatile rate control

- Supports 7-bit addressing mode

- Supports multiple address recognition (four slave addresses with mask option)

5.7 PWM Generator and Capture Timer (PWM)

5.7.1 Overview

The NuMicro™ NUC200 series has 2 sets of PWM group supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively. Refer to 錯誤! 找不到參照來源。 and 錯誤! 找不到參照來源。 for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For

5.8 Real Time Clock (RTC)

5.8.1 Overview

The Real Time Clock (RTC) controller provides user with the real time and calendar message. The clock source of RTC controller is from an external 32.768 kHz low speed crystal which connected at pins X32_IN and X32_OUT (refer to pin Description) or from an external 32.768 kHz low speed oscillator output fed at pin X32_IN. The RTC controller provides the real time message (hour, minute, second) in TLR (RTC Time Loading Register) as well as calendar message (year, month, day) in CLR (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in TAR (RTC Time Alarm Register) and alarm calendar in CAR (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0] Time Tick Register). When real time and calendar message in TLR and CLR are equal to alarm time and calendar settings in TAR and CAR, the AIF (RIIR [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the AIER (RIER [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the correlate interrupt enable bit (AIER or TIER) is set to 1 before chip enters Idle or Power-down mode.

5.8.2 Features

- Supports real time counter in TLR (hour, minute, second) and calendar counter in CLR (year, month, day) for RTC time and calendar check

- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in TAR and CAR

- Selectable 12-hour or 24-hour time scale in TSSR register

- Supports Leap Year indication in LIR register

- Supports Day of the Week counter in DWR register

- Frequency of RTC clock source compensate by FCR register

- All time and calendar message expressed in BCD format

- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second

- Supports RTC Time Tick and Alarm Match interrupt

- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated

6.4.6 Temperature Sensor Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage[1]		2.5	-	5.5	V
Operation Temperature		-40	-	85	℃
Current Consumption		6.4	-	10.5	µA
Gain			-1.76		mV/℃
Offset Voltage	Temp=0 ℃		720		mV

Note: Internal operation voltage comes from internal LDO.

6.4.7 Comparator Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV_{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	℃
Operation Current	V_{DD}=3.0 V	-	20	40	µA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	V_{DDA}-0.1	V
Input Common Mode Range	-	0.1	-	V_{DDA}-1.2	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM = 1.2 V and VDIFF = 0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM=V_{DD}-1.2 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ V_{DD}-1.2 V	-	±10	-	mV
Wake-up Time	CINP = 1.3 V CINN = 1.2 V	-	-	2	µs

6.4.8 USB PHY Specification

6.4.8.1 *USB DC Electrical Characteristics*

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

6.4.8.2 *USB Full-Speed Driver Electrical Characteristics*

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

6.4.8.3 *USB Power Dissipation*

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	USB_VBUS Current (Steady State)	Standby		50		µA

6.4.8.4 *USB LDO Specification*

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
USB_VBUS	USB_VBUS Pin Input Voltage		4.0	5.0	5.5	V
USB_VDD33_CAP	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	uF

6.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		100000			cycles[1]
T_{RET}	Data Retention	At 85℃	10			year
T_{ERASE}	Page Erase Time			2		ms
T_{MER}	Mass Erase Time			10		ms
T_{PROG}	Program Time			20		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current		-	1	20	μA

1. Number of program/erase cycles.

2. V_{DD} is source from chip LDO output voltage.

3. This table is guaranteed by design, not test in production.

7.2   64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)

SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)	b	0.13	0.18	0.23
LEAD WIDTH	b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)	c	0.09	---	0.2
L/F THICKNESS	c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC
	Y	E	9 BSC
	X	D1	7 BSC
	Y	E1	7 BSC
LEAD PITCH	e	0.4 BSC
FOOTPRINT	L	0.45	0.6	0.75
	L1	1 REF
	θ	0°	3.5°	7°
	θ1	0°	---	---
	θ2	11°	12°	13°
	θ3	11°	12°	13°
	R1	0.08	---	---
	R2	0.08	---	0.2
	S	0.2	---	---
PACKAGE EDGE TOLERANCE	aaa	0.2
LEAD EDGE TOLERANCE	bbb	0.2
COPLANARITY	ccc	0.08
LEAD OFFSET	ddd	0.07
MOLD FLATNESS	eee	0.05