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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc220ve3an

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- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function
- Watchdog Timer
 - Multiple clock sources
 - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
 - Wake-up from Power-down or Idle mode
 - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
 - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
 - Supports software compensation by setting frequency compensate register (FCR)
 - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Supports Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Supports battery power pin (V_{BAT})
 - Supports wake-up function
- PWM/Capture
 - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
 - Supports Capture interrupt
- UART
 - Up to three UART controllers
 - UART ports with flow control (TXD, RXD, nCTS and nRTS)
 - UART0 with 64-byte FIFO is for high speed
 - UART1/2(optional) with 16-byte FIFO for standard device
 - Supports IrDA (SIR) and LIN function
 - Supports RS-485 9-bit mode and direction control
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports PDMA mode
- SPI
 - Up to four sets of SPI controllers
 - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
 - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
 - Supports SPI Master/Slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 8 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode

- Supports Byte Suspend mode in 32-bit transmission
- Supports PDMA mode
- Supports three wire, no slave select signal, bi-direction interface
- I²C
 - Up to two sets of I²C device
 - Master/Slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - Programmable clocks allowing for versatile rate control
 - Supports multiple address recognition (four slave address with mask option)
 - Supports wake-up function
- I²S
 - Interface with external audio CODEC
 - Operate as either Master or Slave mode
 - Capable of handling 8-, 16-, 24- and 32-bit word sizes
 - Supports mono and stereo audio data
 - Supports I²S and MSB justified data format
 - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
 - Host communication inhibit and request to send detection
 - Reception frame error detection
 - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
 - Double buffer for data reception
 - Software override bus
- USB 2.0 Full-Speed Device
 - One set of USB 2.0 FS Device 12 Mbps
 - On-chip USB Transceiver
 - Provides 1 interrupt source with 4 interrupt events
 - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
 - Auto suspend function when no bus signaling for 3 ms
 - Provides 6 programmable endpoints
 - Includes 512 Bytes internal SRAM as USB buffer
 - Provides remote wake-up capability
- ADC
 - 12-bit SAR ADC with 760 kSPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion started by software programming or external input

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC200/220xxxAN Selection Guide

3.1.1 NuMicro™ NUC200 Advanced Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	SC	Comp.	PWM	ADC	RTC	ISP ICP IAP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC200LC2AN	32 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	2	1	6	7x12-bit	v	v	LQFP48
NUC200LD2AN	64 KB	8 KB	4KB	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	2	1	6	7x12-bit	v	v	LQFP48
NUC200LE3AN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	2	1	2	-	-	-	1	2	1	6	7x12-bit	v	v	LQFP48
NUC200SC2AN	32 KB	8 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC200SD2AN	64 KB	8 KB	4KB	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC200SE3AN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC200VE3AN	128 KB	16 KB	Definable	4 KB	up to 83	4x32-bit	3	4	2	-	-	-	1	3	2	8	8x12-bit	v	v	LQFP100

3.1.2 NuMicro™ NUC220 USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	SC	Comp.	PWM	ADC	RTC	ISP ICP IAP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC220LC2AN	32 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	2	1	4	7x12-bit	v	v	LQFP48
NUC220LD2AN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	2	1	4	7x12-bit	v	v	LQFP48
NUC220LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	2	1	4	7x12-bit	v	v	LQFP48
NUC220SC2AN	32 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC220SD2AN	64 KB	8 KB	8 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC220SE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	2	6	7x12-bit	v	v	LQFP64
NUC220VE3AN	128 KB	16 KB	Definable	4 KB	up to 79	4x32-bit	3	4	2	1	-	-	1	3	2	8	8x12-bit	v	v	LQFP100

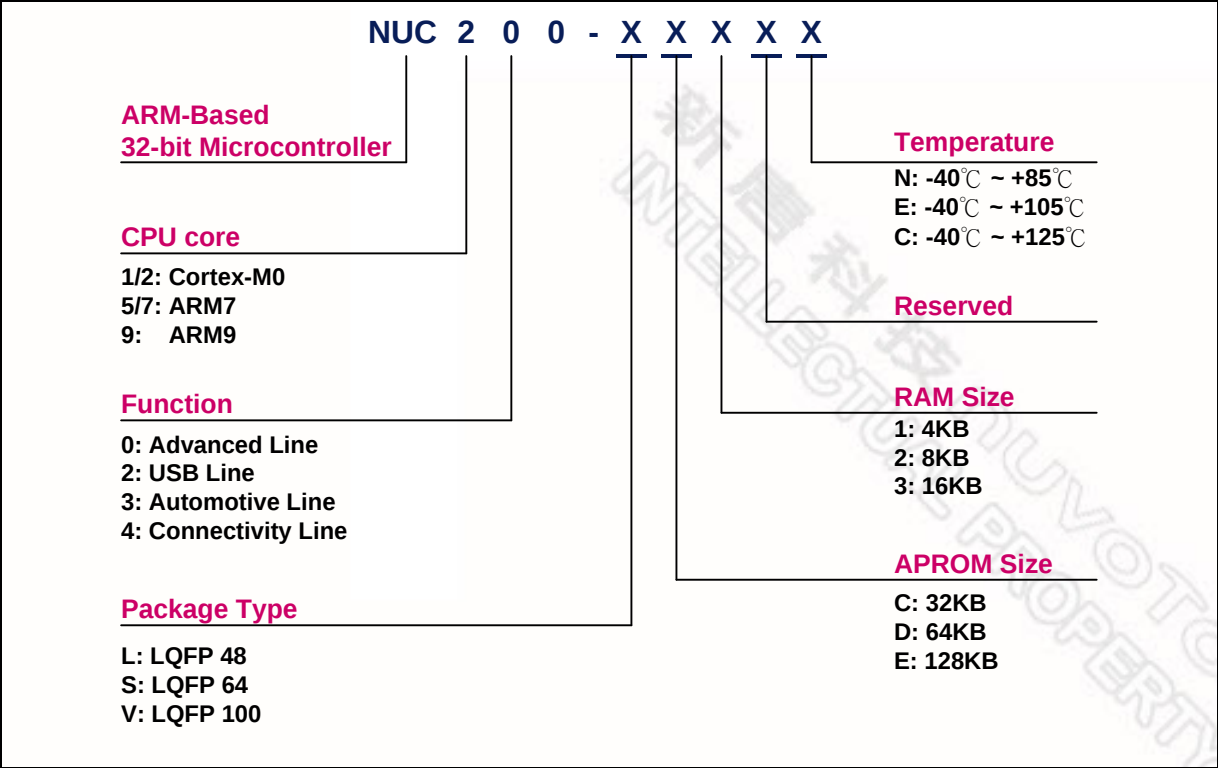


Figure 3-1 NuMicro™ NUC200 Series Selection Code

3.2.1.2 NuMicro™ NUC200RxxAN LQFP 64-pin

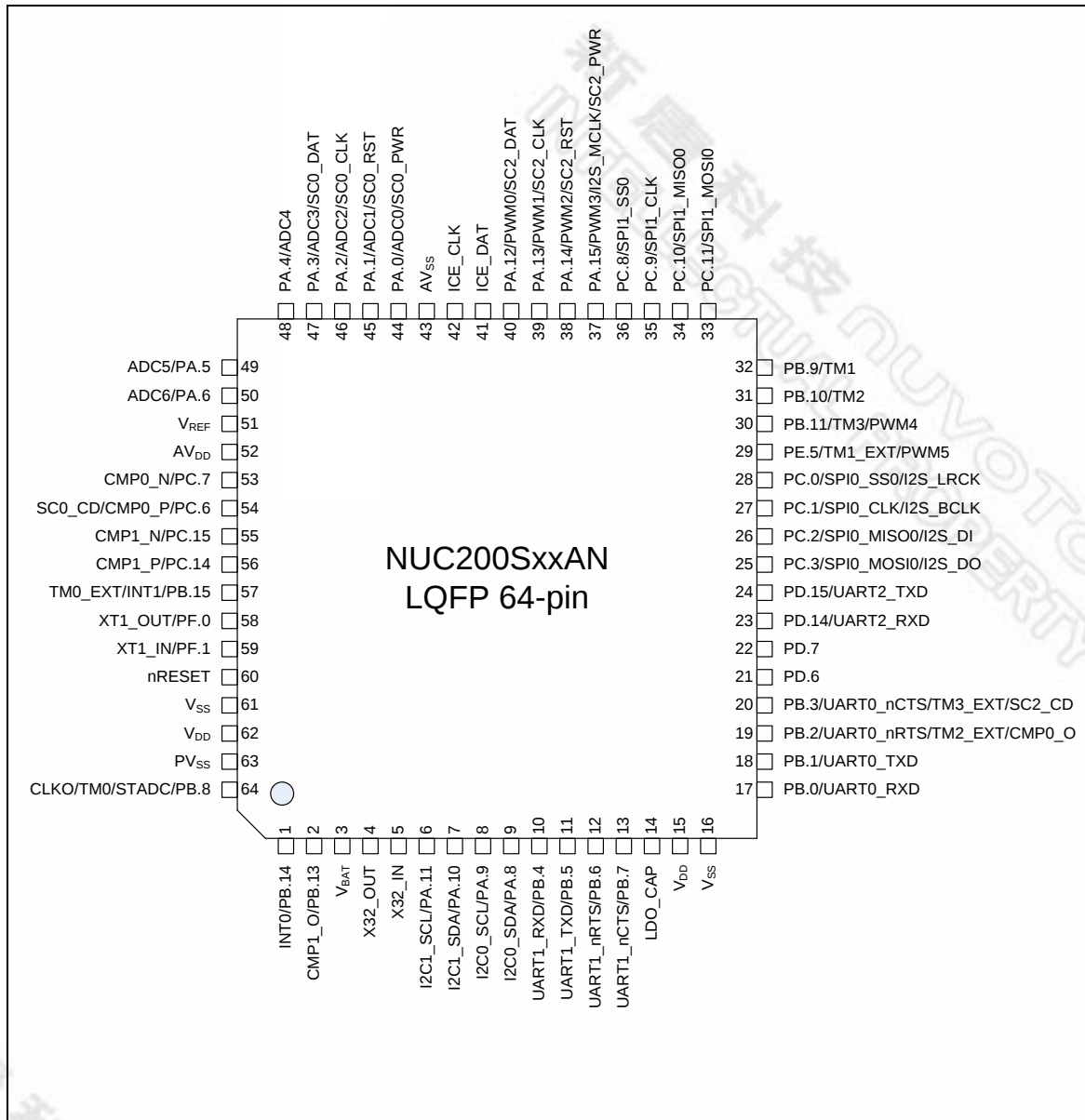


Figure 3-3 NuMicro™ NUC200SxxAN LQFP 64-pin Diagram



3.2.2.2 NuMicro™ NUC220RxxAN LQFP 64-pin

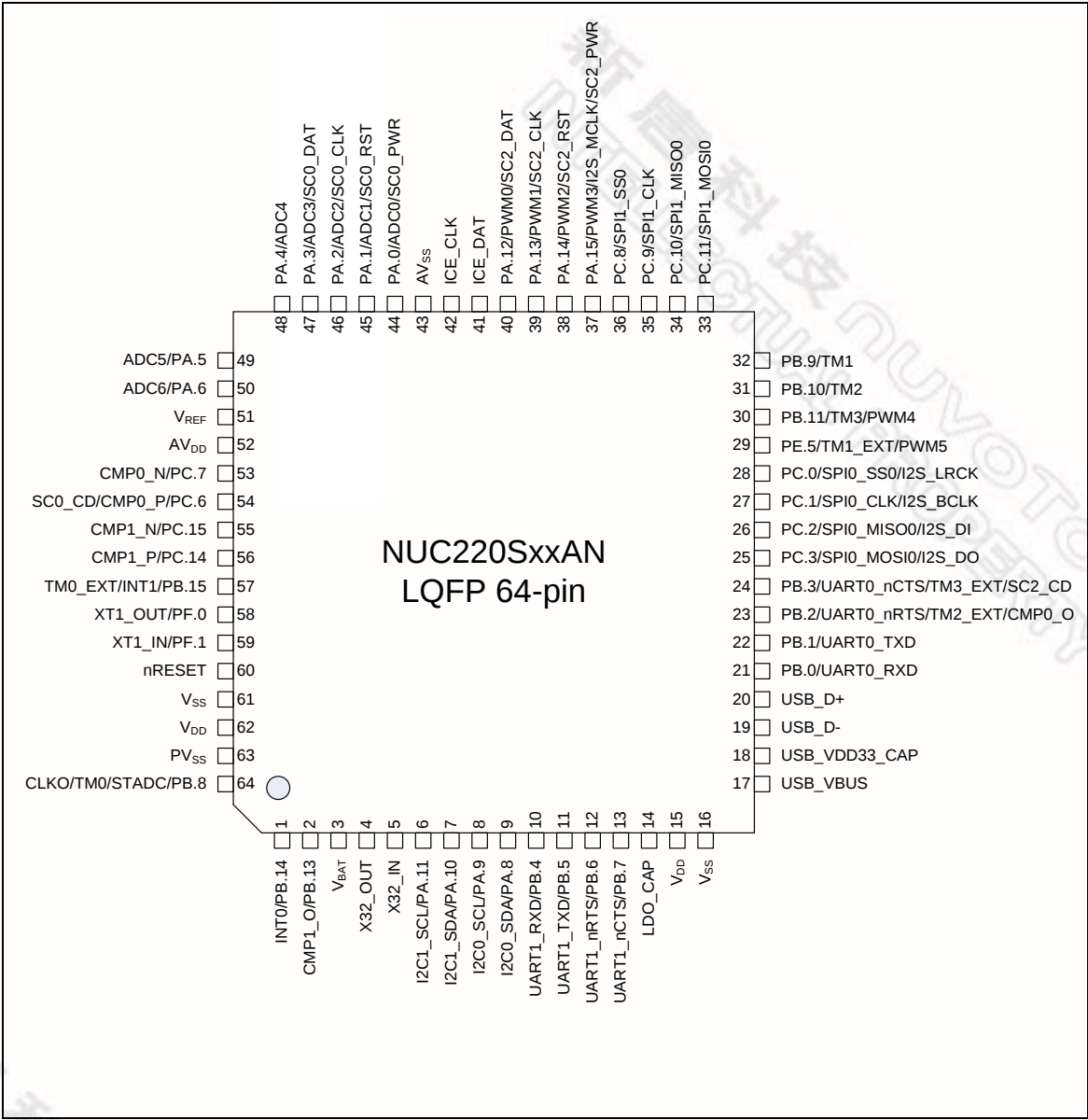


Figure 3-6 NuMicro™ NUC220SxxAN LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
48	30	22	PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31	23	PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPI0_SS1	I/O	2 nd SPI0 slave select pin.
50	32	24	PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS1	I/O	2 nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			SPI1_MOSI1	I/O	2 nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			SPI1_MISO1	I/O	2 nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			SPI1_MOSI0	I/O	1 st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			SPI1_MISO0	I/O	1 st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			SPI1_SS0	I/O	1 st SPI1 slave select pin.
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			I2S_MCLK	O	I ² S master clock output pin.
			SC2_PWR	O	SmartCard2 power pin.
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			SC2_RST	O	SmartCard2 reset pin.
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			SC2_CLK	O	SmartCard2 clock pin.
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			SC2_DAT	O	SmartCard2 data pin.
66	41	29	ICE_DAT	I/O	Serial wire debugger data pin.
67	42	30	ICE_CLK	I	Serial wire debugger clock pin.
68			V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V _{SS}	P	Ground pin for digital circuit.
70	43	31	AV _{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0_PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.
			ADC1	AI	ADC1 analog input.
			SC0_RST	O	SmartCard0 reset pin.
73	46	34	PA.2	I/O	General purpose digital I/O pin.
			ADC2	AI	ADC2 analog input.
			SC0_CLK	O	SmartCard0 clock pin.
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0_DAT	O	SmartCard0 data pin.
75	48	36	PA.4	I/O	General purpose digital I/O pin.
			ADC4	AI	ADC4 analog input.

3.3.2 NuMicro™ NUC220 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			INT0	I	External interrupt0 input pin.
			SPI3_SS1	I/O	2 nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			CMP1_O	O	Comparator1 output pin.
6	3	1	V _{BAT}	P	Power supply by batteries for RTC.
7	4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
8	5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I ² C1 clock pin.
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1_SDA	I/O	I ² C1 data input/output pin.
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0_SCL	I/O	I ² C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0_SDA	I/O	I ² C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPI3_SS0	I/O	1 st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPI3_CLK	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.
			SPI3_MISO0	I/O	1 st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	I/O	General purpose digital I/O pin.
			SPI3_MOSI0	I/O	1 st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	I/O	General purpose digital I/O pin.
			SPI3_MISO1	I/O	2 nd SPI3 MISO (Master In, Slave Out) pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			TM3_EXT	I	Timer3 external capture input pin.
			SC2_CD	I	SmartCard2 card detect pin.
36			PD.6	I/O	General purpose digital I/O pin.
37			PD.7	I/O	General purpose digital I/O pin.
38			PD.14	I/O	General purpose digital I/O pin.
			UART2_RXD	I	Data receiver input pin for UART2.
39			PD.15	I/O	General purpose digital I/O pin.
			UART2_TXD	O	Data transmitter output pin for UART2.
40			PC.5	I/O	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	2 nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			SPI0_MISO1	I/O	2 nd SPI0 MISO (Master In, Slave Out) pin.
42	25	21	PC.3	I/O	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	1 st SPI0 MOSI (Master Out, Slave In) pin.
			I2S_DO	O	I ² S data output.
43	26	22	PC.2	I/O	General purpose digital I/O pin.
			SPI0_MISO0	I/O	1 st SPI0 MISO (Master In, Slave Out) pin.
			I2S_DI	I	I ² S data input.
44	27	23	PC.1	I/O	General purpose digital I/O pin.
			SPI0_CLK	I/O	SPI0 serial clock pin.
			I2S_BCLK	I/O	I ² S bit clock pin.
45	28	24	PC.0	I/O	General purpose digital I/O pin.
			SPI0_SS0	I/O	1 st SPI0 slave select pin.
			I2S_LRCK	I/O	I ² S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47	29		PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.
			TM1_EXT	I	Timer1 external capture input pin.
48	30		PB.11	I/O	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
89	55		PC.15	I/O	General purpose digital I/O pin.
			CMP1_N	AI	Comparator1 negative input pin.
90	56		PC.14	I/O	General purpose digital I/O pin.
			CMP1_P	AI	Comparator1 positive input pin.
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			INT1	I	External interrupt1 input pin.
			TM0_EXT	I	Timer 0 external capture input pin.
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V _{SS}	P	Ground pin for digital circuit.
96	62		V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2_DAT	I/O	PS2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2_CLK	I/O	PS2 clock pin.
99	63	47	PV _{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.
			CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power.

0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I ² C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4019_0000 – 0x4019_3FFF	SC0_BA	SC0 Control Registers
0x4019_4000 – 0x4019_7FFF	SC1_BA	SC1 Control Registers
0x4019_8000 – 0x4019_BFFF	SC2_BA	SC2 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.6.4 Interrupt Source Register Map

Besides the interrupt control registers associated with the NVIC, the NuMicro™ NUC200 Series also implements some specific control registers to facilitate the interrupt functions, including “interrupt source identification”, “NMI source selection” and “interrupt test mode”, which are described below.

R: read only, W: write only, R/W: both read and write

Register	Offset	R/W	Description	Reset Value
INT Base Address: INT_BA = 0x5000_0300				
IRQ0_SRC	INT_BA+0x00	R	IRQ0 (BOD) interrupt source identity	0XXXXX_XXXX
IRQ1_SRC	INT_BA+0x04	R	IRQ1 (WDT) interrupt source identity	0XXXXX_XXXX
IRQ2_SRC	INT_BA+0x08	R	IRQ2 (EINT0) interrupt source identity	0XXXXX_XXXX
IRQ3_SRC	INT_BA+0x0C	R	IRQ3 (EINT1) interrupt source identity	0XXXXX_XXXX
IRQ4_SRC	INT_BA+0x10	R	IRQ4 (GPA/GPB) interrupt source identity	0XXXXX_XXXX
IRQ5_SRC	INT_BA+0x14	R	IRQ5 (GPC/GPD/GPE/GPF) interrupt source identity	0XXXXX_XXXX
IRQ6_SRC	INT_BA+0x18	R	IRQ6 (PWMA) interrupt source identity	0XXXXX_XXXX
IRQ7_SRC	INT_BA+0x1C	R	IRQ7 (PWMB) interrupt source identity	0XXXXX_XXXX
IRQ8_SRC	INT_BA+0x20	R	IRQ8 (TMR0) interrupt source identity	0XXXXX_XXXX
IRQ9_SRC	INT_BA+0x24	R	IRQ9 (TMR1) interrupt source identity	0XXXXX_XXXX
IRQ10_SRC	INT_BA+0x28	R	IRQ10 (TMR2) interrupt source identity	0XXXXX_XXXX
IRQ11_SRC	INT_BA+0x2C	R	IRQ11 (TMR3) interrupt source identity	0XXXXX_XXXX
IRQ12_SRC	INT_BA+0x30	R	IRQ12 (UART0/UART2) interrupt source identity	0XXXXX_XXXX
IRQ13_SRC	INT_BA+0x34	R	IRQ13 (UART1) interrupt source identity	0XXXXX_XXXX
IRQ14_SRC	INT_BA+0x38	R	IRQ14 (SPI0) interrupt source identity	0XXXXX_XXXX
IRQ15_SRC	INT_BA+0x3C	R	IRQ15 (SPI1) interrupt source identity	0XXXXX_XXXX
IRQ16_SRC	INT_BA+0x40	R	IRQ16 (SPI2) interrupt source identity	0XXXXX_XXXX
IRQ17_SRC	INT_BA+0x44	R	IRQ17 (SPI3) interrupt source identity	0XXXXX_XXXX
IRQ18_SRC	INT_BA+0x48	R	IRQ18 (I ² C0) interrupt source identity	0XXXXX_XXXX
IRQ19_SRC	INT_BA+0x4C	R	IRQ19 (I ² C1) interrupt source identity	0XXXXX_XXXX
IRQ20_SRC	INT_BA+0x50	R	Reserved	0XXXXX_XXXX
IRQ21_SRC	INT_BA+0x54	R	Reserved	0XXXXX_XXXX
IRQ22_SRC	INT_BA+0x58	R	IRQ22 (SC0/SC1/SC2) interrupt source identity	0XXXXX_XXXX

example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will be $1/900\text{ns} \approx 1000\text{ kHz}$

5.7.2 Features

5.7.2.1 PWM function:

- Up to 2 PWM groups (PWMA/PWMB) to support 8 PWM channels or 4 complementary PWM paired channels
- Each PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, two clock divider, two PWM-timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

5.7.2.2 Capture Function:

- Timing control logic shared with PWM generators
- Supports 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.13 UART Interface Controller (UART)

The NuMicro™ NUC200 series provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART. Besides, only UART0 and UART1 support the flow control function.

5.13.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR, LIN master/slave mode and RS-485 mode functions. Each UART channel supports seven types of interrupts including:

- Transmitter FIFO empty interrupt (INT_THRE);
- Receiver threshold level reached interrupt (INT_RDA);
- Line status interrupt (parity error or frame error or break interrupt) (INT_RLS);
- Receiver buffer time-out interrupt (INT_TOUT);
- MODEM/Wake-up status interrupt (INT_MODEM);
- Buffer error interrupt (INT_BUF_ERR);
- LIN interrupt (INT_LIN).

Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to the Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The UART1~2 are equipped with 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, frame error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is $\text{Baud Rate} = \text{UART_CLK} / M * [\text{BRD} + 2]$, where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 5-5 lists the equations in the various conditions and Table 5-6 lists the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	Don't care	A	$\text{UART_CLK} / [16 * (A+2)]$
1	1	0	B	A	$\text{UART_CLK} / [(B+1) * (A+2)]$, B must ≥ 8
2	1	1	Don't care	A	$\text{UART_CLK} / (A+2)$, A must ≥ 3

Table 5-5 UART Baud Rate Equation

System clock = internal 22.1184 MHz high speed oscillator			
Baud Rate	Mode 0	Mode 1	Mode 2

	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016
460800	A=1	0x0000_0001	A=1,B=15 A=2,B=11	0x2F00_0001 0x2B00_0002	A=46	0x3000_002E
230400	A=4	0x0000_0004	A=4,B=15 A=6,B=11	0x2F00_0004 0x2B00_0006	A=94	0x3000_005E
115200	A=10	0x0000_000A	A=10,B=15 A=14,B=11	0x2F00_000A 0x2B00_000E	A=190	0x3000_00BE
57600	A=22	0x0000_0016	A=22,B=15 A=30,B=11	0x2F00_0016 0x2B00_001E	A=382	0x3000_017E
38400	A=34	0x0000_0022	A=62,B=8 A=46,B=11 A=34,B=15	0x2800_003E 0x2B00_002E 0x2F00_0022	A=574	0x3000_023E
19200	A=70	0x0000_0046	A=126,B=8 A=94,B=11 A=70,B=15	0x2800_007E 0x2B00_005E 0x2F00_0046	A=1150	0x3000_047E
9600	A=142	0x0000_008E	A=254,B=8 A=190,B=11 A=142,B=15	0x2800_00FE 0x2B00_00BE 0x2F00_008E	A=2302	0x3000_08FE
4800	A=286	0x0000_011E	A=510,B=8 A=382,B=11 A=286,B=15	0x2800_01FE 0x2B00_017E 0x2F00_011E	A=4606	0x3000_11FE

Table 5-6 UART Baud Rate Setting Table

The UART0 and UART1 controllers support the auto-flow control function that uses two low-level signals, nCTS (clear-to-send) and nRTS (request-to-send), to control the flow of data transfer between the chip and external devices (e.g. Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts nRTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the nRTS is de-asserted. The UART sends data out when UART controller detects nCTS is asserted from external device. If a valid asserted nCTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with 1 start bit, 8 data bits, and 1 stop bit. The maximum data rate supports up to 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR Protocol encoder/decoder is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception, and this delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the UA_FUN_SEL[1:0] to '01'. In LIN mode, 1 start bit and 8 data bits format with 1 stop bit are required in accordance with the LIN standard.

For NuMicro™ NUC200 Series, another alternate function of UART controllers is RS-485 9-bit mode, and direction control provided by nRTS pin or can program GPIO (PB.2 for UART0_nRTS and PB.6 for UART1_nRTS) to implement the function by software. The RS-485 mode is selected

5.16 Analog-to-Digital Converter (ADC)

5.16.1 Overview

The NuMicro™ NUC200 Series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM Center-aligned trigger and external STADC pin.

5.16.2 Features

- Analog input voltage range: $0 \sim V_{REF}$
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 760 kSPS conversion rate as ADC clock frequency is 16 MHz (chip working at 5V)
- Three operating modes
 - Single mode: A/D conversion is performed one time on a specified channel
 - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
 - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
 - Writing 1 to ADST bit through software
 - PWM Center-aligned trigger
 - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal Band-gap voltage, and internal temperature sensor output

5.20 FLASH MEMORY CONTROLLER (FMC)

5.20.1 Overview

The NuMicro™ NUC200 Series has 128/64/32K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro™ NUC200 Series also provides additional DATA Flash for user to store some application dependent data. For 128K bytes APROM device, the data flash is shared with original 128K program memory and its start address is configurable in Config1. For 64K/32K bytes APROM device, the data flash is fixed at 4K.

5.20.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 128/64/32 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB data flash for 64/32 KB APROM device
- Configurable data flash size for 128KB APROM device
- Configurable or fixed 4 KB data flash with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash



7 PACKAGE DIMENSIONS

7.1 100-pin LQFP (14x14x1.4 mm footprint 2.0 mm)

