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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	6036
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	203
Number of Gates	108000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	256-BFCQFP with Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/5962-0054302qxc">https://www.e-xfl.com/product-detail/microchip-technology/5962-0054302qxc</a>

## Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable

interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

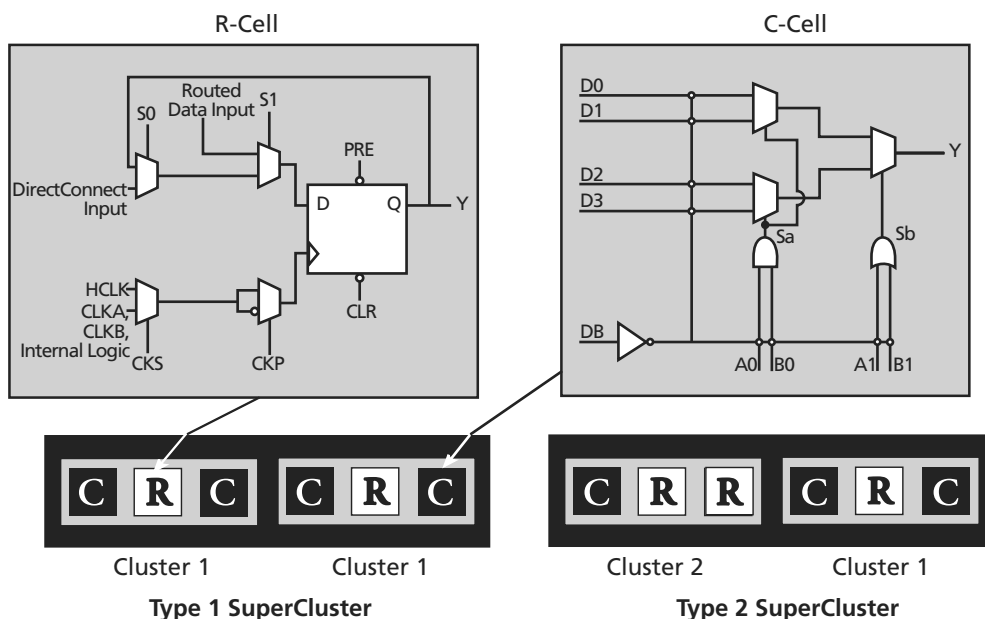


Figure 1-4 • Cluster Organization

## SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a  $70\ \Omega$  series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The  $70\ \Omega$  series termination is used to prevent data transmission corruption during probing and reading back the checksum.

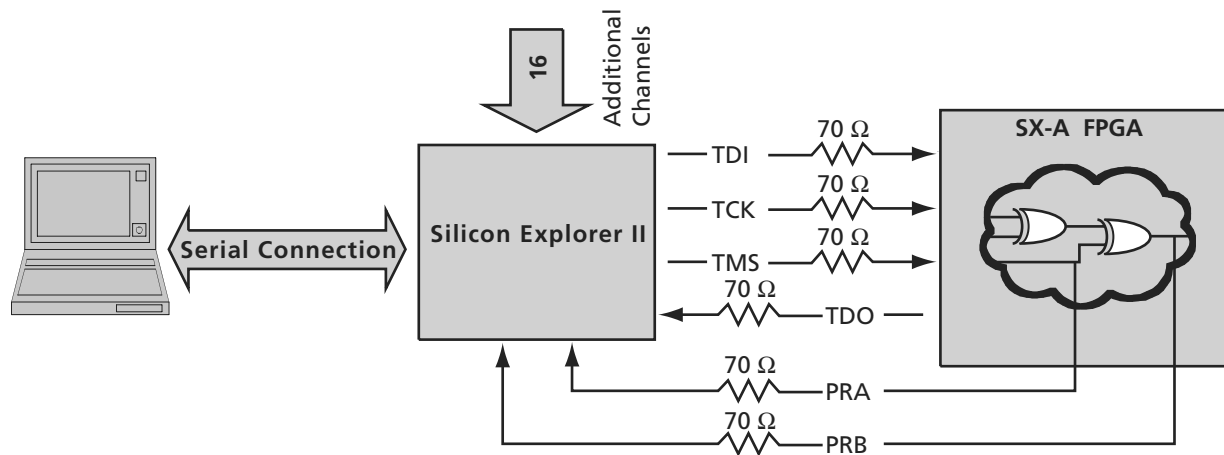


Figure 1-13 • Probe Setup

## Pin Description

### **CLKA/B, I/O**      **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

### **QCLKA/B/C/D, I/O**      **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

### **GND**      **Ground**

Low supply voltage.

### **HCLK**      **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

### **I/O**      **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

### **NC**      **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

### **PRA/B, I/O**      **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### **TCK, I/O**      **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDI, I/O**      **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDO, I/O**      **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

### **TMS**      **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

### **TRST, I/O**      **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

### **V<sub>CC</sub>**      **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V<sub>CC</sub> power pins in the device should be connected.

### **V<sub>CCA</sub>**      **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V<sub>CCA</sub> power pins in the device should be connected.

# Detailed Specifications

## Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
$V_{CCI}$	DC Supply Voltage for I/Os	−0.3 to +6.0	V
$V_{CCA}$	DC Supply Voltage for Arrays	−0.3 to +3.0	V
$V_I$	Input Voltage	−0.5 to +5.75	V
$V_O$	Output Voltage	−0.5 to + $V_{CCI}$ + 0.5	V
$T_{STG}$	Storage Temperature	−65 to +150	°C

**Note:** \*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	−40 to +85	°C
2.5 V Power Supply Range ( $V_{CCA}$ and $V_{CCI}$ )	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range ( $V_{CCI}$ )	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range ( $V_{CCI}$ )	4.75 to 5.25	4.75 to 5.25	V

## Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with  $V_{CCA} = 2.5$  V

Product	$V_{CCI} = 2.5$ V	$V_{CCI} = 3.3$ V	$V_{CCI} = 5$ V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

$V_{CCA}$	$V_{CCI}^*$	Maximum Input Tolerance	Maximum Output Drive
2.5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

**Note:** \*3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

## PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V <sub>CCA</sub>	Supply Voltage for Array		2.25	2.75	V
V <sub>CCI</sub>	Supply Voltage for I/Os		4.75	5.25	V
V <sub>IH</sub>	Input High Voltage		2.0	5.75	V
V <sub>IL</sub>	Input Low Voltage		–0.5	0.8	V
I <sub>IH</sub>	Input High Leakage Current <sup>1</sup>	V <sub>IN</sub> = 2.7	–	70	μA
I <sub>IL</sub>	Input Low Leakage Current <sup>1</sup>	V <sub>IN</sub> = 0.5	–	–70	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = –2 mA	2.4	–	V
V <sub>OL</sub>	Output Low Voltage <sup>2</sup>	I <sub>OUT</sub> = 3 mA, 6 mA	–	0.55	V
C <sub>IN</sub>	Input Pin Capacitance <sup>3</sup>		–	10	pF
C <sub>CLK</sub>	CLK Pin Capacitance		5	12	pF

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

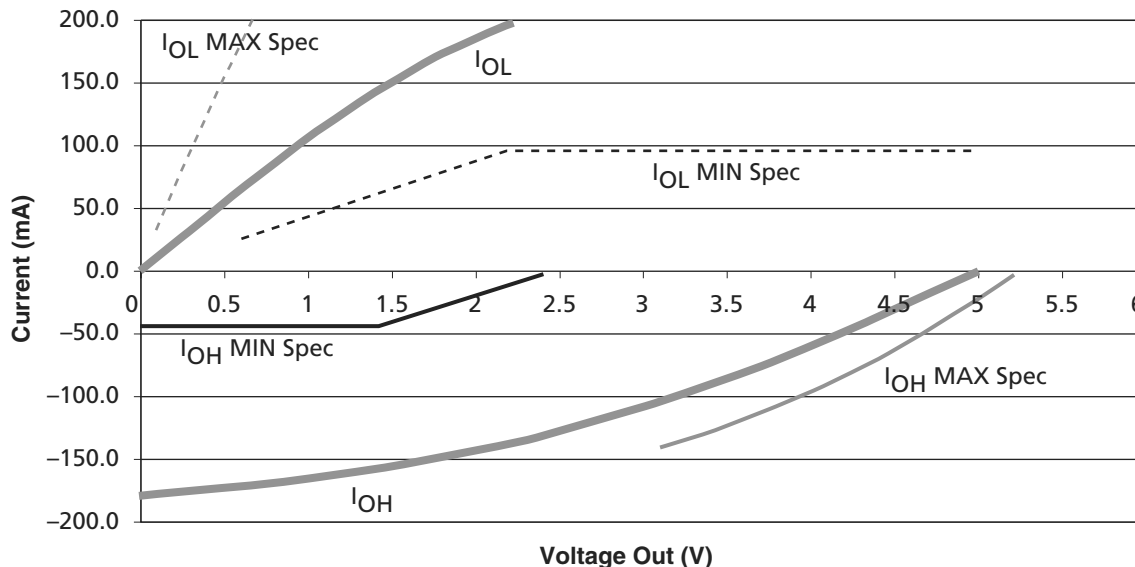


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for  $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for  $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$V_{CCA}$	Supply Voltage for Array		2.25	2.75	V
$V_{CCI}$	Supply Voltage for I/Os		3.0	3.6	V
$V_{IH}$	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
$V_{IL}$	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
$I_{IPU}$	Input Pull-up Voltage <sup>1</sup>		$0.7V_{CCI}$	–	V
$I_{IL}$	Input Leakage Current <sup>2</sup>	$0 < V_{IN} < V_{CCI}$	-10	+10	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$	–	V
$V_{OL}$	Output Low Voltage	$I_{OUT} = 1,500 \mu A$		$0.1V_{CCI}$	V
$C_{IN}$	Input Pin Capacitance <sup>3</sup>		–	10	pF
$C_{CLK}$	CLK Pin Capacitance		5	12	pF

**Notes:**

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

# Thermal Characteristics

## Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

- $\theta_{JA}$  = Junction-to-air thermal resistance
- $\theta_{JC}$  = Junction-to-case thermal resistance
- $T_J$  = Junction temperature
- $T_A$  = Ambient temperature
- $T_C$  = Ambient temperature
- $P$  = total power dissipated by the device

Table 2-12 • Package Thermal Characteristics

Package Type	Pin Count	$\theta_{JC}$	$\theta_{JA}$			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP) <sup>1</sup>	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader <sup>2</sup>	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

### Notes:

- The A54SX08A PQ208 has no heat spreader.
- The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.



# Output Buffer Delays

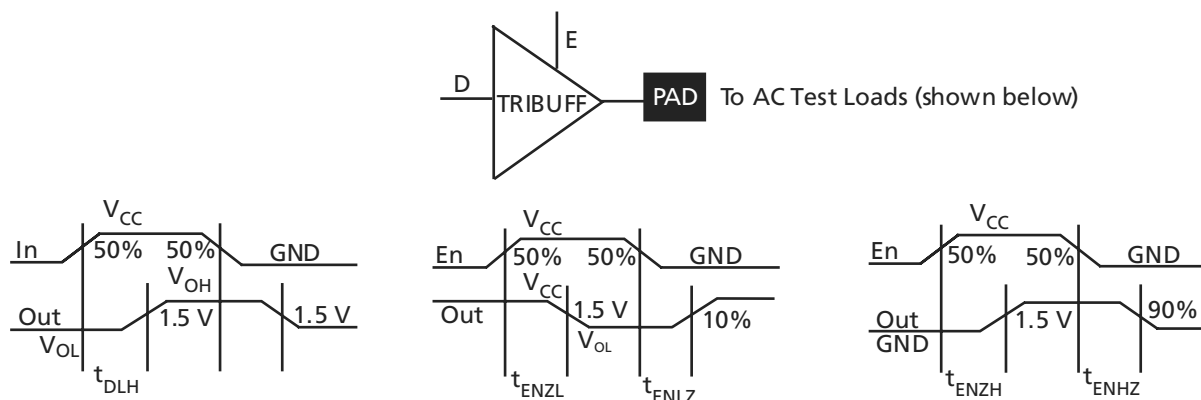


Figure 2-4 • Output Buffer Delays

# AC Test Loads

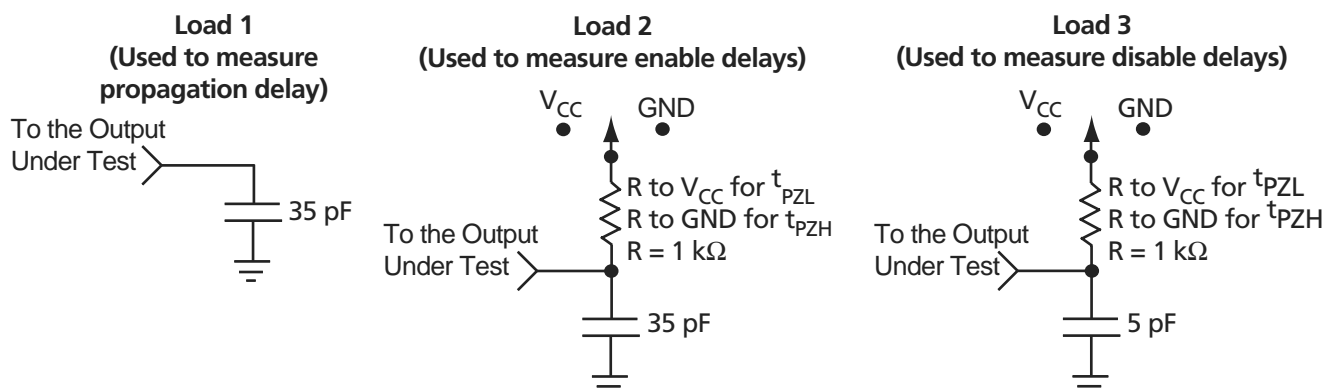


Figure 2-5 • AC Test Loads

## Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

## Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

## Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

## Temperature and Voltage Derating Factors

Table 2-13 • Temperature and Voltage Derating Factors  
(Normalized to Worst-Case Commercial,  $T_J = 70^\circ\text{C}$ ,  $V_{CCA} = 2.25\text{ V}$ )

<b>V<sub>CCA</sub></b>	<b>Junction Temperature (<math>T_J</math>)</b>						
	<b>-55°C</b>	<b>-40°C</b>	<b>0°C</b>	<b>25°C</b>	<b>70°C</b>	<b>85°C</b>	<b>125°C</b>
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-25 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.25\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing <sup>2, 3</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High		3.4		3.9		4.5		5.2		7.3	ns
t <sub>DHL</sub>	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t <sub>DHLS</sub>	Data-to-Pad High to Low—low slew		11.6		13.4		15.2		17.9		25.0	ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t <sub>ENZLS</sub>	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H		3.4		3.9		4.5		5.2		7.3	ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d <sub>TLH</sub> <sup>4</sup>	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d <sub>THL</sub> <sup>4</sup>	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d <sub>THLS</sub> <sup>4</sup>	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

**Note:**

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[LH|HL|HLS]}$  is the worst case delta value from the datasheet in ns/pF.

**Table 2-34 • A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	–3 Speed <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing <sup>2</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	2.1		2.4		2.8		3.2		4.5		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.1		2.4		2.8		3.2		4.5		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing <sup>4</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	1.9		2.2		2.5		2.9		4.1		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	2.5		2.9		3.3		3.9		5.4		ns
t <sub>DHLS</sub>	Data-to-Pad High to Low—low slew	6.6		7.6		8.6		10.1		14.2		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t <sub>ENZLS</sub>	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d <sub>THLS</sub> <sup>3</sup>	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

**Notes:**

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[HL|HL|HLS]}$  is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

Table 2-40 • A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing <sup>2</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	2.3		2.7		3.0		3.6		5.0		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.3		2.7		3.0		3.6		5.0		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing <sup>4</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	3.2		3.7		4.2		5.0		6.9		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	3.2		3.7		4.2		4.9		6.9		ns
t <sub>DHLS</sub>	Data-to-Pad High to Low—low slew	10.3		11.9		13.5		15.8		22.2		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t <sub>ENZLS</sub>	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	3.2		3.7		4.2		5.0		6.9		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	3.2		3.7		4.2		4.9		6.9		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.025		0.03		0.03		0.04		0.045		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.015		0.015		0.015		0.015		0.025		ns/pF
d <sub>THLS</sub> <sup>3</sup>	Delta High to Low—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

**Notes:**

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25  $\Omega$  resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[HLH|HLS]}$  is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
58	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

176-Pin TQFP		176-Pin TQFP		176-Pin TQFP		176-Pin TQFP	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
1	GND	37	I/O	73	I/O	109	V <sub>CCA</sub>
2	TDI, I/O	38	I/O	74	I/O	110	GND
3	I/O	39	I/O	75	I/O	111	I/O
4	I/O	40	I/O	76	I/O	112	I/O
5	I/O	41	I/O	77	I/O	113	I/O
6	I/O	42	I/O	78	I/O	114	I/O
7	I/O	43	I/O	79	I/O	115	I/O
8	I/O	44	GND	80	I/O	116	I/O
9	I/O	45	I/O	81	I/O	117	I/O
10	TMS	46	I/O	82	V <sub>CCI</sub>	118	I/O
11	V <sub>CCI</sub>	47	I/O	83	I/O	119	I/O
12	I/O	48	I/O	84	I/O	120	I/O
13	I/O	49	I/O	85	I/O	121	I/O
14	I/O	50	I/O	86	I/O	122	V <sub>CCA</sub>
15	I/O	51	I/O	87	TDO, I/O	123	GND
16	I/O	52	V <sub>CCI</sub>	88	I/O	124	V <sub>CCI</sub>
17	I/O	53	I/O	89	GND	125	I/O
18	I/O	54	I/O	90	I/O	126	I/O
19	I/O	55	I/O	91	I/O	127	I/O
20	I/O	56	I/O	92	I/O	128	I/O
21	GND	57	I/O	93	I/O	129	I/O
22	V <sub>CCA</sub>	58	I/O	94	I/O	130	I/O
23	GND	59	I/O	95	I/O	131	I/O
24	I/O	60	I/O	96	I/O	132	I/O
25	TRST, I/O	61	I/O	97	I/O	133	GND
26	I/O	62	I/O	98	V <sub>CCA</sub>	134	I/O
27	I/O	63	I/O	99	V <sub>CCI</sub>	135	I/O
28	I/O	64	PRB, I/O	100	I/O	136	I/O
29	I/O	65	GND	101	I/O	137	I/O
30	I/O	66	V <sub>CCA</sub>	102	I/O	138	I/O
31	I/O	67	NC	103	I/O	139	I/O
32	V <sub>CCI</sub>	68	I/O	104	I/O	140	V <sub>CCI</sub>
33	V <sub>CCA</sub>	69	HCLK	105	I/O	141	I/O
34	I/O	70	I/O	106	I/O	142	I/O
35	I/O	71	I/O	107	I/O	143	I/O
36	I/O	72	I/O	108	GND	144	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H6	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H7	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
H8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
H9	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O



## 256-Pin FBGA

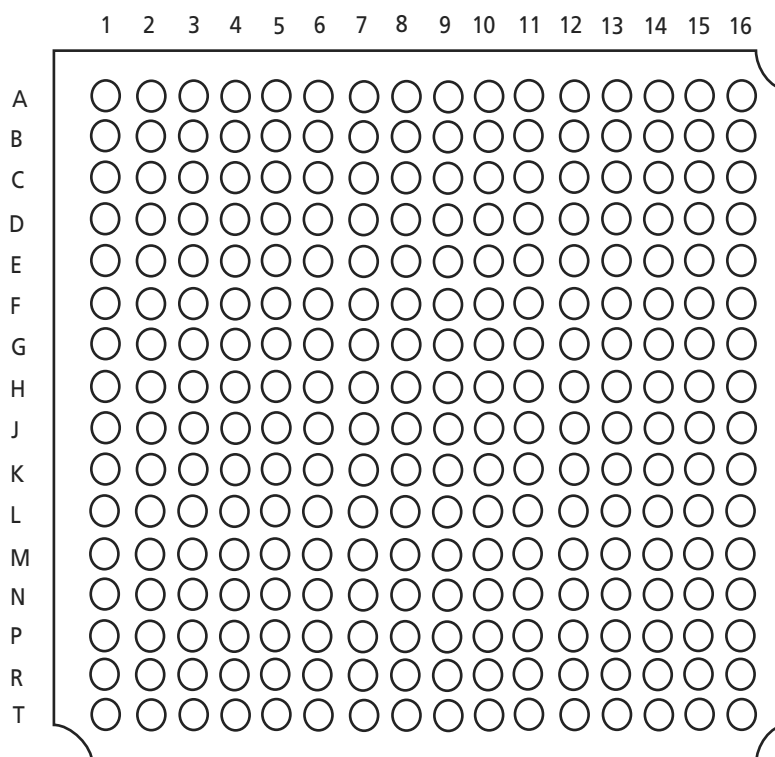


Figure 3-7 • 256-Pin FBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

## 484-Pin FBGA

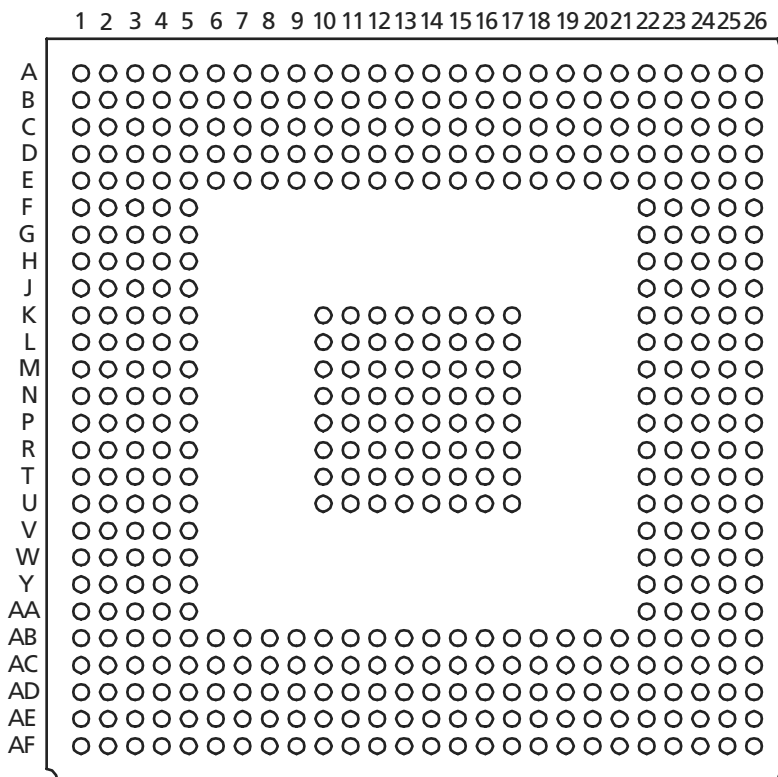


Figure 3-8 • 484-Pin FBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC
A2	NC*	NC
A3	NC*	I/O
A4	NC*	I/O
A5	NC*	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC*	I/O
A12	NC*	I/O
A13	I/O	I/O
A14	NC*	NC
A15	NC*	I/O
A16	NC*	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC*	I/O
A22	NC*	I/O
A23	NC*	I/O
A24	NC*	I/O
A25	NC*	NC
A26	NC*	NC
AA1	NC*	I/O
AA2	NC*	I/O
AA3	V <sub>CCA</sub>	V <sub>CCA</sub>
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AA26	NC*	I/O
AB1	NC*	NC
AB2	V <sub>CCI</sub>	V <sub>CCI</sub>
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC*	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V <sub>CCA</sub>	V <sub>CCA</sub>
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC*	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC*	I/O
AB26	NC*	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC*	I/O
AC5	V <sub>CCI</sub>	V <sub>CCI</sub>
AC6	I/O	I/O
AC7	V <sub>CCI</sub>	V <sub>CCI</sub>
AC8	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V <sub>CCI</sub>	V <sub>CCI</sub>
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC*	I/O
AC24	I/O	I/O
AC25	NC*	I/O
AC26	NC*	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V <sub>CCI</sub>	V <sub>CCI</sub>
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V <sub>CCI</sub>	V <sub>CCI</sub>
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V <sub>CCI</sub>	V <sub>CCI</sub>

**Note:** \*These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V <sub>CCI</sub>	V <sub>CCI</sub>
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V <sub>CCI</sub>	V <sub>CCI</sub>
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V <sub>CCI</sub>	V <sub>CCI</sub>
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V <sub>CCA</sub>	V <sub>CCA</sub>
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V <sub>CCI</sub>	V <sub>CCI</sub>
E26	GND	GND
F1	V <sub>CCI</sub>	V <sub>CCI</sub>
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V <sub>CCA</sub>	V <sub>CCA</sub>
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V <sub>CCI</sub>	V <sub>CCI</sub>
J26	NC*	I/O
K1	I/O	I/O
K2	V <sub>CCI</sub>	V <sub>CCI</sub>
K3	I/O	I/O
K4	I/O	I/O
K5	V <sub>CCA</sub>	V <sub>CCA</sub>

**Note:** \*These pins must be left floating on the A54SX32A device.

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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