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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	69
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	84-CQFP Exposed Pad and Tie Bar
Supplier Device Package	84-CQFP (42x42)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/5962-0151801qzc

General Description

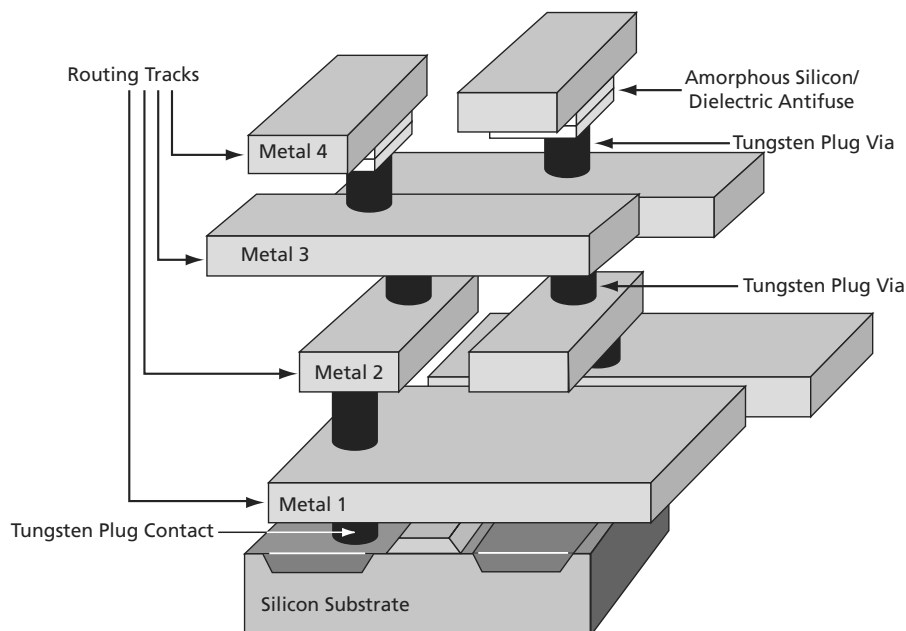
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

Pin Description

CLKA/B, I/O **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND **Ground**

Low supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CC} **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CC} power pins in the device should be connected.

V_{CCA} **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

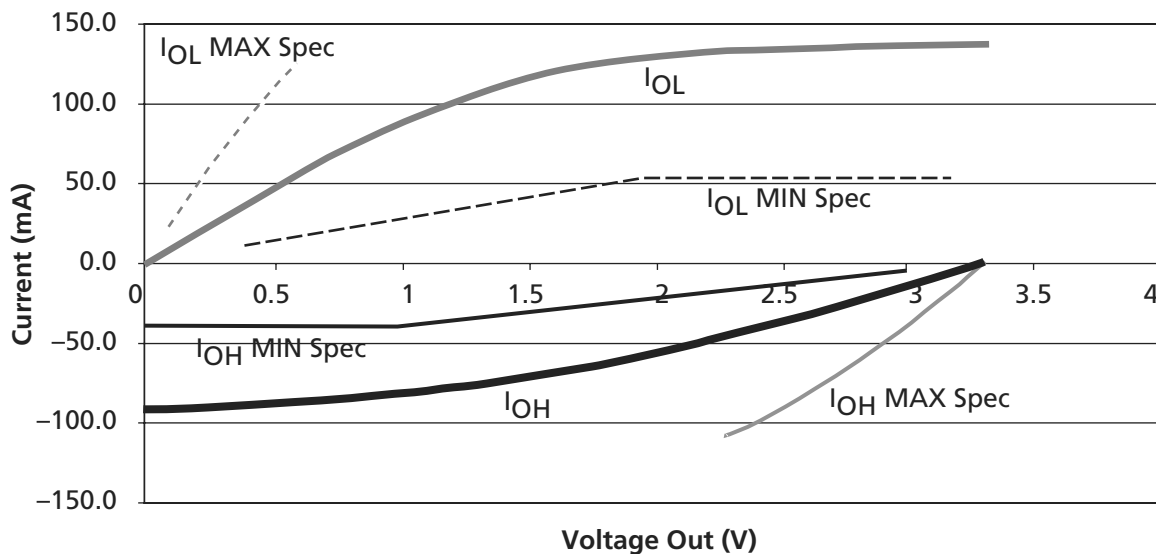


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}\text{C/W} \text{ is taken from Table 2-12 on page 2-11}$$

$$T_A = 125^{\circ}\text{C} \text{ is the maximum limit of ambient (from the datasheet)}$$

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_J = 110^{\circ}\text{C}$$

$$T_A = 70^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 18.0^{\circ}\text{C/W}$$

$$\theta_{JC} = 3.2^{\circ}\text{C/W}$$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{3.00 \text{ W}} = 13.33^{\circ}\text{C/W}$$

EQ 2-13

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.25\text{ V}$)

V_{CCA}	Junction Temperature (T_J)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-17 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.3		1.5		2.3	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.2		1.4		2.0	ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.8	ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.3		1.5		2.1	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.9	ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		1.0		1.1		1.5	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{1,2}										
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-23 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)	1.2		1.4		1.6		1.8		2.8		ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)	1.0		1.1		1.3		1.5		2.2		ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew	0.3		0.3		0.4		0.4		0.6		ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency	357		294		263		227		167		MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)	1.0		1.2		1.3		1.5		2.1		ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)	1.1		1.3		1.4		1.7		2.3		ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.3		1.5		1.7		2.4		ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.7		ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.0		2.8		ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (50% Load)	0.8		0.9		1.0		1.2		1.7		ns
t _{RCKSW}	Maximum Skew (100% Load)	1.0		1.1		1.3		1.5		2.1		ns

Note: *All –3 speed grades have been discontinued.

Table 2-35 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays³												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-36 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		2.9		3.4		4.8	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.7		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.3		3.8		4.5		6.2	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.0		4.7		6.6	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.8		2.1		2.4		2.8		3.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.8		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.6		3.0		3.3		3.9		5.5	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.2		5.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-36 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Package Pin Assignments

208-Pin PQFP

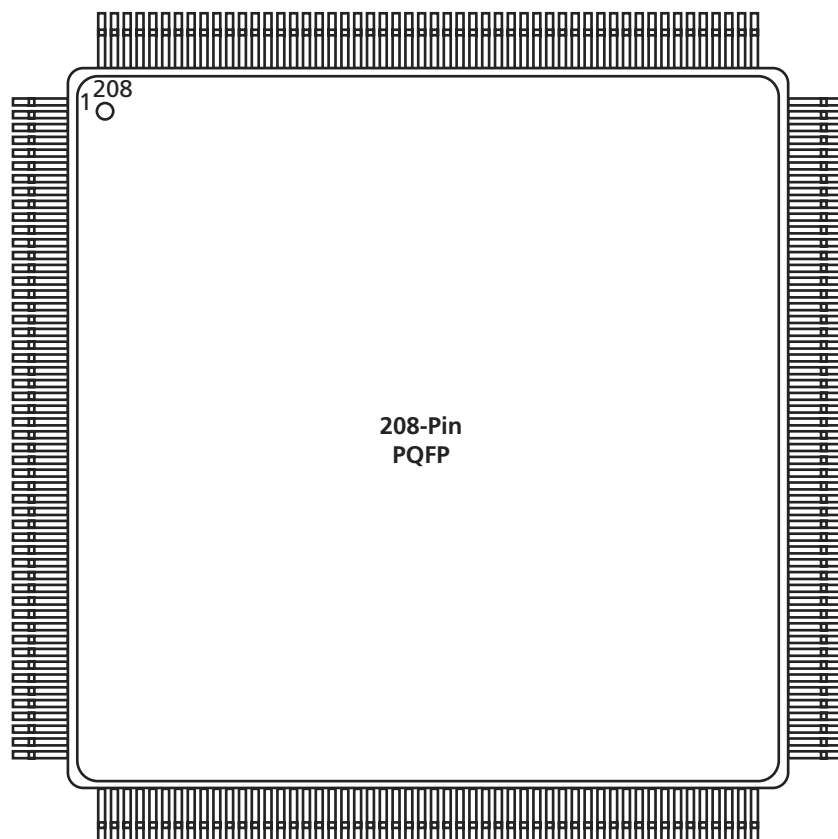


Figure 3-1 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V _{CCI}	V _{CCI}	V _{CCI}
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V _{CCA}	V _{CCA}	V _{CCA}
H6	V _{CCA}	V _{CCA}	V _{CCA}
H7	V _{CCI}	V _{CCI}	V _{CCI}
H8	V _{CCI}	V _{CCI}	V _{CCI}
H9	V _{CCA}	V _{CCA}	V _{CCA}
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V _{CCA}	V _{CCA}	V _{CCA}

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V _{CCA}	V _{CCA}	V _{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

484-Pin FBGA

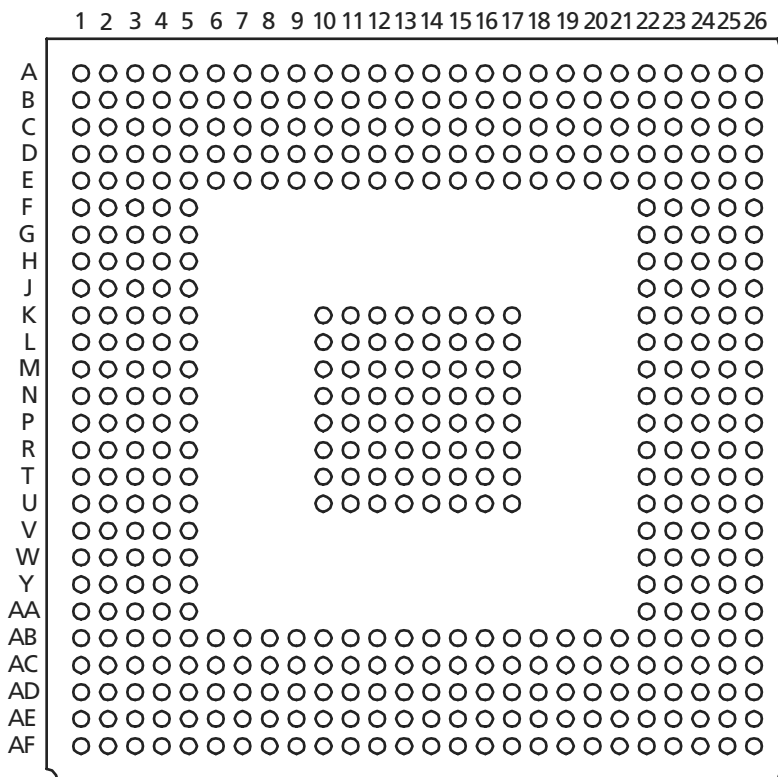


Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V _{CCI}	V _{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V _{CCI}	V _{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V _{CCI}	V _{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V _{CCA}	V _{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V _{CCI}	V _{CCI}
E26	GND	GND
F1	V _{CCI}	V _{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V _{CCA}	V _{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V _{CCI}	V _{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V _{CCI}	V _{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V _{CCA}	V _{CCA}

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC *	NC
K25	NC *	I/O
K26	NC *	I/O
L1	NC *	I/O
L2	NC *	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC *	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC *	I/O
M26	NC *	I/O
N1	I/O	I/O
N2	V _{CCI}	V _{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V _{CCA}	V _{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC *	NC
P1	NC *	I/O
P2	NC *	I/O
P3	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
P4	I/O	I/O
P5	V _{CCA}	V _{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V _{CCI}	V _{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC *	I/O
R2	NC *	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	NC *	I/O
R26	NC *	I/O
T1	NC *	I/O
T2	NC *	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC *	I/O
T26	NC *	I/O
U1	I/O	I/O
U2	V _{CCI}	V _{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V _{CCI}	V _{CCI}
U26	I/O	I/O
V1	NC *	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
V2	NC *	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V _{CCA}	V _{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC *	I/O
V26	NC *	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V _{CCA}	V _{CCA}
W24	I/O	I/O
W25	NC *	I/O
W26	NC *	I/O
Y1	NC *	I/O
Y2	NC *	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC *	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V _{CCI}	V _{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

Previous Version	Changes in Current Version (v5.3)	Page
v4.0 (continued)	Table 2-12 was updated.	2-11
	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The "Clock Resources" section was updated.	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new.	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23