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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	12000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08a-1fgg144

Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Speed Grade and Temperature Grade Matrix

	F	Std	-1	-2	-3
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

Notes:

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.

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SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

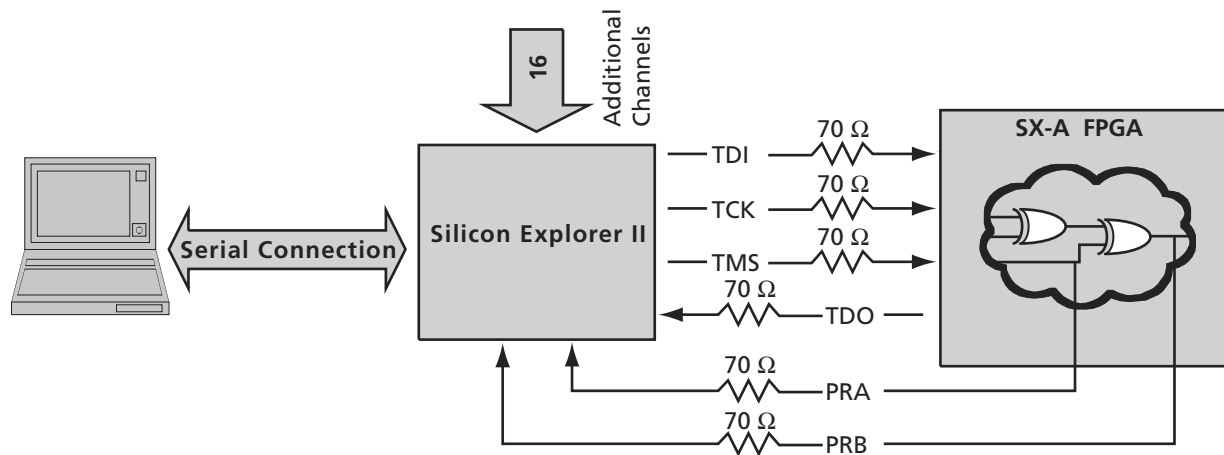


Figure 1-13 • Probe Setup

Pin Description

CLKA/B, I/O **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND **Ground**

Low supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CC} **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CC} power pins in the device should be connected.

V_{CCA} **Supply Voltage**

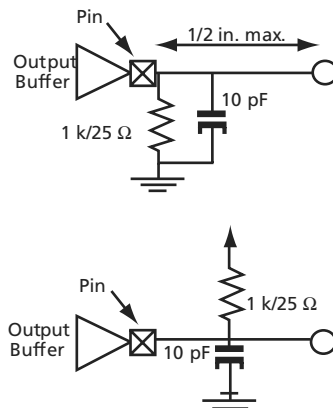
Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

Table 2-10 • AC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CCI}^1$	$-12V_{CCI}$	–	mA
		$0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}^1$	$(-17.1(V_{CCI} - V_{OUT}))$	–	mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}^{1,2}$	–	EQ 2-3 on page 2-7	–
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$	–	$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \geq 0.6V_{CCI}^1$	$16V_{CCI}$	–	mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^1$	$(26.7V_{OUT})$	–	mA
		$0.18V_{CCI} > V_{OUT} > 0^{1,2}$	–	EQ 2-4 on page 2-7	–
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$	–	$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI} - 0.6V_{CCI}$ load ³	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI} - 0.2V_{CCI}$ load ³	1	4	V/ns

Notes:

1. Refer to the *VII* curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 2-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{\text{DC}} = I_{\text{standby}} * V_{\text{CCA}}$$

EQ 2-6

Note: For other combinations of temperature and voltage settings, refer to the *eX, SX-A and RT54SX-S Power Calculator*.

AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{\text{AC}} = P_{\text{C-cells}} + P_{\text{R-cells}} + P_{\text{CLKA}} + P_{\text{CLKB}} + P_{\text{HCLK}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 2-7

or:

$$P_{\text{AC}} = V_{\text{CCA}}^2 * [(m * C_{\text{EQCM}} * f_m)_{\text{C-cells}} + (m * C_{\text{EQSM}} * f_m)_{\text{R-cells}} + (n * C_{\text{EQI}} * f_n)_{\text{Input Buffer}} + (p * (C_{\text{EQO}} + C_L) * f_p)_{\text{Output Buffer}} + (0.5 * (q_1 * C_{\text{EQCR}} * f_{q1}) + (r_1 * f_{q1}))_{\text{CLKA}} + (0.5 * (q_2 * C_{\text{EQCR}} * f_{q2}) + (r_2 * f_{q2}))_{\text{CLKB}} + (0.5 * (s_1 * C_{\text{EQHV}} * f_{s1}) + (C_{\text{EQHF}} * f_{s1}))_{\text{HCLK}}]$$

EQ 2-8

Output Buffer Delays

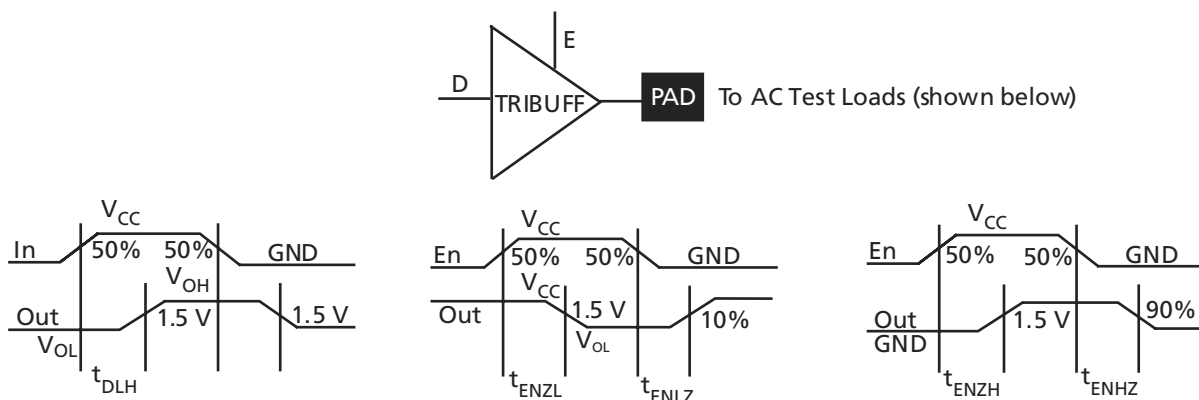


Figure 2-4 • Output Buffer Delays

AC Test Loads

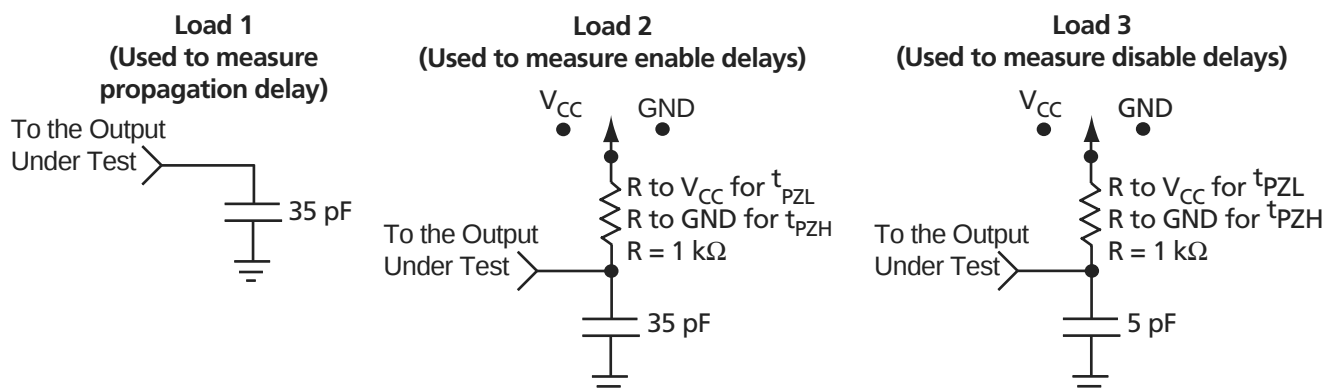


Figure 2-5 • AC Test Loads

Table 2-14 • A54SX08A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays²										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-31 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-32 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{2,3}												
t _{DLH}	Data-to-Pad Low to High	3.3		3.8		4.2		5.0		7.0		ns
t _{DHL}	Data-to-Pad High to Low	2.5		2.9		3.2		3.8		5.3		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	11.1		12.8		14.5		17.0		23.8		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8		3.2		3.7		5.2		ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8		13.7		15.5		18.2		25.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.3		3.8		4.2		5.0		7.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5		2.8		3.3		4.7		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.2		3.8		5.3		ns
d _{TLH} ⁴	Delta Low to High	0.031		0.037		0.043		0.051		0.071		ns/pF
d _{THL} ⁴	Delta High to Low	0.017		0.017		0.023		0.023		0.037		ns/pF
d _{THLS} ⁴	Delta High to Low—low slew	0.057		0.06		0.071		0.086		0.117		ns/pF

Note:

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

176-Pin TQFP	
Pin Number	A54SX32A Function
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V _{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V _{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
A1	GND	AA15	I/O	AC6	I/O	B20	I/O
A2	GND	AA16	I/O	AC7	I/O	B21	I/O
A3	V _{CCI}	AA17	I/O	AC8	I/O	B22	GND
A4	NC	AA18	I/O	AC9	V _{CCI}	B23	V _{CCI}
A5	I/O	AA19	I/O	AC10	I/O	C1	NC
A6	I/O	AA20	TDO, I/O	AC11	I/O	C2	TDI, I/O
A7	V _{CCI}	AA21	V _{CCI}	AC12	I/O	C3	GND
A8	NC	AA22	I/O	AC13	I/O	C4	I/O
A9	I/O	AA23	V _{CCI}	AC14	I/O	C5	I/O
A10	I/O	AB1	I/O	AC15	NC	C6	I/O
A11	I/O	AB2	GND	AC16	I/O	C7	I/O
A12	I/O	AB3	I/O	AC17	I/O	C8	I/O
A13	CLKB	AB4	I/O	AC18	I/O	C9	I/O
A14	I/O	AB5	I/O	AC19	I/O	C10	I/O
A15	I/O	AB6	I/O	AC20	I/O	C11	I/O
A16	I/O	AB7	I/O	AC21	NC	C12	I/O
A17	I/O	AB8	I/O	AC22	V _{CCI}	C13	I/O
A18	I/O	AB9	I/O	AC23	GND	C14	I/O
A19	I/O	AB10	I/O	B1	V _{CCI}	C15	I/O
A20	I/O	AB11	PRB, I/O	B2	GND	C16	I/O
A21	NC	AB12	I/O	B3	I/O	C17	I/O
A22	V _{CCI}	AB13	HCLK	B4	I/O	C18	I/O
A23	GND	AB14	I/O	B5	I/O	C19	I/O
AA1	V _{CCI}	AB15	I/O	B6	I/O	C20	I/O
AA2	I/O	AB16	I/O	B7	I/O	C21	V _{CCI}
AA3	GND	AB17	I/O	B8	I/O	C22	GND
AA4	I/O	AB18	I/O	B9	I/O	C23	NC
AA5	I/O	AB19	I/O	B10	I/O	D1	I/O
AA6	I/O	AB20	I/O	B11	I/O	D2	I/O
AA7	I/O	AB21	I/O	B12	PRA, I/O	D3	I/O
AA8	I/O	AB22	GND	B13	CLKA	D4	TCK, I/O
AA9	I/O	AB23	I/O	B14	I/O	D5	I/O
AA10	I/O	AC1	GND	B15	I/O	D6	I/O
AA11	I/O	AC2	V _{CCI}	B16	I/O	D7	I/O
AA12	I/O	AC3	NC	B17	I/O	D8	I/O
AA13	I/O	AC4	I/O	B18	I/O	D9	I/O
AA14	I/O	AC5	I/O	B19	I/O	D10	I/O

144-Pin FBGA

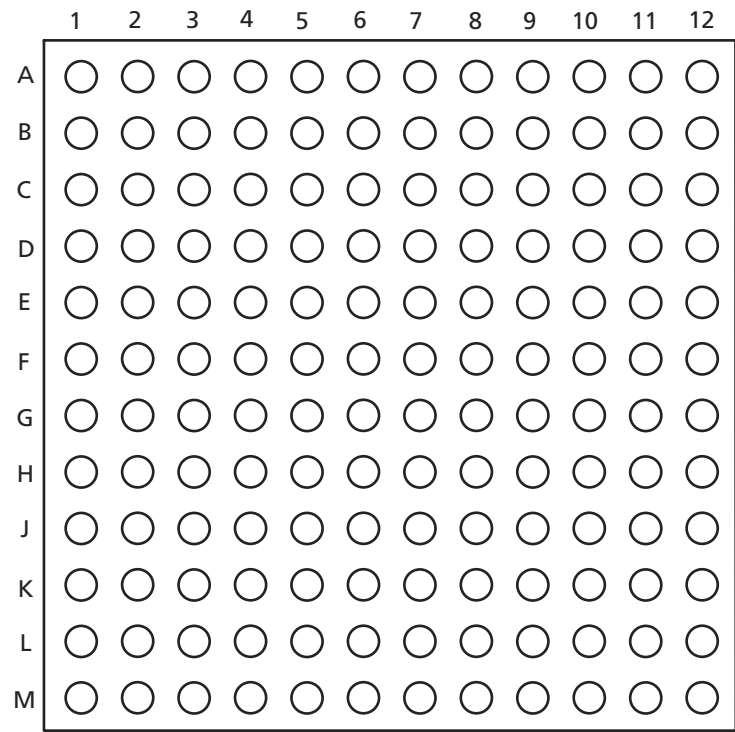


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

256-Pin FBGA

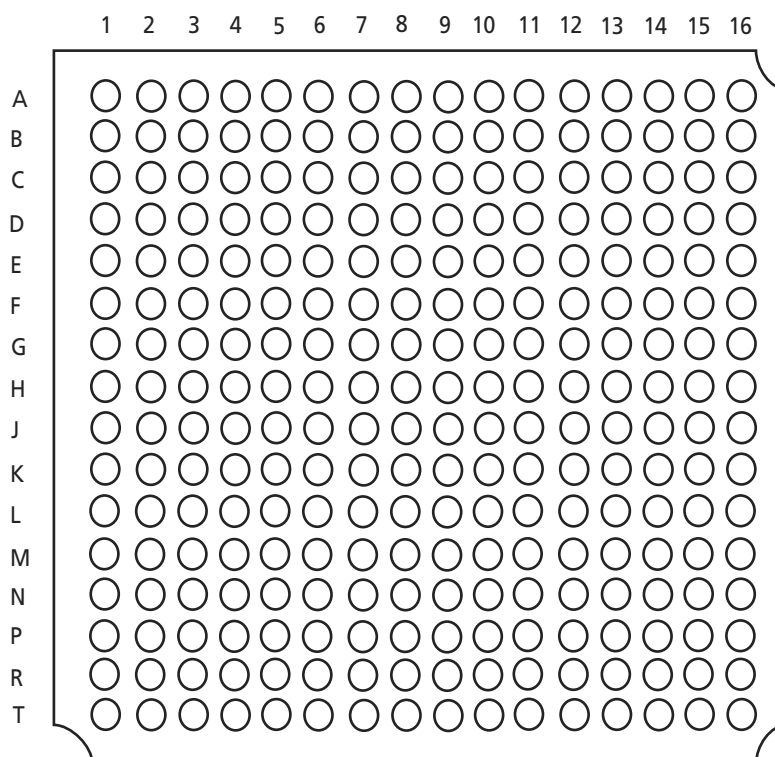


Figure 3-7 • 256-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
K5	I/O	I/O	I/O
K6	V _{CCI}	V _{CCI}	V _{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V _{CCI}	V _{CCI}	V _{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V _{CCI}	V _{CCI}	V _{CCI}
L8	V _{CCI}	V _{CCI}	V _{CCI}
L9	V _{CCI}	V _{CCI}	V _{CCI}
L10	V _{CCI}	V _{CCI}	V _{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V _{CCA}	V _{CCA}	V _{CCA}
P14	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V _{CCA}	V _{CCA}	V _{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V _{CCI}	V _{CCI}
AD24	NC*	I/O
AD25	NC*	I/O
AD26	NC*	I/O
AE1	NC*	NC
AE2	I/O	I/O
AE3	NC*	I/O
AE4	NC*	I/O
AE5	NC*	I/O
AE6	NC*	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	NC*	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	NC*	I/O
AE16	NC*	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	NC*	I/O
AE22	NC*	I/O
AE23	NC*	I/O
AE24	NC*	I/O
AE25	NC*	NC
AE26	NC*	NC

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AF1	NC*	NC
AF2	NC*	NC
AF3	NC	I/O
AF4	NC*	I/O
AF5	NC*	I/O
AF6	NC*	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	NC*	I/O
AF12	NC*	NC
AF13	HCLK	HCLK
AF14	I/O	QCLKB
AF15	NC*	I/O
AF16	NC*	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	NC*	I/O
AF21	NC*	I/O
AF22	NC*	I/O
AF23	NC*	I/O
AF24	NC*	I/O
AF25	NC*	NC
AF26	NC*	NC
B1	NC*	NC
B2	NC*	NC
B3	NC*	I/O
B4	NC*	I/O
B5	NC*	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
B10	I/O	I/O
B11	NC*	I/O
B12	NC*	I/O
B13	V _{CCI}	V _{CCI}
B14	CLKA	CLKA
B15	NC*	I/O
B16	NC*	I/O
B17	I/O	I/O
B18	V _{CCI}	V _{CCI}
B19	I/O	I/O
B20	I/O	I/O
B21	NC*	I/O
B22	NC*	I/O
B23	NC*	I/O
B24	NC*	I/O
B25	I/O	I/O
B26	NC*	NC
C1	NC*	I/O
C2	NC*	I/O
C3	NC*	I/O
C4	NC*	I/O
C5	I/O	I/O
C6	V _{CCI}	V _{CCI}
C7	I/O	I/O
C8	I/O	I/O
C9	V _{CCI}	V _{CCI}
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	PRA, I/O	PRA, I/O
C14	I/O	I/O
C15	I/O	QCLKD
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200

Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom

Phone +44 (0) 1276 609 300

Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671

Fax +81.03.3445.7668

www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460

Fax +852 2185 6488

www.actel.com.cn