



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

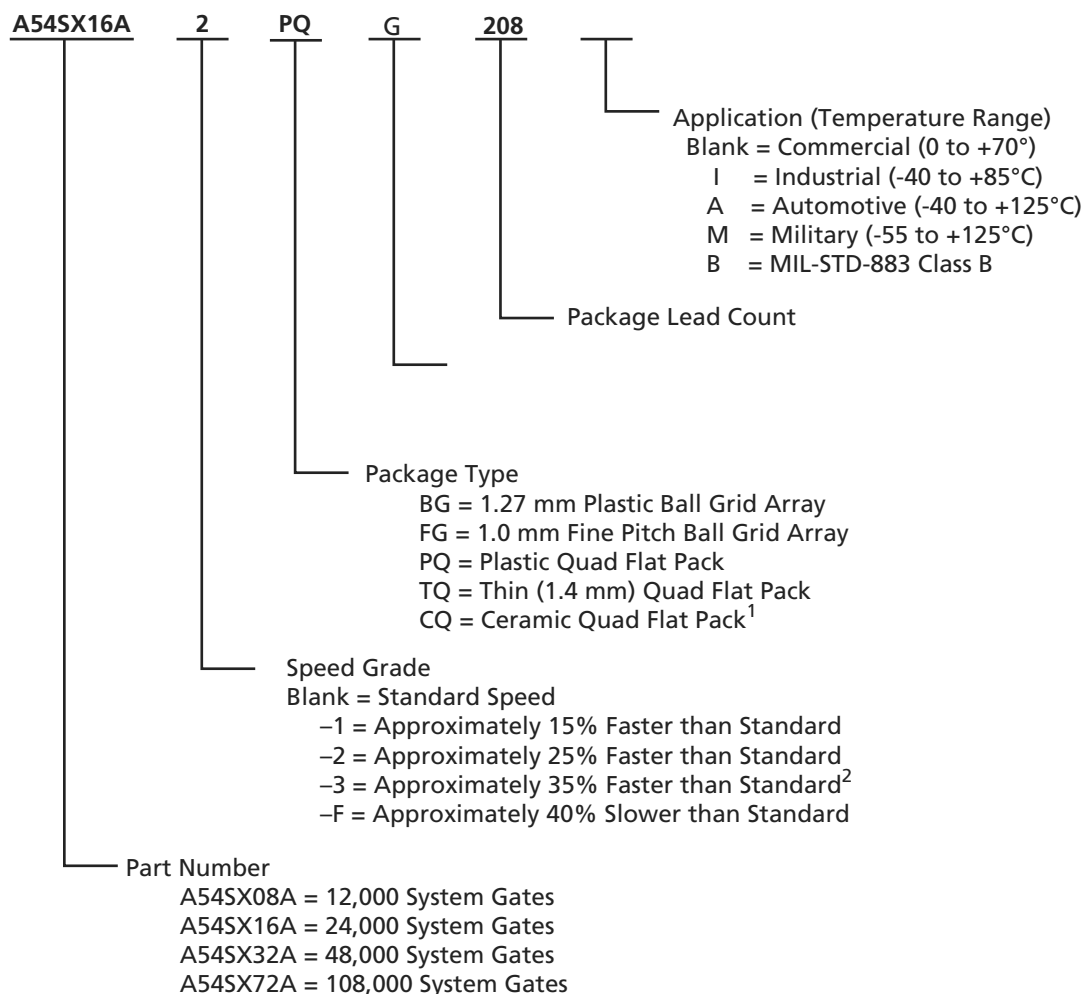
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	12000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08a-1fgg144i

Ordering Information



Notes:

- For more information about the CQFP package options, refer to the HiRel SX-A datasheet.
- All -3 speed grades have been discontinued.

Device Resources

Device	User I/Os (Including Clock Buffers)							
	208-Pin PQFP	100-Pin TQFP	144-Pin TQFP	176-Pin TQFP	329-Pin PBGA	144-Pin FBGA	256-Pin FBGA	484-Pin FBGA
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices

http://www.actel.com/documents/GlobalClk_AN.pdf

Using A54SX72A and RT54SX72S Quadrant Clocks

http://www.actel.com/documents/QCLK_AN.pdf

Implementation of Security in Actel Antifuse FPGAs

http://www.actel.com/documents/Antifuse_Security_AN.pdf

Actel eX, SX-A, and RTSX-S I/Os

http://www.actel.com/documents/AntifuseIO_AN.pdf

Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

http://www.actel.com/documents/HotSwapColdSparing_AN.pdf

Programming Antifuse Devices

http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs

http://www.actel.com/documents/HR SXA_DS.pdf

SX-A Automotive Family FPGAs

http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide

http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −1 mA)	0.9 V _{CCI}		0.9 V _{CCI}		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OH} = −8 mA)	2.4		2.4		V
V _{OL}	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)	0.4		0.4		V
	V _{CCI} = Minimum V _I = V _{IH} or V _{IL}	(I _{OL} = 12 mA)	0.4		0.4		V
V _{IL}	Input Low Voltage		0.8		0.8		V
V _{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		−10	10	−10	10	μA
I _{OZ}	Tristate Output Leakage Current		−10	10	−10	10	μA
t _R , t _F	Input Transition Time t _R , t _F		10		10		ns
C _{IO}	I/O Capacitance		10		10		pF
I _{CC}	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100 μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100 μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1 mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	5.75	1.7	5.75	V
I _{IL} /I _{IH}	Input Leakage Current, V _{IN} = V _{CCI} or GND		-10	10	-10	10	μA
I _{OZ}	Tristate Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: *The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) = f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX*, *SX-A* and *RT54SX-S* *Power Calculator* worksheet.

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_C = Ambient temperature
- P = total power dissipated by the device

Table 2-12 • Package Thermal Characteristics

Package Type	Pin Count	θ_{JC}	θ_{JA}			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP) ¹	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader ²	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

- The A54SX08A PQ208 has no heat spreader.
- The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.25\text{ V}$)

V_{CCA}	Junction Temperature (T_J)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{1,2}										
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-28 • A54SX32A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.9		1.1		1.2		1.4		1.9	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		1.4		1.6		1.8		2.1		2.9	ns
Input Module Predicted Routing Delays³												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-29 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t _{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t _{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f _{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t _{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t _{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t _{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t _{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t _{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t _{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d _{TLH} ³	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t _{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d _{TLH} ³	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V _{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

100-Pin TQFP

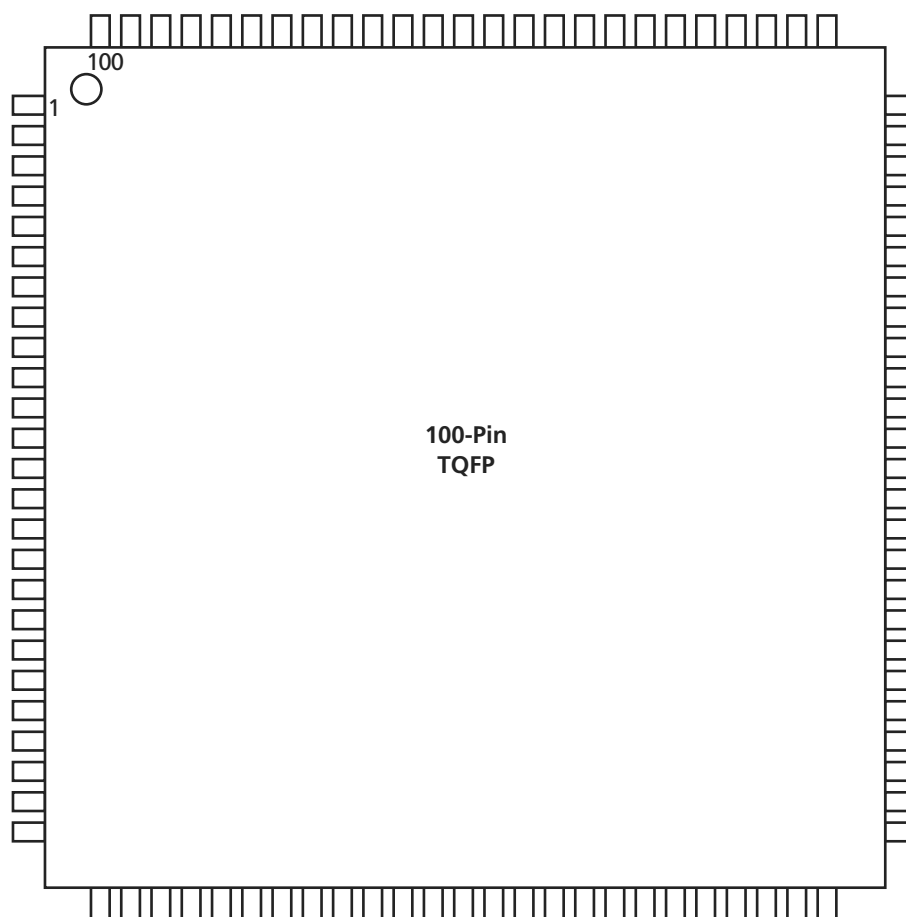


Figure 3-2 • 100-Pin TQFP

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V _{CCA}	V _{CCA}	V _{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V _{CCI}	V _{CCI}	V _{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V _{CCI}	V _{CCI}	V _{CCI}
30	V _{CCA}	V _{CCA}	V _{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V _{CCA}	V _{CCA}	V _{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V _{CCI}	V _{CCI}	V _{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O

176-Pin TQFP		176-Pin TQFP		176-Pin TQFP		176-Pin TQFP	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
1	GND	37	I/O	73	I/O	109	V _{CCA}
2	TDI, I/O	38	I/O	74	I/O	110	GND
3	I/O	39	I/O	75	I/O	111	I/O
4	I/O	40	I/O	76	I/O	112	I/O
5	I/O	41	I/O	77	I/O	113	I/O
6	I/O	42	I/O	78	I/O	114	I/O
7	I/O	43	I/O	79	I/O	115	I/O
8	I/O	44	GND	80	I/O	116	I/O
9	I/O	45	I/O	81	I/O	117	I/O
10	TMS	46	I/O	82	V _{CCI}	118	I/O
11	V _{CCI}	47	I/O	83	I/O	119	I/O
12	I/O	48	I/O	84	I/O	120	I/O
13	I/O	49	I/O	85	I/O	121	I/O
14	I/O	50	I/O	86	I/O	122	V _{CCA}
15	I/O	51	I/O	87	TDO, I/O	123	GND
16	I/O	52	V _{CCI}	88	I/O	124	V _{CCI}
17	I/O	53	I/O	89	GND	125	I/O
18	I/O	54	I/O	90	I/O	126	I/O
19	I/O	55	I/O	91	I/O	127	I/O
20	I/O	56	I/O	92	I/O	128	I/O
21	GND	57	I/O	93	I/O	129	I/O
22	V _{CCA}	58	I/O	94	I/O	130	I/O
23	GND	59	I/O	95	I/O	131	I/O
24	I/O	60	I/O	96	I/O	132	I/O
25	TRST, I/O	61	I/O	97	I/O	133	GND
26	I/O	62	I/O	98	V _{CCA}	134	I/O
27	I/O	63	I/O	99	V _{CCI}	135	I/O
28	I/O	64	PRB, I/O	100	I/O	136	I/O
29	I/O	65	GND	101	I/O	137	I/O
30	I/O	66	V _{CCA}	102	I/O	138	I/O
31	I/O	67	NC	103	I/O	139	I/O
32	V _{CCI}	68	I/O	104	I/O	140	V _{CCI}
33	V _{CCA}	69	HCLK	105	I/O	141	I/O
34	I/O	70	I/O	106	I/O	142	I/O
35	I/O	71	I/O	107	I/O	143	I/O
36	I/O	72	I/O	108	GND	144	I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
A1	GND	AA15	I/O	AC6	I/O	B20	I/O
A2	GND	AA16	I/O	AC7	I/O	B21	I/O
A3	V _{CCI}	AA17	I/O	AC8	I/O	B22	GND
A4	NC	AA18	I/O	AC9	V _{CCI}	B23	V _{CCI}
A5	I/O	AA19	I/O	AC10	I/O	C1	NC
A6	I/O	AA20	TDO, I/O	AC11	I/O	C2	TDI, I/O
A7	V _{CCI}	AA21	V _{CCI}	AC12	I/O	C3	GND
A8	NC	AA22	I/O	AC13	I/O	C4	I/O
A9	I/O	AA23	V _{CCI}	AC14	I/O	C5	I/O
A10	I/O	AB1	I/O	AC15	NC	C6	I/O
A11	I/O	AB2	GND	AC16	I/O	C7	I/O
A12	I/O	AB3	I/O	AC17	I/O	C8	I/O
A13	CLKB	AB4	I/O	AC18	I/O	C9	I/O
A14	I/O	AB5	I/O	AC19	I/O	C10	I/O
A15	I/O	AB6	I/O	AC20	I/O	C11	I/O
A16	I/O	AB7	I/O	AC21	NC	C12	I/O
A17	I/O	AB8	I/O	AC22	V _{CCI}	C13	I/O
A18	I/O	AB9	I/O	AC23	GND	C14	I/O
A19	I/O	AB10	I/O	B1	V _{CCI}	C15	I/O
A20	I/O	AB11	PRB, I/O	B2	GND	C16	I/O
A21	NC	AB12	I/O	B3	I/O	C17	I/O
A22	V _{CCI}	AB13	HCLK	B4	I/O	C18	I/O
A23	GND	AB14	I/O	B5	I/O	C19	I/O
AA1	V _{CCI}	AB15	I/O	B6	I/O	C20	I/O
AA2	I/O	AB16	I/O	B7	I/O	C21	V _{CCI}
AA3	GND	AB17	I/O	B8	I/O	C22	GND
AA4	I/O	AB18	I/O	B9	I/O	C23	NC
AA5	I/O	AB19	I/O	B10	I/O	D1	I/O
AA6	I/O	AB20	I/O	B11	I/O	D2	I/O
AA7	I/O	AB21	I/O	B12	PRA, I/O	D3	I/O
AA8	I/O	AB22	GND	B13	CLKA	D4	TCK, I/O
AA9	I/O	AB23	I/O	B14	I/O	D5	I/O
AA10	I/O	AC1	GND	B15	I/O	D6	I/O
AA11	I/O	AC2	V _{CCI}	B16	I/O	D7	I/O
AA12	I/O	AC3	NC	B17	I/O	D8	I/O
AA13	I/O	AC4	I/O	B18	I/O	D9	I/O
AA14	I/O	AC5	I/O	B19	I/O	D10	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V _{CCI}	V _{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V _{CCI}	V _{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V _{CCI}	V _{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V _{CCA}	V _{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V _{CCI}	V _{CCI}
E26	GND	GND
F1	V _{CCI}	V _{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V _{CCA}	V _{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V _{CCI}	V _{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V _{CCI}	V _{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V _{CCA}	V _{CCA}

Note: *These pins must be left floating on the A54SX32A device.

Actel and the Actel logo are registered trademarks of Actel Corporation.
All other trademarks are the property of their owners.



www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200

Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom

Phone +44 (0) 1276 609 300

Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671

Fax +81.03.3445.7668

www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460

Fax +852 2185 6488

www.actel.com.cn