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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 768 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 130 |
| Number of Gates | 12000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx08a-1pqg208 |

## Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

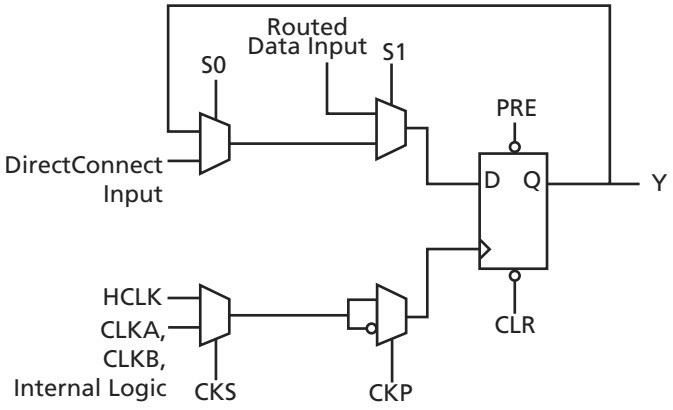


*Figure 1-2* • **R-Cell**

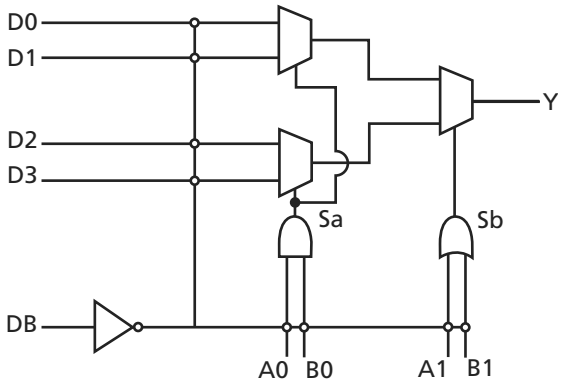


*Figure 1-3* • **C-Cell**

## Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Device*s and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

*Table 1-1* • **SX-A Clock Resources**

| | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---|---|---|---|---|
| Routed Clocks (CLKA, CLKB) | 2 | 2 | 2 | 2 |
| Hardwired Clocks (HCLK) | 1 | 1 | 1 | 1 |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0 | 0 | 0 | 4 |

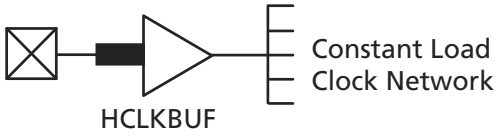


*Figure 1-7* • **SX-A HCLK Clock Buffer**

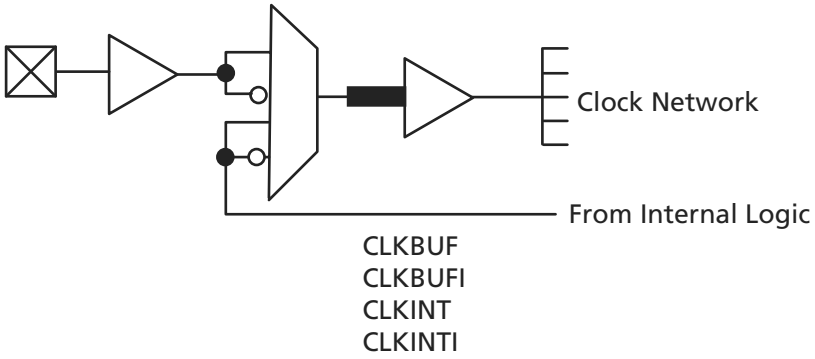


*Figure 1-8* • **SX-A Routed Clock Buffer**

## SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

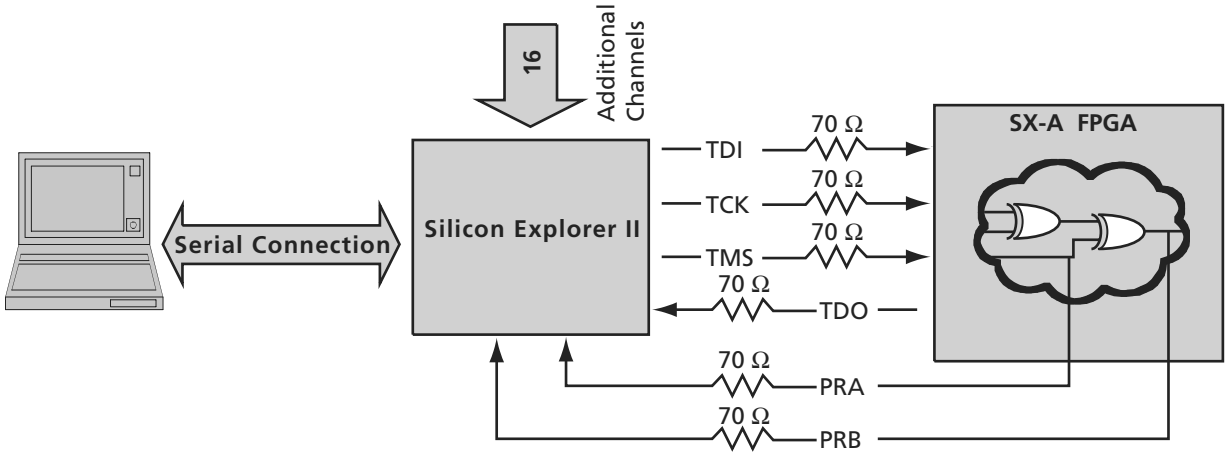


*Figure 1-13* • **Probe Setup**

## Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) =f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

# Thermal Characteristics

## Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

*EQ 2-9*

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

*EQ 2-10*

Where:

$\theta_{JA}$ = Junction-to-air thermal resistance

$\theta_{JC}$ = Junction-to-case thermal resistance

$T_J$ = Junction temperature

$T_A$ = Ambient temperature

$T_C$ = Ambient temperature

P = total power dissipated by the device

*Table 2-12* • **Package Thermal Characteristics**

| Package Type | Pin Count | $\theta_{JC}$ | $\theta_{JA}$ | | | Units |
|---|---|---|---|---|---|---|
| | | | Still Air | 1.0 m/s 200 ft./min. | 2.5 m/s 500 ft./min. | |
| Thin Quad Flat Pack (TQFP) | 100 | 14 | 33.5 | 27.4 | 25 | °C/W |
| Thin Quad Flat Pack (TQFP) | 144 | 11 | 33.5 | 28 | 25.7 | °C/W |
| Thin Quad Flat Pack (TQFP) | 176 | 11 | 24.7 | 19.9 | 18 | °C/W |
| Plastic Quad Flat Pack (PQFP)[1] | 208 | 8 | 26.1 | 22.5 | 20.8 | °C/W |
| Plastic Quad Flat Pack (PQFP) with Heat Spreader[2] | 208 | 3.8 | 16.2 | 13.3 | 11.9 | °C/W |
| Plastic Ball Grid Array (PBGA) | 329 | 3 | 17.1 | 13.8 | 12.8 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 144 | 3.8 | 26.9 | 22.9 | 21.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.8 | 26.6 | 22.8 | 21.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 484 | 3.2 | 18 | 14.7 | 13.6 | °C/W |

***Notes:***

1. *The A54SX08A PQ208 has no heat spreader.*
2. *The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.*

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 2-14*

where:

$\theta_{CS}$ = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

# Output Buffer Delays

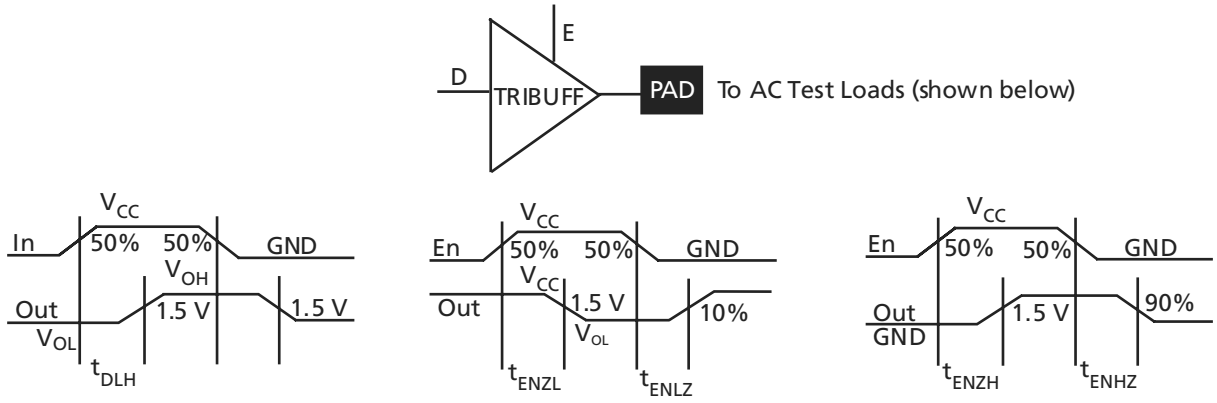


*Figure 2-4* • **Output Buffer Delays**

# AC Test Loads

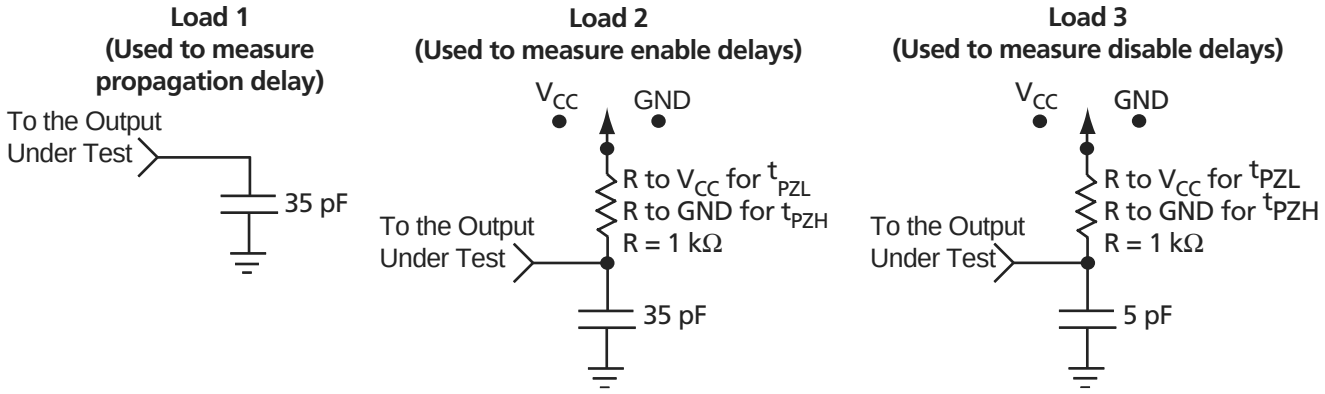


*Figure 2-5* • **AC Test Loads**

*Table 2-16* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.6 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.5 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |

*Table 2-18* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.3 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **2.5 V LVCMOS Output Module Timing[1,2]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 13.3 | | 15.1 | | 17.7 | | 24.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

*Table 2-21* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.6 | | 1.9 | | 2.7 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-22* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.2 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.7 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-23* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-25* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **2.5 V LVCMOS Output Module Timing [2, 3]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 11.6 | | 13.4 | | 15.2 | | 17.9 | | 25.0 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[4] | Delta Low to High | | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[4] | Delta High to Low | | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[4] | Delta High to Low—low slew | | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

*Table 2-28* • **A54SX32A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-34* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **5 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.1 | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.1 | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 1.9 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.5 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 6.6 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.9 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.3 | | 3.9 | | 5.4 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-35* • **A54SX72A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-36* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| $t_{HP}$ | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.7 | | 4.3 | | 6.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.9 | | 3.3 | | 3.8 | | 4.5 | | 6.2 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.1 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| **Quadrant Array Clock Networks** | | | | | | | | | | | | |
| $t_{QCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{QCHKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{QCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{QCHKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| A1 | GND | GND | GND |
| A2 | TCK, I/O | TCK, I/O | TCK, I/O |
| A3 | I/O | I/O | I/O |
| A4 | I/O | I/O | I/O |
| A5 | I/O | I/O | I/O |
| A6 | I/O | I/O | I/O |
| A7 | I/O | I/O | I/O |
| A8 | I/O | I/O | I/O |
| A9 | CLKB | CLKB | CLKB |
| A10 | I/O | I/O | I/O |
| A11 | I/O | I/O | I/O |
| A12 | NC | I/O | I/O |
| A13 | I/O | I/O | I/O |
| A14 | I/O | I/O | I/O |
| A15 | GND | GND | GND |
| A16 | GND | GND | GND |
| B1 | I/O | I/O | I/O |
| B2 | GND | GND | GND |
| B3 | I/O | I/O | I/O |
| B4 | I/O | I/O | I/O |
| B5 | I/O | I/O | I/O |
| B6 | NC | I/O | I/O |
| B7 | I/O | I/O | I/O |
| B8 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| B9 | I/O | I/O | I/O |
| B10 | I/O | I/O | I/O |
| B11 | NC | I/O | I/O |
| B12 | I/O | I/O | I/O |
| B13 | I/O | I/O | I/O |
| B14 | I/O | I/O | I/O |
| B15 | GND | GND | GND |
| B16 | I/O | I/O | I/O |
| C1 | I/O | I/O | I/O |
| C2 | TDI, I/O | TDI, I/O | TDI, I/O |
| C3 | GND | GND | GND |
| C4 | I/O | I/O | I/O |
| C5 | NC | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| C6 | I/O | I/O | I/O |
| C7 | I/O | I/O | I/O |
| C8 | I/O | I/O | I/O |
| C9 | CLKA | CLKA | CLKA |
| C10 | I/O | I/O | I/O |
| C11 | I/O | I/O | I/O |
| C12 | I/O | I/O | I/O |
| C13 | I/O | I/O | I/O |
| C14 | I/O | I/O | I/O |
| C15 | I/O | I/O | I/O |
| C16 | I/O | I/O | I/O |
| D1 | I/O | I/O | I/O |
| D2 | I/O | I/O | I/O |
| D3 | I/O | I/O | I/O |
| D4 | I/O | I/O | I/O |
| D5 | I/O | I/O | I/O |
| D6 | I/O | I/O | I/O |
| D7 | I/O | I/O | I/O |
| D8 | PRA, I/O | PRA, I/O | PRA, I/O |
| D9 | I/O | I/O | QCLKD |
| D10 | I/O | I/O | I/O |
| D11 | NC | I/O | I/O |
| D12 | I/O | I/O | I/O |
| D13 | I/O | I/O | I/O |
| D14 | I/O | I/O | I/O |
| D15 | I/O | I/O | I/O |
| D16 | I/O | I/O | I/O |
| E1 | I/O | I/O | I/O |
| E2 | I/O | I/O | I/O |
| E3 | I/O | I/O | I/O |
| E4 | I/O | I/O | I/O |
| E5 | I/O | I/O | I/O |
| E6 | I/O | I/O | I/O |
| E7 | I/O | I/O | QCLKC |
| E8 | I/O | I/O | I/O |
| E9 | I/O | I/O | I/O |
| E10 | I/O | I/O | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| T3 | I/O | I/O |
| T4 | I/O | I/O |
| T5 | I/O | I/O |
| T10 | GND | GND |
| T11 | GND | GND |
| T12 | GND | GND |
| T13 | GND | GND |
| T14 | GND | GND |
| T15 | GND | GND |
| T16 | GND | GND |
| T17 | GND | GND |
| T22 | I/O | I/O |
| T23 | I/O | I/O |
| T24 | I/O | I/O |
| T25 | NC* | I/O |
| T26 | NC* | I/O |
| U1 | I/O | I/O |
| U2 | $V_{CCI}$ | $V_{CCI}$ |
| U3 | I/O | I/O |
| U4 | I/O | I/O |
| U5 | I/O | I/O |
| U10 | GND | GND |
| U11 | GND | GND |
| U12 | GND | GND |
| U13 | GND | GND |
| U14 | GND | GND |
| U15 | GND | GND |
| U16 | GND | GND |
| U17 | GND | GND |
| U22 | I/O | I/O |
| U23 | I/O | I/O |
| U24 | I/O | I/O |
| U25 | $V_{CCI}$ | $V_{CCI}$ |
| U26 | I/O | I/O |
| V1 | NC* | I/O |

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| V2 | NC* | I/O |
| V3 | I/O | I/O |
| V4 | I/O | I/O |
| V5 | I/O | I/O |
| V22 | $V_{CCA}$ | $V_{CCA}$ |
| V23 | I/O | I/O |
| V24 | I/O | I/O |
| V25 | NC* | I/O |
| V26 | NC* | I/O |
| W1 | I/O | I/O |
| W2 | I/O | I/O |
| W3 | I/O | I/O |
| W4 | I/O | I/O |
| W5 | I/O | I/O |
| W22 | I/O | I/O |
| W23 | $V_{CCA}$ | $V_{CCA}$ |
| W24 | I/O | I/O |
| W25 | NC* | I/O |
| W26 | NC* | I/O |
| Y1 | NC* | I/O |
| Y2 | NC* | I/O |
| Y3 | I/O | I/O |
| Y4 | I/O | I/O |
| Y5 | NC* | I/O |
| Y22 | I/O | I/O |
| Y23 | I/O | I/O |
| Y24 | $V_{CCI}$ | $V_{CCI}$ |
| Y25 | I/O | I/O |
| Y26 | I/O | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*