



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	12000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-2tqg144i">https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-2tqg144i</a>

## Temperature Grade Offering

Package	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

**Notes:**

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

## Speed Grade and Temperature Grade Matrix

	F	Std	-1	-2	-3
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

**Notes:**

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.

## Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable

interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

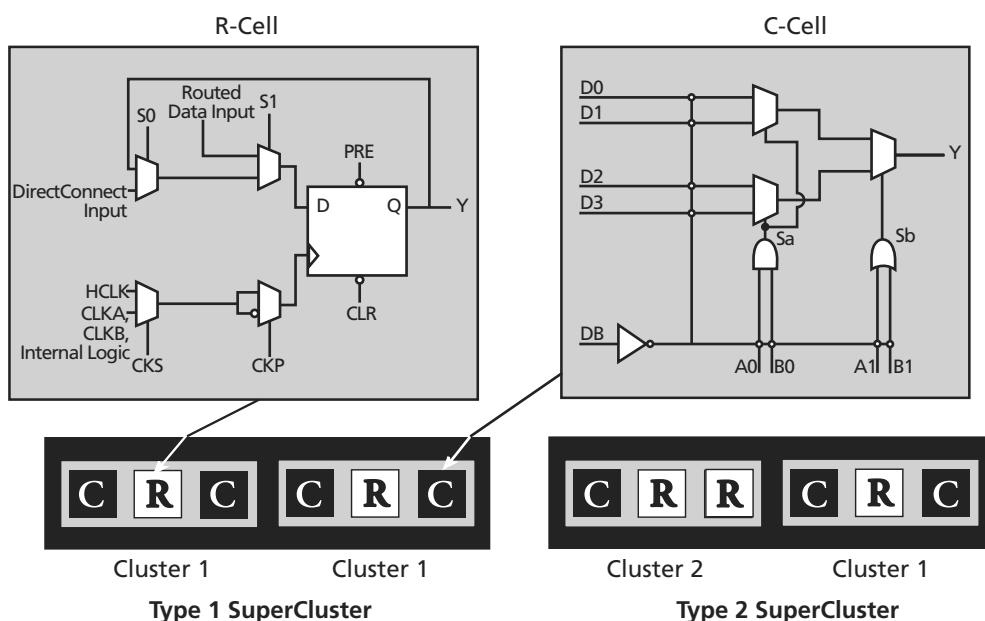


Figure 1-4 • Cluster Organization

## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

### Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

### Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V<sub>CC</sub> should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

### TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

## Pin Description

### **CLKA/B, I/O**      **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

### **QCLKA/B/C/D, I/O**      **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

### **GND**      **Ground**

Low supply voltage.

### **HCLK**      **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

### **I/O**      **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

### **NC**      **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

### **PRA/B, I/O**      **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### **TCK, I/O**      **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDI, I/O**      **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDO, I/O**      **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

### **TMS**      **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

### **TRST, I/O**      **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

### **V<sub>CC</sub>**      **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V<sub>CC</sub> power pins in the device should be connected.

### **V<sub>CCA</sub>**      **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V<sub>CCA</sub> power pins in the device should be connected.



## Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = −1 mA)	0.9 V <sub>CCI</sub>		0.9 V <sub>CCI</sub>		V
	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = −8 mA)	2.4		2.4		V
V <sub>OL</sub>	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 1 mA)	0.4		0.4		V
	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 12 mA)	0.4		0.4		V
V <sub>IL</sub>	Input Low Voltage		0.8		0.8		V
V <sub>IH</sub>	Input High Voltage		2.0	5.75	2.0	5.75	V
I <sub>IL</sub> /I <sub>IH</sub>	Input Leakage Current, V <sub>IN</sub> = V <sub>CCI</sub> or GND		−10	10	−10	10	μA
I <sub>OZ</sub>	Tristate Output Leakage Current		−10	10	−10	10	μA
t <sub>R</sub> , t <sub>F</sub>	Input Transition Time t <sub>R</sub> , t <sub>F</sub>		10		10		ns
C <sub>IO</sub>	I/O Capacitance		10		10		pF
I <sub>CC</sub>	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -100 μA)	2.1		2.1		V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -1 mA)	2.0		2.0		V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -2 mA)	1.7		1.7		V
V <sub>OL</sub>	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 100 μA)		0.2		0.2	V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 1 mA)		0.4		0.4	V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 2 mA)		0.7		0.7	V
V <sub>IL</sub>	Input Low Voltage, V <sub>OUT</sub> ≤ V <sub>VOL(max)</sub>		-0.3	0.7	-0.3	0.7	V
V <sub>IH</sub>	Input High Voltage, V <sub>OUT</sub> ≥ V <sub>VOH(min)</sub>		1.7	5.75	1.7	5.75	V
I <sub>IL</sub> /I <sub>IH</sub>	Input Leakage Current, V <sub>IN</sub> = V <sub>CC1</sub> or GND		-10	10	-10	10	μA
I <sub>OZ</sub>	Tristate Output Leakage Current, V <sub>OUT</sub> = V <sub>CC1</sub> or GND		-10	10	-10	10	μA
t <sub>R</sub> , t <sub>F</sub>	Input Transition Time t <sub>R</sub> , t <sub>F</sub>			10		10	ns
C <sub>IO</sub>	I/O Capacitance			10		10	pF
I <sub>CC</sub>	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

## PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V <sub>CCA</sub>	Supply Voltage for Array		2.25	2.75	V
V <sub>CCI</sub>	Supply Voltage for I/Os		4.75	5.25	V
V <sub>IH</sub>	Input High Voltage		2.0	5.75	V
V <sub>IL</sub>	Input Low Voltage		–0.5	0.8	V
I <sub>IH</sub>	Input High Leakage Current <sup>1</sup>	V <sub>IN</sub> = 2.7	–	70	μA
I <sub>IL</sub>	Input Low Leakage Current <sup>1</sup>	V <sub>IN</sub> = 0.5	–	–70	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = –2 mA	2.4	–	V
V <sub>OL</sub>	Output Low Voltage <sup>2</sup>	I <sub>OUT</sub> = 3 mA, 6 mA	–	0.55	V
C <sub>IN</sub>	Input Pin Capacitance <sup>3</sup>		–	10	pF
C <sub>CLK</sub>	CLK Pin Capacitance		5	12	pF

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).



To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

$$\theta_{CS} = 0.37^{\circ}\text{C/W}$$

= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{thermal resistance of the heat sink in } ^{\circ}\text{C/W}$$

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33^{\circ}\text{C/W} - 3.20^{\circ}\text{C/W} - 0.37^{\circ}\text{C/W}$$

$$\theta_{SA} = 9.76^{\circ}\text{C/W}$$

A heat sink with a thermal resistance of  $9.76^{\circ}\text{C/W}$  or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Table 2-22 • **A54SX16A Timing Characteristics**  
**(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.25\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t <sub>HCKSW</sub>	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t <sub>HP</sub>	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f <sub>HMAX</sub>	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

**Note:** \*All –3 speed grades have been discontinued.

Table 2-26 • **A54SX16A Timing Characteristics**  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing <sup>2</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High		2.0		2.3		2.6		3.1		4.3	ns
t <sub>DHL</sub>	Data-to-Pad High to Low		2.2		2.5		2.8		3.3		4.6	ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H		2.0		2.3		2.6		3.1		4.3	ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z		2.2		2.5		2.8		3.3		4.6	ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTTL Output Module Timing <sup>4</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High		2.8		3.2		3.6		4.3		6.0	ns
t <sub>DHL</sub>	Data-to-Pad High to Low		2.7		3.1		3.5		4.1		5.7	ns
t <sub>DHLS</sub>	Data-to-Pad High to Low—low slew		9.5		10.9		12.4		14.6		20.4	ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t <sub>ENZLS</sub>	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H		2.8		3.2		3.6		4.3		6.0	ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z		2.7		3.1		3.5		4.1		5.7	ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d <sub>THLS</sub> <sup>3</sup>	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

**Notes:**

1. All –3 speed grades have been discontinued.
2. Delays based on 10 pF loading and 25  $\Omega$  resistance.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[LH|HL|HLS]}$  is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

**Table 2-28 • A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions,  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	-3 Speed <sup>1</sup>		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>2</sup>												
t <sub>PD</sub>	Internal Array Module	0.8		0.9		1.1		1.2		1.7		ns
Predicted Routing Delays <sup>3</sup>												
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t <sub>RCO</sub>	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RECASYN</sub>	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t <sub>HASYN</sub>	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t <sub>MPW</sub>	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays												
t <sub>INYH</sub>	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.2		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 2.5 V LVCMOS	1.2		1.3		1.5		1.8		2.5		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V PCI	0.6		0.7		0.8		0.9		1.3		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V LVTTL	0.8		0.9		1.0		1.2		1.6		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V LVTTL	1.4		1.6		1.8		2.2		3.0		ns

**Notes:**

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t <sub>HP</sub>	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f <sub>HMAX</sub>	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

**Note:** \*All –3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{QCKH}$	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
$t_{QCHKL}$	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
$t_{QPWH}$	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
$t_{QPWL}$	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
$t_{QCKSW}$	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
$t_{QCKSW}$	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
$t_{QCKSW}$	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

**Note:** \*All –3 speed grades have been discontinued.

Table 2-41 • **A54SX72A Timing Characteristics**  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed <sup>1</sup>		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing <sup>2</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	2.7		3.1		3.5		4.1		5.7		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	3.4		3.9		4.4		5.1		7.2		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.7		3.1		3.5		4.1		5.7		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	3.4		3.9		4.4		5.1		7.2		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing <sup>4</sup>												
t <sub>DLH</sub>	Data-to-Pad Low to High	2.4		2.8		3.1		3.7		5.1		ns
t <sub>DHL</sub>	Data-to-Pad High to Low	3.1		3.5		4.0		4.7		6.6		ns
t <sub>DHLS</sub>	Data-to-Pad High to Low—low slew	7.4		8.5		9.7		11.4		15.9		ns
t <sub>ENZL</sub>	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t <sub>ENZLS</sub>	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t <sub>ENZH</sub>	Enable-to-Pad, Z to H	2.4		2.8		3.1		3.7		5.1		ns
t <sub>ENLZ</sub>	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t <sub>ENHZ</sub>	Enable-to-Pad, H to Z	3.1		3.5		4.0		4.7		6.6		ns
d <sub>TLH</sub> <sup>3</sup>	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d <sub>THL</sub> <sup>3</sup>	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d <sub>THLS</sub> <sup>3</sup>	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

**Notes:**

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[HL|HL|HLS]}$  is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V <sub>CCA</sub>
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
41	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O



208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V <sub>CCI</sub>
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

<b>100-TQFP</b>			
<b>Pin Number</b>	<b>A54SX08A Function</b>	<b>A54SX16A Function</b>	<b>A54SX32A Function</b>
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>

<b>100-TQFP</b>			
<b>Pin Number</b>	<b>A54SX08A Function</b>	<b>A54SX16A Function</b>	<b>A54SX32A Function</b>
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
58	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

329-Pin PBGA	
Pin Number	A54SX32A Function
D11	V <sub>CCA</sub>
D12	NC
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V <sub>CCI</sub>
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V <sub>CCA</sub>
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	NC
L10	GND
L11	GND
L12	GND
L13	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
L14	GND
L20	NC
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V <sub>CCA</sub>
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V <sub>CCA</sub>
M21	I/O
M22	I/O
M23	V <sub>CCI</sub>
N1	I/O
N2	TRST, I/O
N3	I/O
N4	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND

329-Pin PBGA	
Pin Number	A54SX32A Function
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V <sub>CCA</sub>
U4	I/O
U20	I/O
U21	V <sub>CCA</sub>
U22	I/O
U23	I/O
V1	V <sub>CCI</sub>
V2	I/O
V3	I/O
V4	I/O
V20	I/O
V21	I/O

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

## International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.

Actel and the Actel logo are registered trademarks of Actel Corporation.  
All other trademarks are the property of their owners.



[www.actel.com](http://www.actel.com)

**Actel Corporation**

2061 Stierlin Court  
Mountain View, CA  
94043-4655 USA

**Phone** 650.318.4200

**Fax** 650.318.4600

**Actel Europe Ltd.**

River Court, Meadows Business Park  
Station Approach, Blackwater  
Camberley, Surrey GU17 9AB  
United Kingdom

**Phone** +44 (0) 1276 609 300

**Fax** +44 (0) 1276 607 540

**Actel Japan**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Phone** +81.03.3445.7671

**Fax** +81.03.3445.7668

[www.jp.actel.com](http://www.jp.actel.com)

**Actel Hong Kong**

Suite 2114, Two Pacific Place  
88 Queensway, Admiralty  
Hong Kong

**Phone** +852 2185 6460

**Fax** +852 2185 6488

[www.actel.com.cn](http://www.actel.com.cn)