# Microchip Technology - A54SX08A-TQ144 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 768 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 113 |
| Number of Gates | 12000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-tq144 |

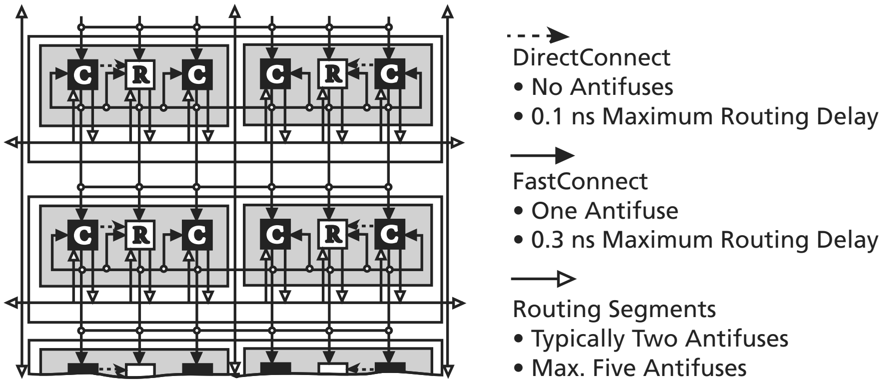

*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

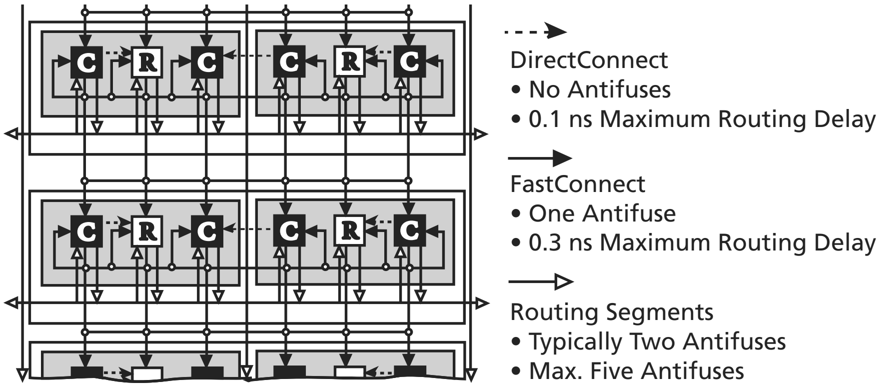

*Figure 1-6* • **DirectConnect and FastConnect for Type 2 SuperClusters**

## Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Device*s and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

*Table 1-1* • **SX-A Clock Resources**

| | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---|---|---|---|---|
| Routed Clocks (CLKA, CLKB) | 2 | 2 | 2 | 2 |
| Hardwired Clocks (HCLK) | 1 | 1 | 1 | 1 |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0 | 0 | 0 | 4 |

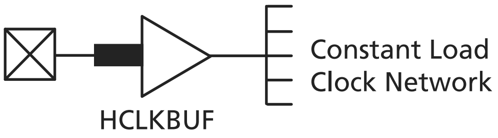

*Figure 1-7* • **SX-A HCLK Clock Buffer**

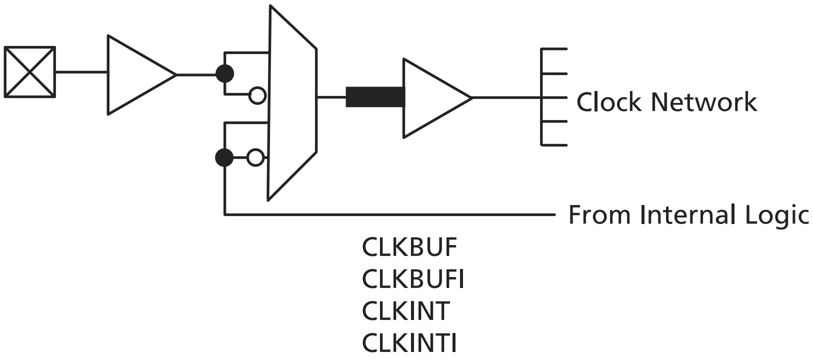

*Figure 1-8* • **SX-A Routed Clock Buffer**

# Other Architectural Features

## Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 $\mu$ / 0.25 $\mu$ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 $\Omega$ with capacitance of 1.0 fF for low signal impedance.

## Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

## User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).

*Figure 1-11* • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

## I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than $V_{CCI}$ and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and $V_{CCI}$ is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 k$\Omega$ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before $V_{CCA}$ reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

## Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

*Table 1-9* • **Device Configuration Options for Probe Capability (TRST Pin Reserved)**

| JTAG Mode | TRST[1] | Security Fuse Programmed | PRA, PRB[2] | TDI, TCK, TDO[2] |
|---|---|---|---|---|
| Dedicated | Low | No | User I/O[3] | JTAG Disabled |
| | High | No | Probe Circuit Outputs | JTAG I/O |
| Flexible | Low | No | User I/O[3] | User I/O[3] |
| | High | No | Probe Circuit Outputs | JTAG I/O |
| | | Yes | Probe Circuit Secured | Probe Circuit Secured |

***Notes:***

1. *If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

## SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

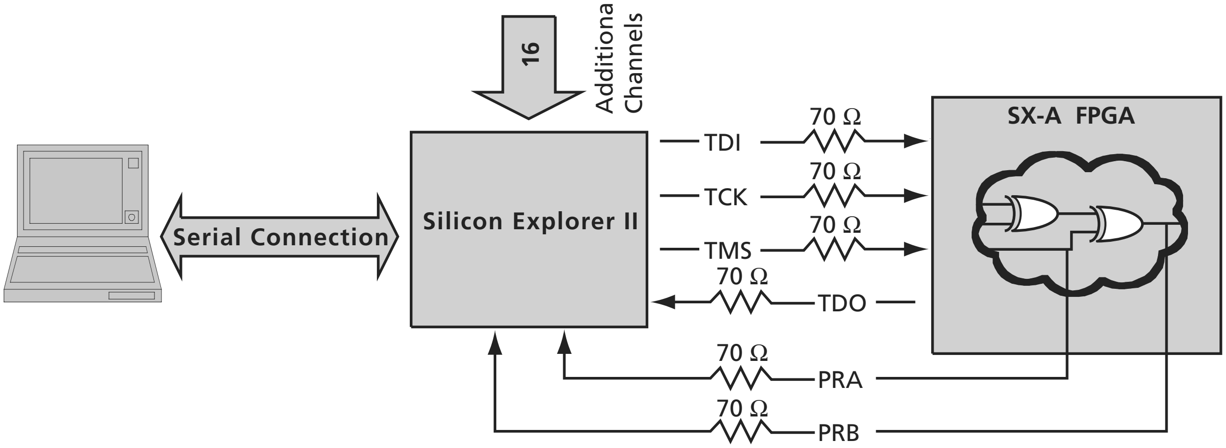

*Figure 1-13* • **Probe Setup**

## Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel’s integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

# Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User’s Guide*.

# Related Documents

## Application Notes

*Global Clock Networks in Actel's Antifuse Devices*
http://www.actel.com/documents/GlobalClk_AN.pdf
*Using A54SX72A and RT54SX72S Quadrant Clocks*
http://www.actel.com/documents/QCLK_AN.pdf
*Implementation of Security in Actel Antifuse FPGAs*
http://www.actel.com/documents/Antifuse_Security_AN.pdf
*Actel eX, SX-A, and RTSX-S I/Os*
http://www.actel.com/documents/AntifuseIO_AN.pdf
*Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*
http://www.actel.com/documents/HotSwapColdSparing_AN.pdf
*Programming Antifuse Devices*
http://www.actel.com/documents/AntifuseProgram_AN.pdf

## Datasheets

*HiRel SX-A Family FPGAs*
http://www.actel.com/documents/HRSXA_DS.pdf
*SX-A Automotive Family FPGAs*
http://www.actel.com/documents/SXA_Auto_DS.pdf

## User's Guides

*Silicon Sculptor User's Guide*
http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

# Electrical Specifications

*Table 2-5* • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

| | | | **Commercial** | | **Industrial** | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 0.9 $V_{CCI}$ | | 0.9 $V_{CCI}$ | | V |
| | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –8 mA) | 2.4 | | 2.4 | | V |
| $V_{OL}$ | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 12 mA) | | 0.4 | | 0.4 | V |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | 5.75 | 2.0 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

*Table 2-6* • **2.5 V LVCMOS2 Electrical Specifications**

| | | | **Commercial** | | **Industrial** | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –100 µA) | 2.1 | | 2.1 | | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 2.0 | | 2.0 | | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ =–-2 mA) | 1.7 | | 1.7 | | V |
| $V_{OL}$ | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 100 µA) | | 0.2 | | 0.2 | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 2 mA) | | 0.7 | | 0.7 | V |
| $V_{IL}$ | Input Low Voltage, $V_{OUT} \leq V_{VOL(max)}$ | | -0.3 | 0.7 | -0.3 | 0.7 | V |
| $V_{IH}$ | Input High Voltage, $V_{OUT} \geq V_{VOH(min)}$ | | 1.7 | 5.75 | 1.7 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

## Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules
Inputs Switching (n) = Number inputs/4
Outputs Switching (p) = Number of outputs/4
CLKA Loads (q1) = 20% of R-cells
CLKB Loads (q2) = 20% of R-cells
Load Capacitance (CL) = 35 pF
Average Logic Module Switching Rate (fm) = f/10
Average Input Switching Rate (fn) =f/5
Average Output Switching Rate (fp) = f/10
Average CLKA Rate (fq1) = f/2
Average CLKB Rate (fq2) = f/2
Average HCLK Rate (fs1) = f
HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 2-14*

where:

$\theta_{CS}$ = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
$\theta_{SA}$ = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

*Table 2-14* • **A54SX08A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.5 | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| **Input Module Predicted Routing Delays**[2] | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *For dual-module macros, use* $t_{PD} + t_{RD1} + t_{PDn}$ *,* $t_{RCO} + t_{RD1} + t_{PDn}$ *, or* $t_{PD1} + t_{RD1} + t_{SUD}$ *, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-29* • **A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | | 5.0 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | NC | NC | NC |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | NC | NC | NC |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

| 144-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| G1 | I/O | I/O | I/O |
| G2 | GND | GND | GND |
| G3 | I/O | I/O | I/O |
| G4 | I/O | I/O | I/O |
| G5 | GND | GND | GND |
| G6 | GND | GND | GND |
| G7 | GND | GND | GND |
| G8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| G9 | I/O | I/O | I/O |
| G10 | I/O | I/O | I/O |
| G11 | I/O | I/O | I/O |
| G12 | I/O | I/O | I/O |
| H1 | TRST, I/O | TRST, I/O | TRST, I/O |
| H2 | I/O | I/O | I/O |
| H3 | I/O | I/O | I/O |
| H4 | I/O | I/O | I/O |
| H5 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H6 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H9 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H10 | I/O | I/O | I/O |
| H11 | I/O | I/O | I/O |
| H12 | NC | NC | NC |
| J1 | I/O | I/O | I/O |
| J2 | I/O | I/O | I/O |
| J3 | I/O | I/O | I/O |
| J4 | I/O | I/O | I/O |
| J5 | I/O | I/O | I/O |
| J6 | PRB, I/O | PRB, I/O | PRB, I/O |
| J7 | I/O | I/O | I/O |
| J8 | I/O | I/O | I/O |
| J9 | I/O | I/O | I/O |
| J10 | I/O | I/O | I/O |
| J11 | I/O | I/O | I/O |
| J12 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |

| 144-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| K1 | I/O | I/O | I/O |
| K2 | I/O | I/O | I/O |
| K3 | I/O | I/O | I/O |
| K4 | I/O | I/O | I/O |
| K5 | I/O | I/O | I/O |
| K6 | I/O | I/O | I/O |
| K7 | GND | GND | GND |
| K8 | I/O | I/O | I/O |
| K9 | I/O | I/O | I/O |
| K10 | GND | GND | GND |
| K11 | I/O | I/O | I/O |
| K12 | I/O | I/O | I/O |
| L1 | GND | GND | GND |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | HCLK | HCLK | HCLK |
| L8 | I/O | I/O | I/O |
| L9 | I/O | I/O | I/O |
| L10 | I/O | I/O | I/O |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| M8 | I/O | I/O | I/O |
| M9 | I/O | I/O | I/O |
| M10 | I/O | I/O | I/O |
| M11 | TDO, I/O | TDO, I/O | TDO, I/O |
| M12 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| A1 | GND | GND | GND |
| A2 | TCK, I/O | TCK, I/O | TCK, I/O |
| A3 | I/O | I/O | I/O |
| A4 | I/O | I/O | I/O |
| A5 | I/O | I/O | I/O |
| A6 | I/O | I/O | I/O |
| A7 | I/O | I/O | I/O |
| A8 | I/O | I/O | I/O |
| A9 | CLKB | CLKB | CLKB |
| A10 | I/O | I/O | I/O |
| A11 | I/O | I/O | I/O |
| A12 | NC | I/O | I/O |
| A13 | I/O | I/O | I/O |
| A14 | I/O | I/O | I/O |
| A15 | GND | GND | GND |
| A16 | GND | GND | GND |
| B1 | I/O | I/O | I/O |
| B2 | GND | GND | GND |
| B3 | I/O | I/O | I/O |
| B4 | I/O | I/O | I/O |
| B5 | I/O | I/O | I/O |
| B6 | NC | I/O | I/O |
| B7 | I/O | I/O | I/O |
| B8 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| B9 | I/O | I/O | I/O |
| B10 | I/O | I/O | I/O |
| B11 | NC | I/O | I/O |
| B12 | I/O | I/O | I/O |
| B13 | I/O | I/O | I/O |
| B14 | I/O | I/O | I/O |
| B15 | GND | GND | GND |
| B16 | I/O | I/O | I/O |
| C1 | I/O | I/O | I/O |
| C2 | TDI, I/O | TDI, I/O | TDI, I/O |
| C3 | GND | GND | GND |
| C4 | I/O | I/O | I/O |
| C5 | NC | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| C6 | I/O | I/O | I/O |
| C7 | I/O | I/O | I/O |
| C8 | I/O | I/O | I/O |
| C9 | CLKA | CLKA | CLKA |
| C10 | I/O | I/O | I/O |
| C11 | I/O | I/O | I/O |
| C12 | I/O | I/O | I/O |
| C13 | I/O | I/O | I/O |
| C14 | I/O | I/O | I/O |
| C15 | I/O | I/O | I/O |
| C16 | I/O | I/O | I/O |
| D1 | I/O | I/O | I/O |
| D2 | I/O | I/O | I/O |
| D3 | I/O | I/O | I/O |
| D4 | I/O | I/O | I/O |
| D5 | I/O | I/O | I/O |
| D6 | I/O | I/O | I/O |
| D7 | I/O | I/O | I/O |
| D8 | PRA, I/O | PRA, I/O | PRA, I/O |
| D9 | I/O | I/O | QCLKD |
| D10 | I/O | I/O | I/O |
| D11 | NC | I/O | I/O |
| D12 | I/O | I/O | I/O |
| D13 | I/O | I/O | I/O |
| D14 | I/O | I/O | I/O |
| D15 | I/O | I/O | I/O |
| D16 | I/O | I/O | I/O |
| E1 | I/O | I/O | I/O |
| E2 | I/O | I/O | I/O |
| E3 | I/O | I/O | I/O |
| E4 | I/O | I/O | I/O |
| E5 | I/O | I/O | I/O |
| E6 | I/O | I/O | I/O |
| E7 | I/O | I/O | QCLKC |
| E8 | I/O | I/O | I/O |
| E9 | I/O | I/O | I/O |
| E10 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| K5 | I/O | I/O | I/O |
| K6 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K7 | GND | GND | GND |
| K8 | GND | GND | GND |
| K9 | GND | GND | GND |
| K10 | GND | GND | GND |
| K11 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K12 | I/O | I/O | I/O |
| K13 | I/O | I/O | I/O |
| K14 | I/O | I/O | I/O |
| K15 | NC | I/O | I/O |
| K16 | I/O | I/O | I/O |
| L1 | I/O | I/O | I/O |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L9 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| L13 | I/O | I/O | I/O |
| L14 | I/O | I/O | I/O |
| L15 | I/O | I/O | I/O |
| L16 | NC | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | I/O | I/O | QCLKA |
| M8 | PRB, I/O | PRB, I/O | PRB, I/O |
| M9 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| Pin Number | A54SX16A Function | A54SX32A Function | A54SX72A Function |
| M10 | I/O | I/O | I/O |
| M11 | I/O | I/O | I/O |
| M12 | NC | I/O | I/O |
| M13 | I/O | I/O | I/O |
| M14 | NC | I/O | I/O |
| M15 | I/O | I/O | I/O |
| M16 | I/O | I/O | I/O |
| N1 | I/O | I/O | I/O |
| N2 | I/O | I/O | I/O |
| N3 | I/O | I/O | I/O |
| N4 | I/O | I/O | I/O |
| N5 | I/O | I/O | I/O |
| N6 | I/O | I/O | I/O |
| N7 | I/O | I/O | I/O |
| N8 | I/O | I/O | I/O |
| N9 | I/O | I/O | I/O |
| N10 | I/O | I/O | I/O |
| N11 | I/O | I/O | I/O |
| N12 | I/O | I/O | I/O |
| N13 | I/O | I/O | I/O |
| N14 | I/O | I/O | I/O |
| N15 | I/O | I/O | I/O |
| N16 | I/O | I/O | I/O |
| P1 | I/O | I/O | I/O |
| P2 | GND | GND | GND |
| P3 | I/O | I/O | I/O |
| P4 | I/O | I/O | I/O |
| P5 | NC | I/O | I/O |
| P6 | I/O | I/O | I/O |
| P7 | I/O | I/O | I/O |
| P8 | I/O | I/O | I/O |
| P9 | I/O | I/O | I/O |
| P10 | NC | I/O | I/O |
| P11 | I/O | I/O | I/O |
| P12 | I/O | I/O | I/O |
| P13 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| P14 | I/O | I/O | I/O |

# 484-Pin FBGA

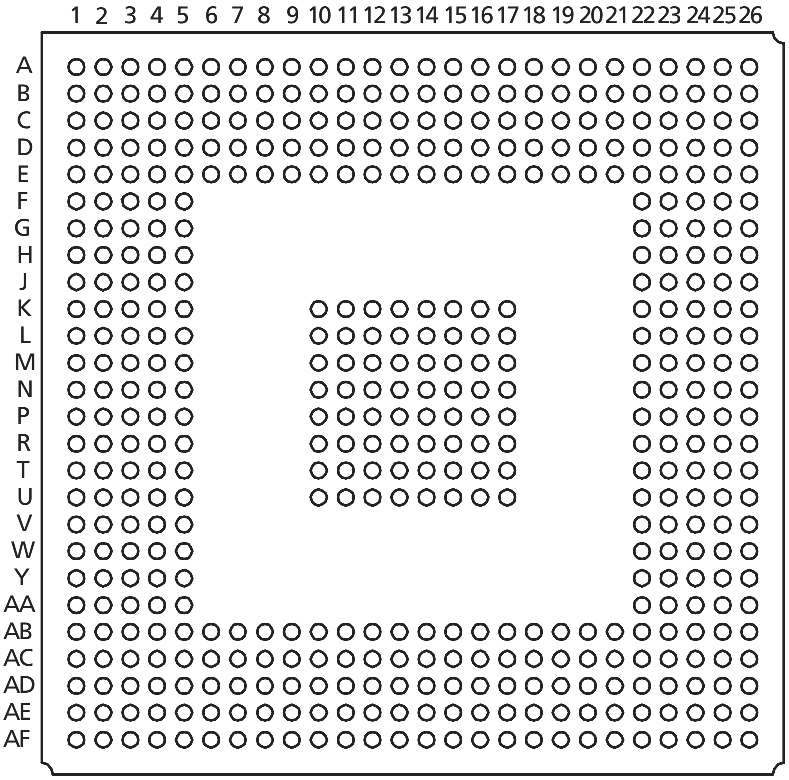

*Figure 3-8* • **484-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| C19 | I/O | I/O |
| C20 | $V_{CCI}$ | $V_{CCI}$ |
| C21 | I/O | I/O |
| C22 | I/O | I/O |
| C23 | I/O | I/O |
| C24 | I/O | I/O |
| C25 | NC* | I/O |
| C26 | NC* | I/O |
| D1 | NC* | I/O |
| D2 | TMS | TMS |
| D3 | I/O | I/O |
| D4 | $V_{CCI}$ | $V_{CCI}$ |
| D5 | NC* | I/O |
| D6 | TCK, I/O | TCK, I/O |
| D7 | I/O | I/O |
| D8 | I/O | I/O |
| D9 | I/O | I/O |
| D10 | I/O | I/O |
| D11 | I/O | I/O |
| D12 | I/O | QCLKC |
| D13 | I/O | I/O |
| D14 | I/O | I/O |
| D15 | I/O | I/O |
| D16 | I/O | I/O |
| D17 | I/O | I/O |
| D18 | I/O | I/O |
| D19 | I/O | I/O |
| D20 | I/O | I/O |
| D21 | $V_{CCI}$ | $V_{CCI}$ |
| D22 | GND | GND |
| D23 | I/O | I/O |
| D24 | I/O | I/O |
| D25 | NC* | I/O |
| D26 | NC* | I/O |
| E1 | NC* | I/O |
| E2 | NC* | I/O |
| E3 | I/O | I/O |
| E4 | I/O | I/O |
| E5 | GND | GND |
| E6 | TDI, IO | TDI, IO |
| E7 | I/O | I/O |
| E8 | I/O | I/O |
| E9 | I/O | I/O |
| E10 | I/O | I/O |
| E11 | I/O | I/O |
| E12 | I/O | I/O |
| E13 | $V_{CCA}$ | $V_{CCA}$ |
| E14 | CLKB | CLKB |
| E15 | I/O | I/O |
| E16 | I/O | I/O |
| E17 | I/O | I/O |
| E18 | I/O | I/O |
| E19 | I/O | I/O |
| E20 | I/O | I/O |
| E21 | I/O | I/O |
| E22 | I/O | I/O |
| E23 | I/O | I/O |
| E24 | I/O | I/O |
| E25 | $V_{CCI}$ | $V_{CCI}$ |
| E26 | GND | GND |
| F1 | $V_{CCI}$ | $V_{CCI}$ |
| F2 | NC* | I/O |
| F3 | NC* | I/O |
| F4 | I/O | I/O |
| F5 | I/O | I/O |
| F22 | I/O | I/O |
| F23 | I/O | I/O |
| F24 | I/O | I/O |
| F25 | I/O | I/O |
| F26 | NC* | I/O |
| G1 | NC* | I/O |
| G2 | NC* | I/O |
| G3 | NC* | I/O |
| G4 | I/O | I/O |
| G5 | I/O | I/O |
| G22 | I/O | I/O |
| G23 | $V_{CCA}$ | $V_{CCA}$ |
| G24 | I/O | I/O |
| G25 | NC* | I/O |
| G26 | NC* | I/O |
| H1 | NC* | I/O |
| H2 | NC* | I/O |
| H3 | I/O | I/O |
| H4 | I/O | I/O |
| H5 | I/O | I/O |
| H22 | I/O | I/O |
| H23 | I/O | I/O |
| H24 | I/O | I/O |
| H25 | NC* | I/O |
| H26 | NC* | I/O |
| J1 | NC* | I/O |
| J2 | NC* | I/O |
| J3 | I/O | I/O |
| J4 | I/O | I/O |
| J5 | I/O | I/O |
| J22 | I/O | I/O |
| J23 | I/O | I/O |
| J24 | I/O | I/O |
| J25 | $V_{CCI}$ | $V_{CCI}$ |
| J26 | NC* | I/O |
| K1 | I/O | I/O |
| K2 | $V_{CCI}$ | $V_{CCI}$ |
| K3 | I/O | I/O |
| K4 | I/O | I/O |
| K5 | $V_{CCA}$ | $V_{CCA}$ |

***Note:*** **These pins must be left floating on the A54SX32A device.*

| 484-Pin FBGA | | |
|---|---|---|
| **Pin Number** | **A54SX32A Function** | **A54SX72A Function** |
| K10 | GND | GND |
| K11 | GND | GND |
| K12 | GND | GND |
| K13 | GND | GND |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | GND | GND |
| K17 | GND | GND |
| K22 | I/O | I/O |
| K23 | I/O | I/O |
| K24 | NC* | NC |
| K25 | NC* | I/O |
| K26 | NC* | I/O |
| L1 | NC* | I/O |
| L2 | NC* | I/O |
| L3 | I/O | I/O |
| L4 | I/O | I/O |
| L5 | I/O | I/O |
| L10 | GND | GND |
| L11 | GND | GND |
| L12 | GND | GND |
| L13 | GND | GND |
| L14 | GND | GND |
| L15 | GND | GND |
| L16 | GND | GND |
| L17 | GND | GND |
| L22 | I/O | I/O |
| L23 | I/O | I/O |
| L24 | I/O | I/O |
| L25 | I/O | I/O |
| L26 | I/O | I/O |
| M1 | NC* | NC |
| M2 | I/O | I/O |
| M3 | I/O | I/O |
| M4 | I/O | I/O |
| M5 | I/O | I/O |
| M10 | GND | GND |
| M11 | GND | GND |
| M12 | GND | GND |
| M13 | GND | GND |
| M14 | GND | GND |
| M15 | GND | GND |
| M16 | GND | GND |
| M17 | GND | GND |
| M22 | I/O | I/O |
| M23 | I/O | I/O |
| M24 | I/O | I/O |
| M25 | NC* | I/O |
| M26 | NC* | I/O |
| N1 | I/O | I/O |
| N2 | $V_{CCI}$ | $V_{CCI}$ |
| N3 | I/O | I/O |
| N4 | I/O | I/O |
| N5 | I/O | I/O |
| N10 | GND | GND |
| N11 | GND | GND |
| N12 | GND | GND |
| N13 | GND | GND |
| N14 | GND | GND |
| N15 | GND | GND |
| N16 | GND | GND |
| N17 | GND | GND |
| N22 | $V_{CCA}$ | $V_{CCA}$ |
| N23 | I/O | I/O |
| N24 | I/O | I/O |
| N25 | I/O | I/O |
| N26 | NC* | NC |
| P1 | NC* | I/O |
| P2 | NC* | I/O |
| P3 | I/O | I/O |
| P4 | I/O | I/O |
| P5 | $V_{CCA}$ | $V_{CCA}$ |
| P10 | GND | GND |
| P11 | GND | GND |
| P12 | GND | GND |
| P13 | GND | GND |
| P14 | GND | GND |
| P15 | GND | GND |
| P16 | GND | GND |
| P17 | GND | GND |
| P22 | I/O | I/O |
| P23 | I/O | I/O |
| P24 | $V_{CCI}$ | $V_{CCI}$ |
| P25 | I/O | I/O |
| P26 | I/O | I/O |
| R1 | NC* | I/O |
| R2 | NC* | I/O |
| R3 | I/O | I/O |
| R4 | I/O | I/O |
| R5 | TRST, I/O | TRST, I/O |
| R10 | GND | GND |
| R11 | GND | GND |
| R12 | GND | GND |
| R13 | GND | GND |
| R14 | GND | GND |
| R15 | GND | GND |
| R16 | GND | GND |
| R17 | GND | GND |
| R22 | I/O | I/O |
| R23 | I/O | I/O |
| R24 | I/O | I/O |
| R25 | NC* | I/O |
| R26 | NC* | I/O |
| T1 | NC* | I/O |
| T2 | NC* | I/O |

***Note:*** **These pins must be left floating on the A54SX32A device.*

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v5.2<br>(June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1<br>February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| | Table 2-11 was updated. | 2-9 |