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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-tqg100">https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-tqg100</a>

## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

### Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

### Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V<sub>CC</sub> should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

### TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

## Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

JTAG Mode	TRST <sup>1</sup>	Security Fuse Programmed	PRA, PRB <sup>2</sup>	TDI, TCK, TDO <sup>2</sup>
Dedicated	Low	No	User I/O <sup>3</sup>	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O <sup>3</sup>	User I/O <sup>3</sup>
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

### Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

## Pin Description

### **CLKA/B, I/O**      **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

### **QCLKA/B/C/D, I/O**      **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

### **GND**      **Ground**

Low supply voltage.

### **HCLK**      **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

### **I/O**      **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

### **NC**      **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

### **PRA/B, I/O**      **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

### **TCK, I/O**      **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDI, I/O**      **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

### **TDO, I/O**      **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

### **TMS**      **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

### **TRST, I/O**      **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

### **V<sub>CC</sub>**      **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V<sub>CC</sub> power pins in the device should be connected.

### **V<sub>CCA</sub>**      **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V<sub>CCA</sub> power pins in the device should be connected.

**Table 2-8 • AC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ <sup>1</sup>	-44	–	mA
		$1.4 \leq V_{OUT} < 2.4$ <sup>1, 2</sup>	$(-44 + (V_{OUT} - 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ <sup>1, 3</sup>	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ <sup>3</sup>	–	-142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ <sup>1</sup>	95	–	mA
		$2.2 > V_{OUT} > 0.55$ <sup>1</sup>	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ <sup>1, 3</sup>	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ <sup>3</sup>	–	206	mA
$I_{CL}$	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load <sup>4</sup>	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load <sup>4</sup>	1	5	V/ns

**Notes:**

1. Refer to the *V<sub>I</sub>* curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

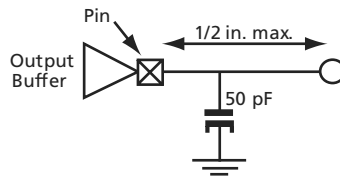


Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

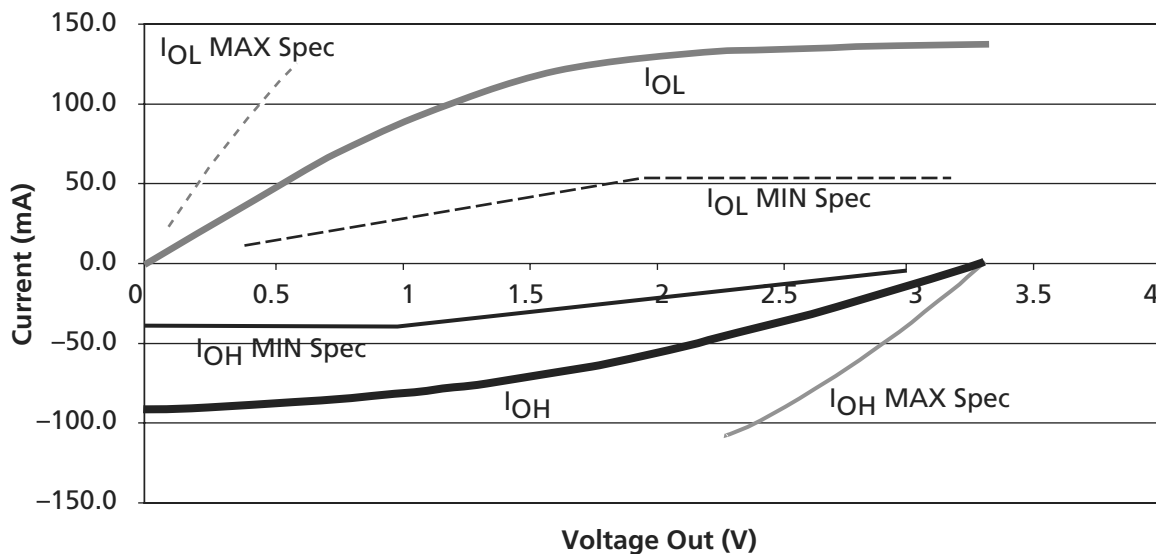


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for  $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for  $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

## Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 2-5

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{\text{DC}} = I_{\text{standby}} * V_{\text{CCA}}$$

EQ 2-6

Note: For other combinations of temperature and voltage settings, refer to the *eX, SX-A and RT54SX-S Power Calculator*.

## AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{\text{AC}} = P_{\text{C-cells}} + P_{\text{R-cells}} + P_{\text{CLKA}} + P_{\text{CLKB}} + P_{\text{HCLK}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 2-7

or:

$$P_{\text{AC}} = V_{\text{CCA}}^2 * [(m * C_{\text{EQCM}} * f_m)_{\text{C-cells}} + (m * C_{\text{EQSM}} * f_m)_{\text{R-cells}} + (n * C_{\text{EQI}} * f_n)_{\text{Input Buffer}} + (p * (C_{\text{EQO}} + C_L) * f_p)_{\text{Output Buffer}} + (0.5 * (q_1 * C_{\text{EQCR}} * f_{q1}) + (r_1 * f_{q1}))_{\text{CLKA}} + (0.5 * (q_2 * C_{\text{EQCR}} * f_{q2}) + (r_2 * f_{q2}))_{\text{CLKB}} + (0.5 * (s_1 * C_{\text{EQHV}} * f_{s1}) + (C_{\text{EQHF}} * f_{s1}))_{\text{HCLK}}]$$

EQ 2-8

## Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}\text{C/W} \text{ is taken from Table 2-12 on page 2-11}$$

$$T_A = 125^{\circ}\text{C} \text{ is the maximum limit of ambient (from the datasheet)}$$

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

## Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

## Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data  $T_J$  and  $T_A$  are given as follows:

$$T_J = 110^{\circ}\text{C}$$

$$T_A = 70^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 18.0^{\circ}\text{C/W}$$

$$\theta_{JC} = 3.2^{\circ}\text{C/W}$$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

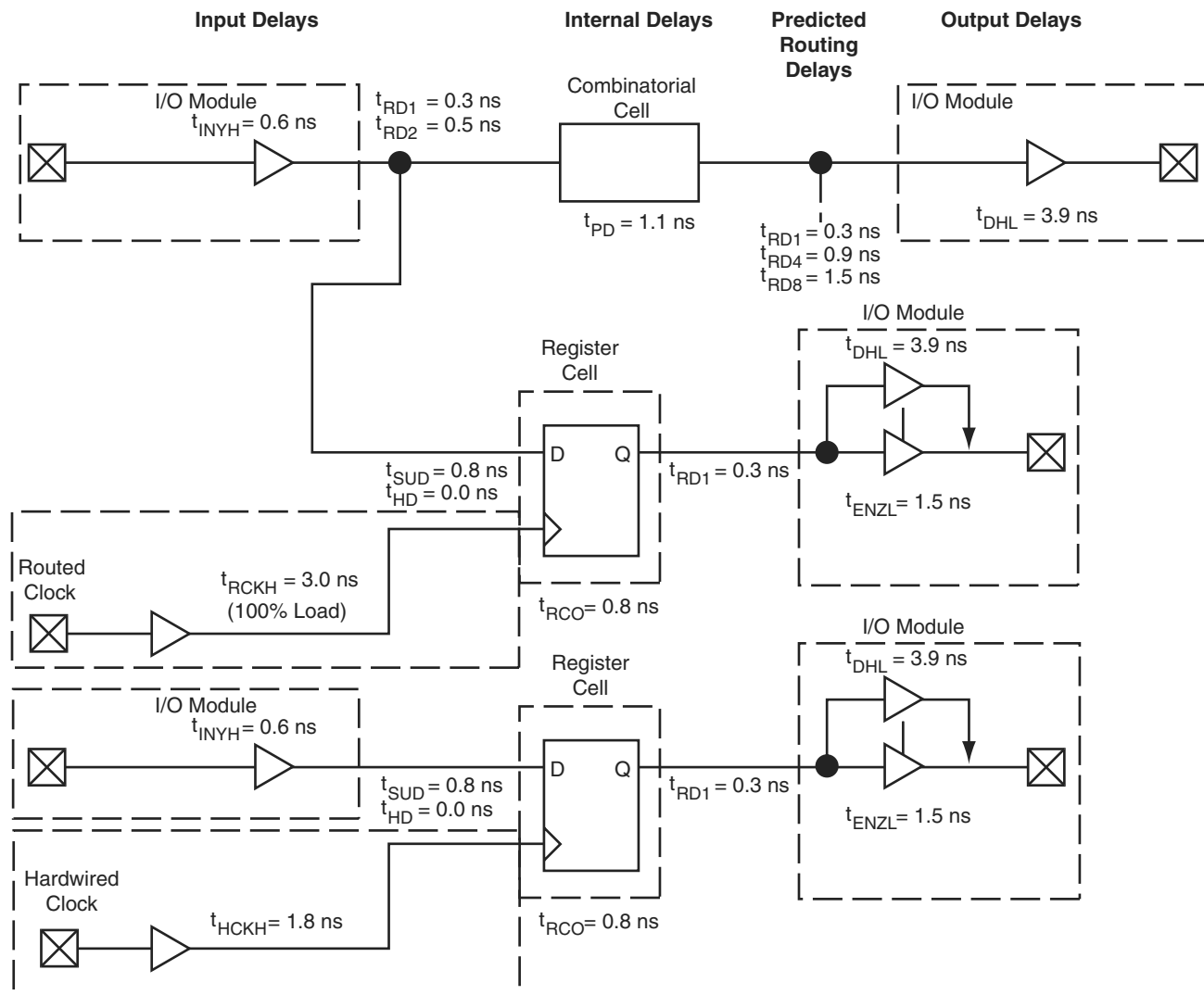
The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{3.00 \text{ W}} = 13.33^{\circ}\text{C/W}$$

EQ 2-13



## SX-A Timing Model



**Note:** \*Values shown for A54SX72A, -2, worst-case commercial conditions at 5 V PCI with standard place-and-route.

Figure 2-3 • SX-A Timing Model

## Sample Path Calculations

### Hardwired Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH} \\ &= 0.6 + 0.3 + 0.8 - 1.8 = -0.1 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 \text{ ns} \end{aligned}$$

### Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH} \\ &= 0.6 + 0.3 + 0.8 - 3.0 = -1.3 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 \text{ ns} \end{aligned}$$

**Table 2-28 • A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions,  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	-3 Speed <sup>1</sup>		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>2</sup>												
t <sub>PD</sub>	Internal Array Module	0.8		0.9		1.1		1.2		1.7		ns
Predicted Routing Delays <sup>3</sup>												
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t <sub>RCO</sub>	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RECASYN</sub>	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t <sub>HASYN</sub>	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t <sub>MPW</sub>	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays												
t <sub>INYH</sub>	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.2		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 2.5 V LVCMOS	1.2		1.3		1.5		1.8		2.5		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V PCI	0.6		0.7		0.8		0.9		1.3		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V LVTTTL	0.8		0.9		1.0		1.2		1.6		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V LVTTTL	1.4		1.6		1.8		2.2		3.0		ns

**Notes:**

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t <sub>HP</sub>	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f <sub>HMAX</sub>	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

**Note:** \*All –3 speed grades have been discontinued.

Table 2-38 • **A54SX72A Timing Characteristics**  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t <sub>HCKSW</sub>	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t <sub>HP</sub>	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f <sub>HMAX</sub>	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t <sub>QCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t <sub>QCHKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t <sub>QCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t <sub>QCHKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

**Note:** \*All –3 speed grades have been discontinued.

## 100-Pin TQFP

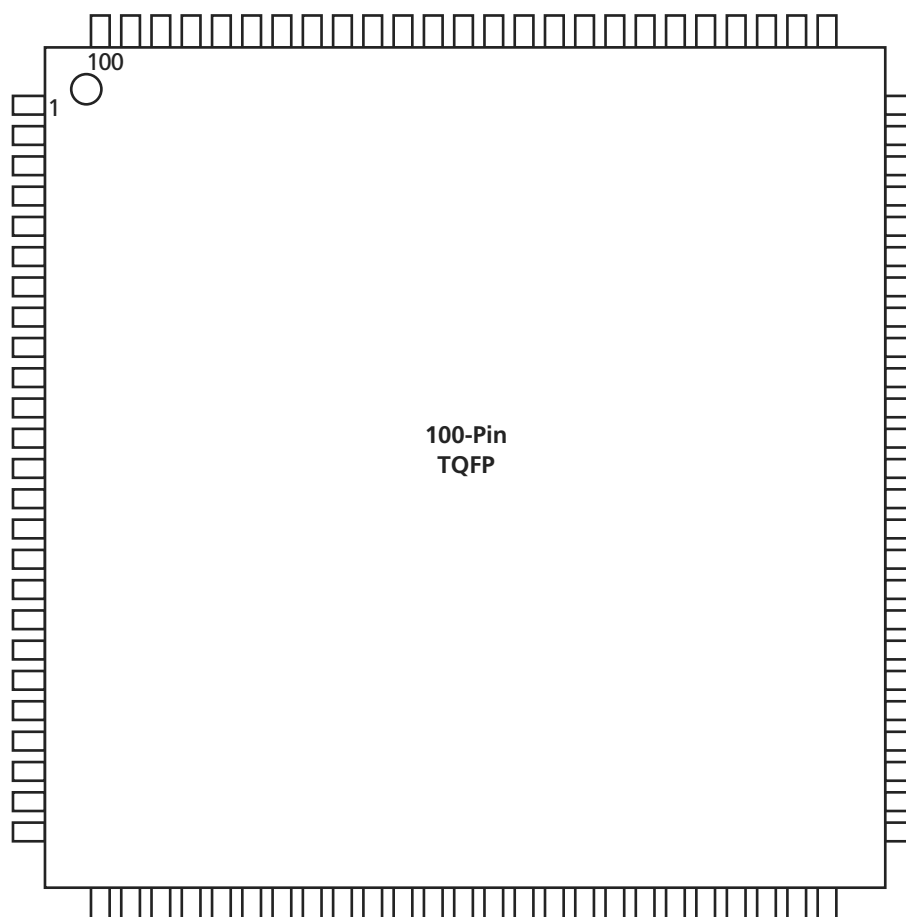


Figure 3-2 • 100-Pin TQFP

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA	
Pin Number	A54SX32A Function
A1	GND
A2	GND
A3	V <sub>CCI</sub>
A4	NC
A5	I/O
A6	I/O
A7	V <sub>CCI</sub>
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V <sub>CCI</sub>
A23	GND
AA1	V <sub>CCI</sub>
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O
AA13	I/O
AA14	I/O

329-Pin PBGA	
Pin Number	A54SX32A Function
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V <sub>CCI</sub>
AA22	I/O
AA23	V <sub>CCI</sub>
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND
AC2	V <sub>CCI</sub>
AC3	NC
AC4	I/O
AC5	I/O

329-Pin PBGA	
Pin Number	A54SX32A Function
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V <sub>CCI</sub>
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC
AC22	V <sub>CCI</sub>
AC23	GND
B1	V <sub>CCI</sub>
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O

329-Pin PBGA	
Pin Number	A54SX32A Function
B20	I/O
B21	I/O
B22	GND
B23	V <sub>CCI</sub>
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	V <sub>CCI</sub>
C22	GND
C23	NC
D1	I/O
D2	I/O
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H6	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H7	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
H8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
H9	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

## 256-Pin FBGA

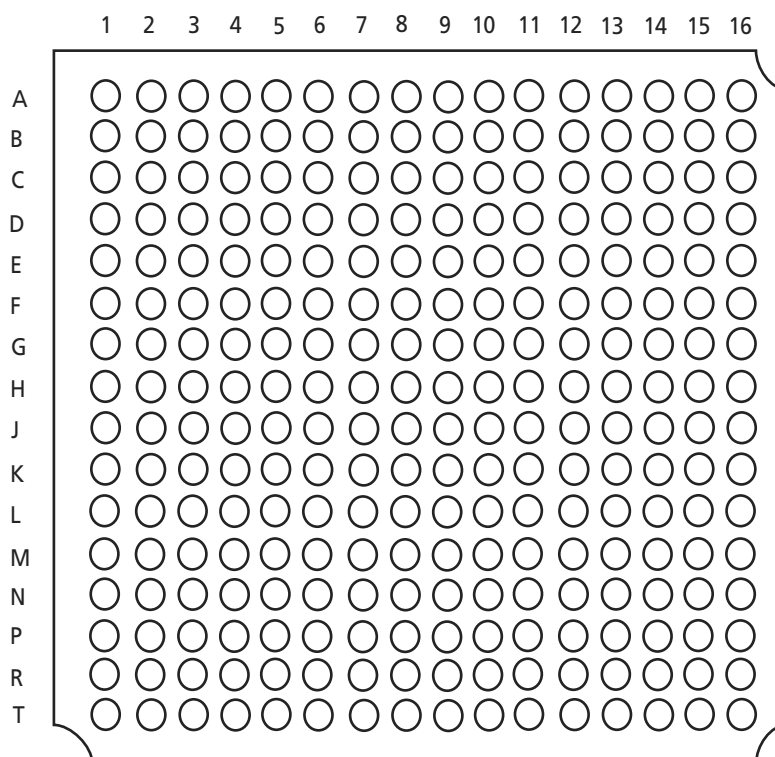


Figure 3-7 • 256-Pin FBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.



256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND
C4	I/O	I/O	I/O
C5	NC	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O
E7	I/O	I/O	QCLKC
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
K5	I/O	I/O	I/O
K6	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
L8	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
L9	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
L10	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
P14	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

## 484-Pin FBGA

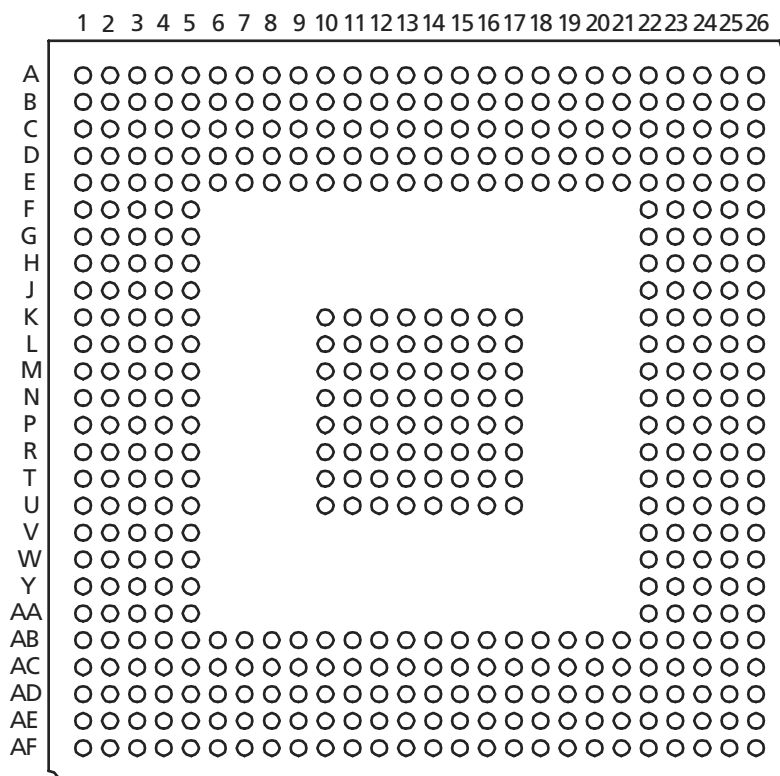


Figure 3-8 • 484-Pin FBGA (Top View)

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V <sub>CCI</sub>	V <sub>CCI</sub>
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V <sub>CCI</sub>	V <sub>CCI</sub>
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V <sub>CCI</sub>	V <sub>CCI</sub>
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V <sub>CCA</sub>	V <sub>CCA</sub>
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V <sub>CCI</sub>	V <sub>CCI</sub>
E26	GND	GND
F1	V <sub>CCI</sub>	V <sub>CCI</sub>
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V <sub>CCA</sub>	V <sub>CCA</sub>
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V <sub>CCI</sub>	V <sub>CCI</sub>
J26	NC*	I/O
K1	I/O	I/O
K2	V <sub>CCI</sub>	V <sub>CCI</sub>
K3	I/O	I/O
K4	I/O	I/O
K5	V <sub>CCA</sub>	V <sub>CCA</sub>

**Note:** \*These pins must be left floating on the A54SX32A device.