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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

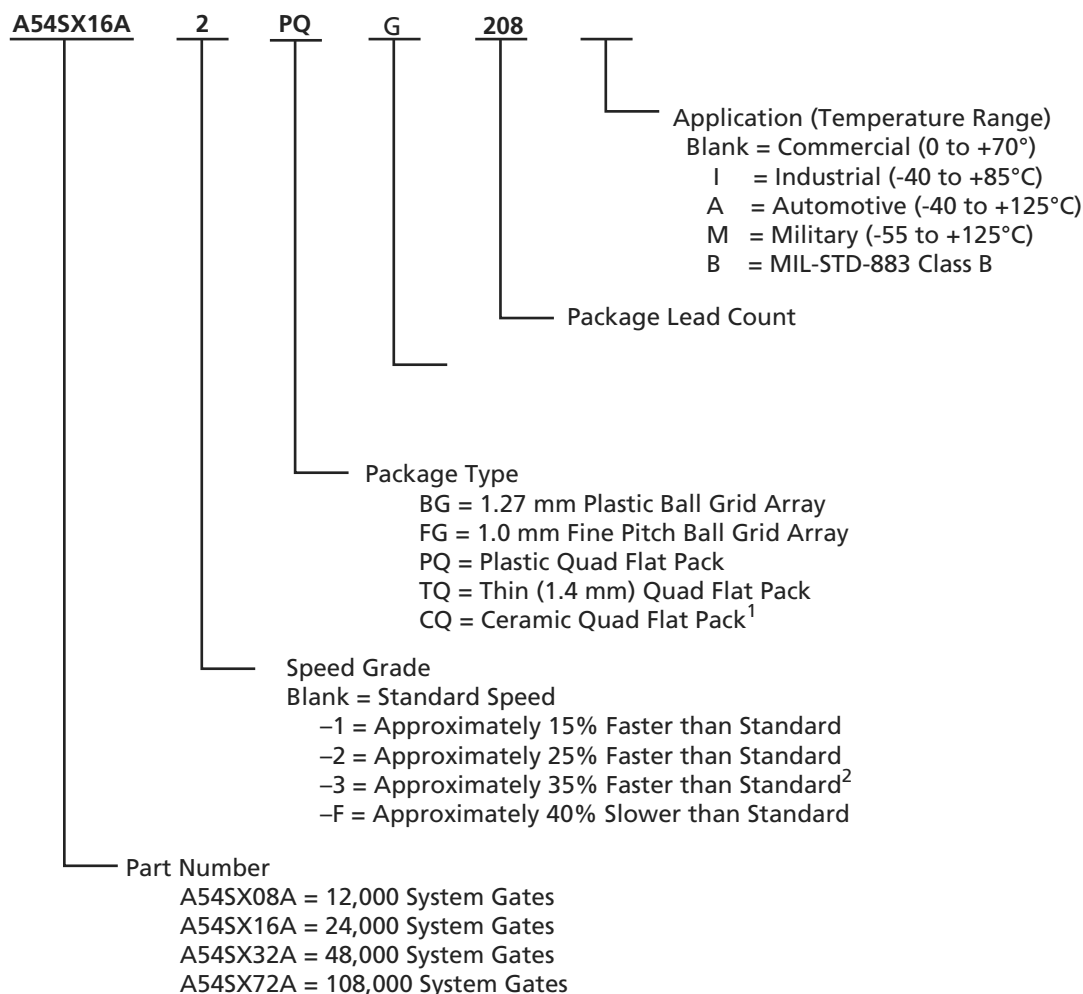
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	12000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx08a-tqg144i

Ordering Information



Notes:

- For more information about the CQFP package options, refer to the HiRel SX-A datasheet.
- All -3 speed grades have been discontinued.

Device Resources

Device	User I/Os (Including Clock Buffers)							
	208-Pin PQFP	100-Pin TQFP	144-Pin TQFP	176-Pin TQFP	329-Pin PBGA	144-Pin FBGA	256-Pin FBGA	484-Pin FBGA
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices and Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • **SX-A Clock Resources**

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

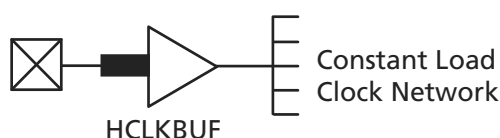


Figure 1-7 • **SX-A HCLK Clock Buffer**

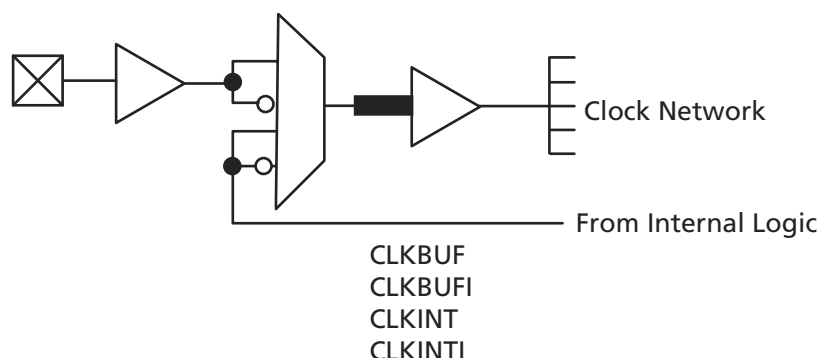


Figure 1-8 • **SX-A Routed Clock Buffer**

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CC} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a $70\ \Omega$ series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The $70\ \Omega$ series termination is used to prevent data transmission corruption during probing and reading back the checksum.

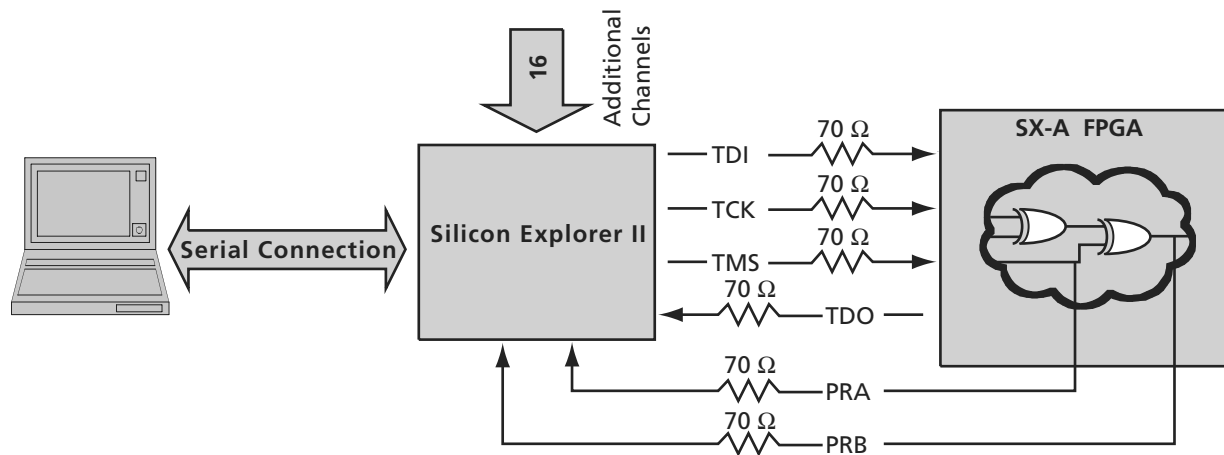


Figure 1-13 • Probe Setup

Pin Description

CLKA/B, I/O Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND Ground

Low supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC No Connection

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user I/O when checksum is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CC} Supply Voltage

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CC} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

Table 2-8 • AC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ ¹	-44	–	mA
		$1.4 \leq V_{OUT} < 2.4$ ^{1, 2}	$(-44 + (V_{OUT} - 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ ^{1, 3}	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ ³	–	-142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ ¹	95	–	mA
		$2.2 > V_{OUT} > 0.55$ ¹	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ ^{1, 3}	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ ³	–	206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Notes:

1. Refer to the *VII* curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

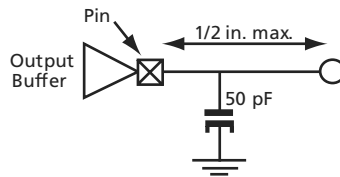


Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

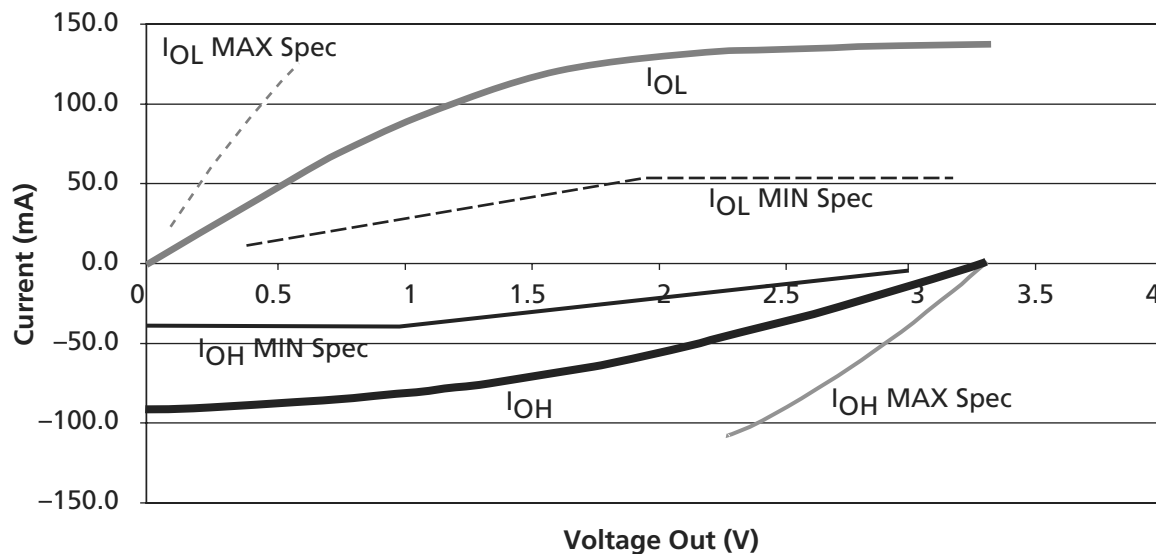


Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

for $0.7 V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CCI}$

EQ 2-4

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) = f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX*, *SX-A* and *RT54SX-S* *Power Calculator* worksheet.

Output Buffer Delays

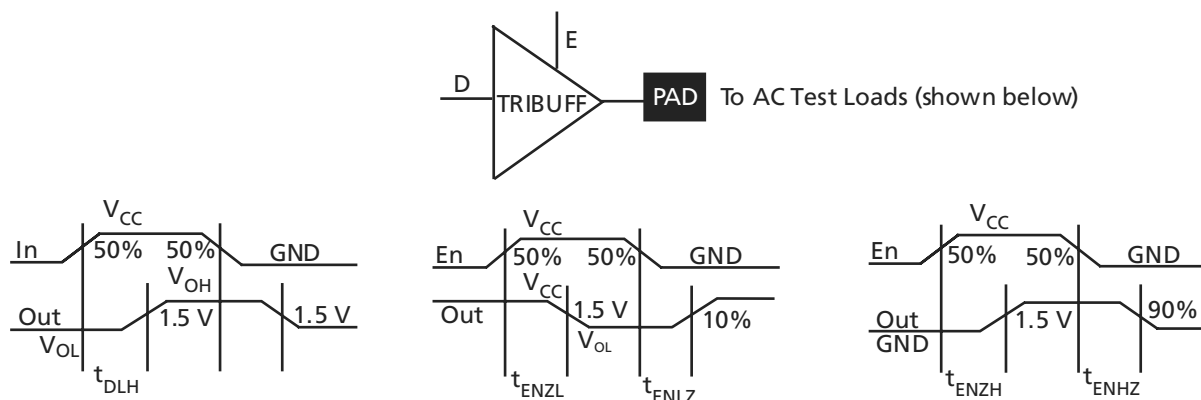


Figure 2-4 • Output Buffer Delays

AC Test Loads

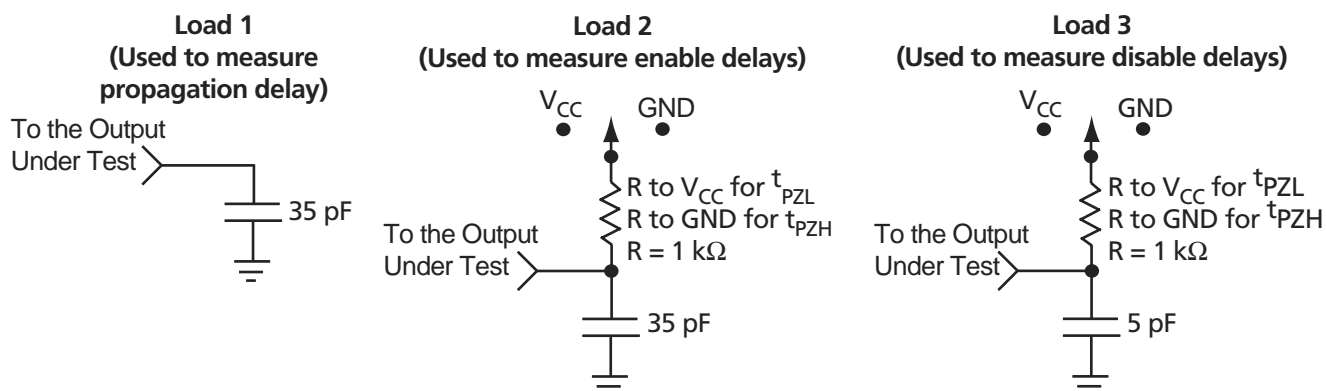


Figure 2-5 • AC Test Loads

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.25\text{ V}$)

V_{CCA}	Junction Temperature (T_J)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-14 • A54SX08A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays²										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-15 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)	1.4		1.6		1.8		2.6		ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)	1.3		1.5		1.7		2.4		ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew	0.4		0.4		0.5		0.7		ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency	313		278		238		172		MHz
Routed Array Clock Networks										
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)	1.0		1.1		1.3		1.8		ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)	1.0		1.1		1.3		1.8		ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.4		ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)	0.7		0.8		0.9		1.3		ns
t _{RCKSW}	Maximum Skew (50% Load)	0.7		0.8		0.9		1.3		ns
t _{RCKSW}	Maximum Skew (100% Load)	0.9		1.0		1.2		1.7		ns

Table 2-19 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.2		2.4		2.9		4.0		ns
t _{DHL}	Data-to-Pad High to Low	2.3		2.6		3.1		4.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.4		2.9		4.0		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.3		2.6		3.1		4.3		ns
d _{TLH} ²	Delta Low to High	0.03		0.03		0.04		0.045		ns/pF
d _{THL} ²	Delta High to Low	0.015		0.015		0.015		0.025		ns/pF
3.3 V LVTTTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	3.0		3.4		4.0		5.6		ns
t _{DHL}	Data-to-Pad High to Low	3.0		3.3		3.9		5.5		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.4		11.8		13.8		19.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	3		3.4		4		5.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3		3.3		3.9		5.5		ns
d _{TLH} ²	Delta Low to High	0.03		0.03		0.04		0.045		ns/pF
d _{THL} ²	Delta High to Low	0.015		0.015		0.015		0.025		ns/pF
d _{THLS} ²	Delta High to Low—low slew	0.053		0.067		0.073		0.107		ns/pF

Notes:

- Delays based on 10 pF loading and 25 Ω resistance.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-20 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ¹										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH} ²	Delta Low to High	0.016		0.02		0.022		0.032		ns/pF
d _{THL} ²	Delta High to Low	0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.2		4.5		ns
t _{DHL}	Data-to-Pad High to Low	3.2		3.6		4.2		5.9		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.6		8.6		10.1		14.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.2		4.5		ns
t _{ENLZ}	Enable-to-Pad, L to Z	4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2		3.6		4.2		5.9		ns
d _{TLH}	Delta Low to High	0.017		0.017		0.023		0.031		ns/pF
d _{THL}	Delta High to Low	0.029		0.031		0.037		0.051		ns/pF
d _{THLS}	Delta High to Low—low slew	0.046		0.057		0.066		0.089		ns/pF

Notes:

- Delays based on 50 pF loading.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
- Delays based on 35 pF loading.

Table 2-25 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{2, 3}												
t _{DLH}	Data-to-Pad Low to High		3.4		3.9		4.5		5.2		7.3	ns
t _{DHL}	Data-to-Pad High to Low		2.6		3.0		3.3		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		11.6		13.4		15.2		17.9		25.0	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.4		3.9		4.5		5.2		7.3	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.6		3.0		3.3		3.9		5.5	ns
d _{TLH} ⁴	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ⁴	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ⁴	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-35 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	1.0		1.1		1.3		1.5		2.0		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.7		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.6		0.7		1		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.7		0.8		0.9		1.3		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.9		1		1.1		1.5		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.5		1.7		2.1		2.9		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2.2		2.5		3		4.2		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.7		0.8		0.9		1.1		1.5		ns
t _{CLR}	Asynchronous Clear-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.8		1.0		1.4		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.3		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	0.8		1.0		1.1		1.3		1.7		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.6		0.7		0.7		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.0		1.4		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTL	0.7		0.7		0.8		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL	1.0		1.2		1.3		1.5		2.1		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

144-Pin FBGA

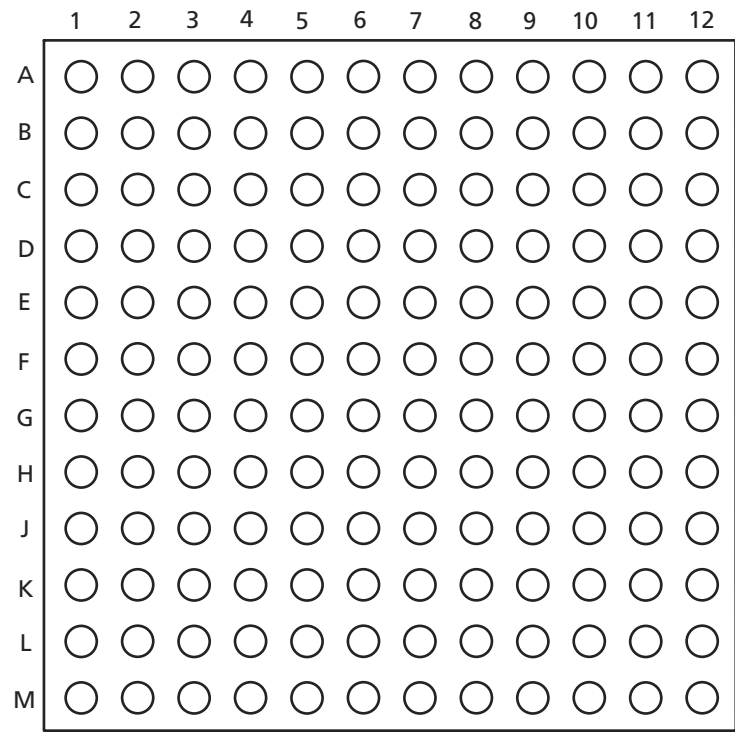


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

484-Pin FBGA

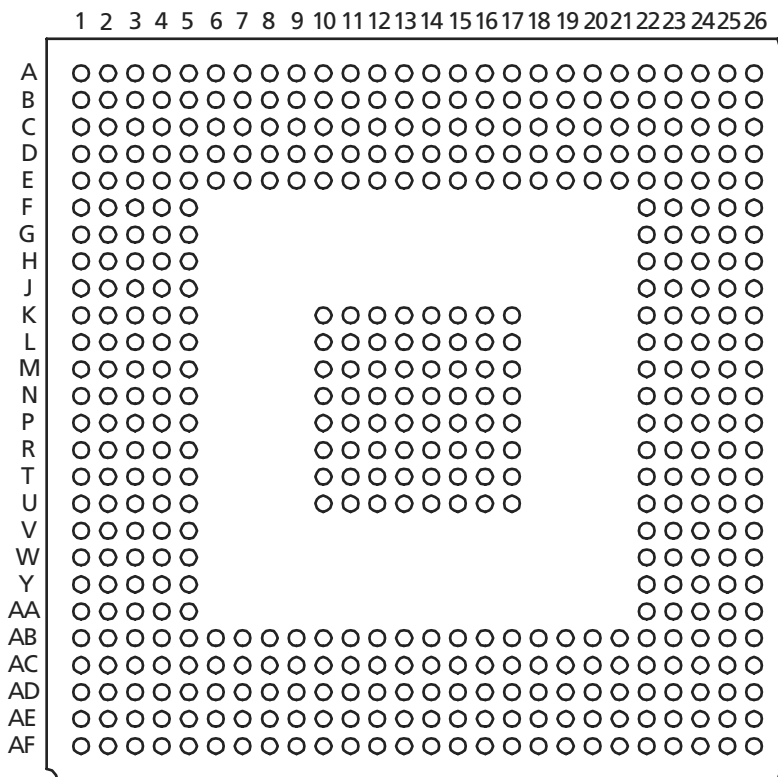


Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200

Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom

Phone +44 (0) 1276 609 300

Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671

Fax +81.03.3445.7668

www.jp.actel.com

Actel Hong Kong

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460

Fax +852 2185 6488

www.actel.com.cn