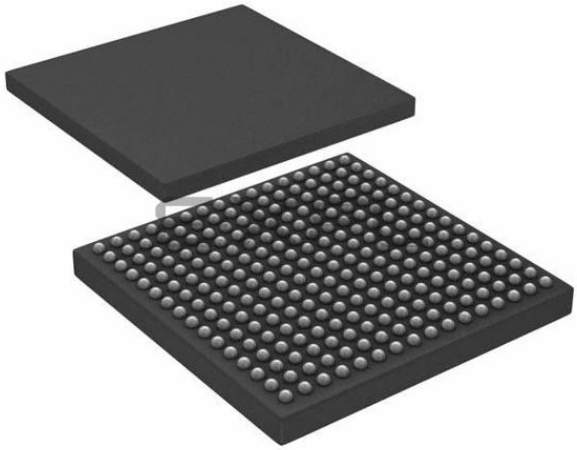

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

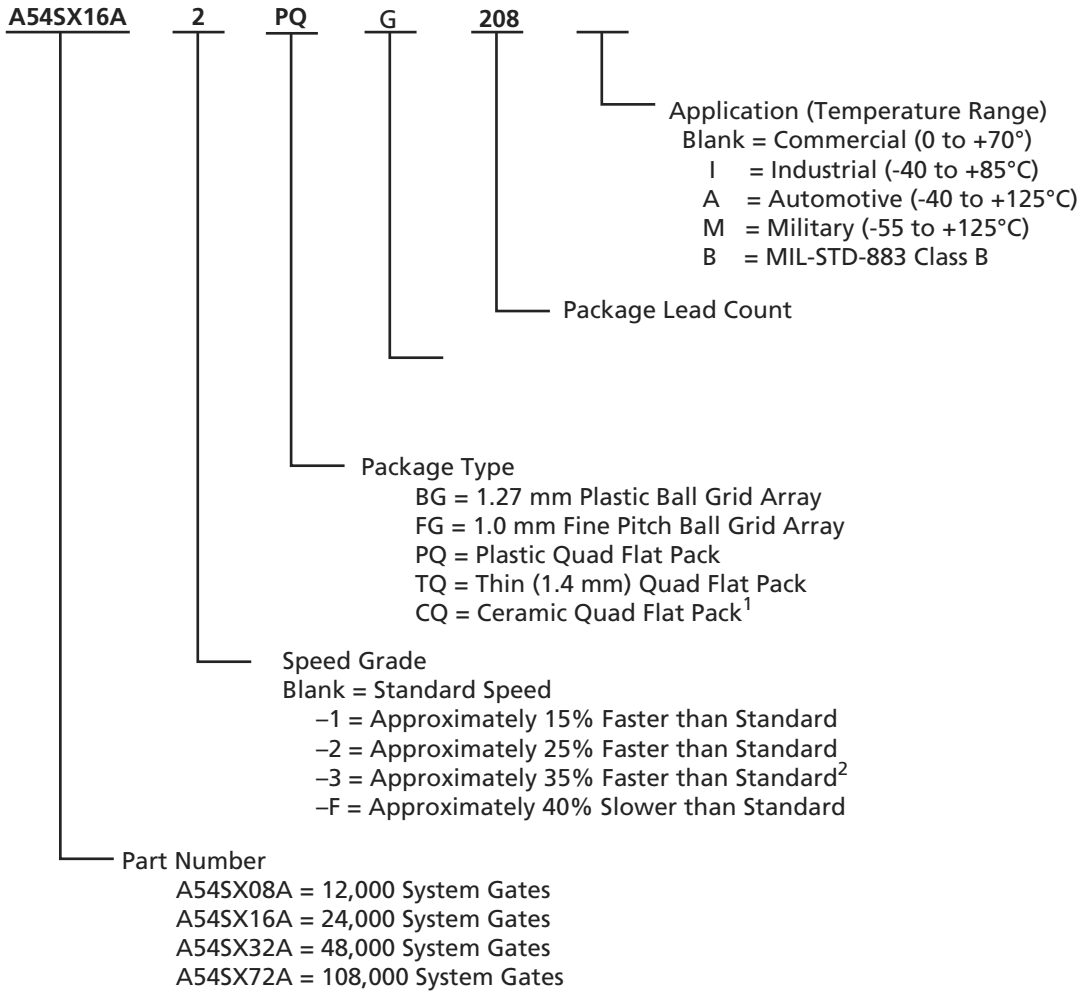
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 180 |
| Number of Gates | 24000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx16a-1fg256i |

# Ordering Information




***Notes:***

1. *For more information about the CQFP package options, refer to the* HiRel SX-A datasheet.
2. *All –3 speed grades have been discontinued.*

# Device Resources

| | User I/Os (Including Clock Buffers) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Device** | **208-Pin PQFP** | **100-Pin TQFP** | **144-Pin TQFP** | **176-Pin TQFP** | **329-Pin PBGA** | **144-Pin FBGA** | **256-Pin FBGA** | **484-Pin FBGA** |
| A54SX08A | 130 | 81 | 113 | – | – | 111 | – | – |
| A54SX16A | 175 | 81 | 113 | – | – | 111 | 180 | – |
| A54SX32A | 174 | 81 | 113 | 147 | 249 | 111 | 203 | 249 |
| A54SX72A | 171 | – | – | – | – | – | 203 | 360 |

***Notes:*** *Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array*

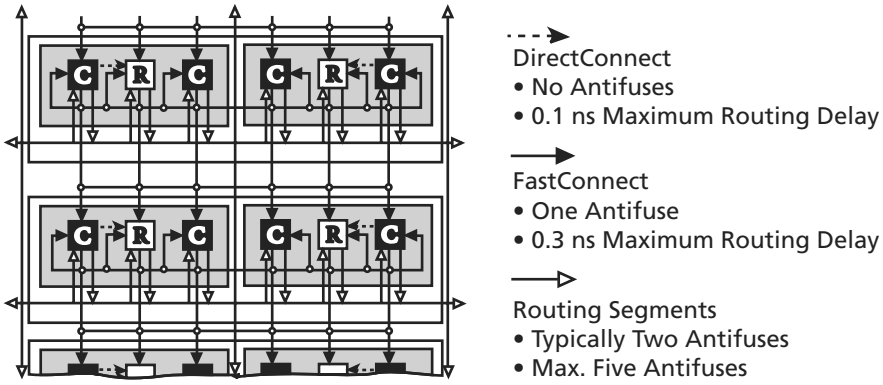



*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

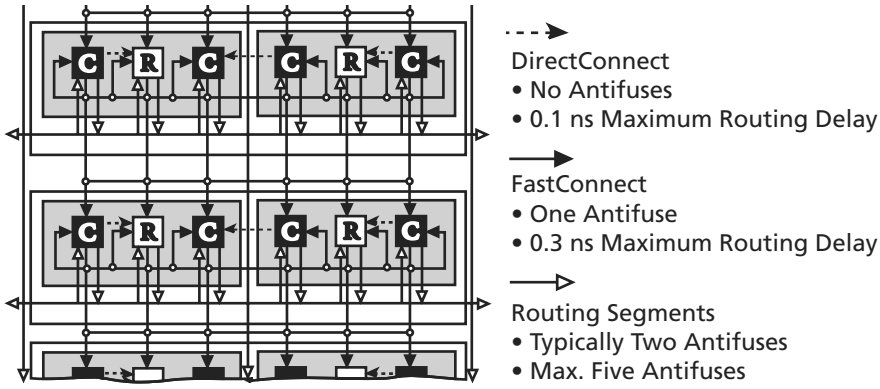



*Figure 1-6* • **DirectConnect and FastConnect for Type 2 SuperClusters**

## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

## Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

*Figure 1-12* • **Device Selection Wizard**

*Table 1-5* • **Reserve Pin Definitions**

| Pin | Function |
|---|---|
| Reserve JTAG | Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS) |
| Reserve JTAG Test Reset | Regular I/O or JTAG reset with an internal pull-up |
| Reserve Probe | Keeps pins from being used or regular I/O |

## Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to $V_{CCI}$ should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

*Table 1-6* • **Boundary-Scan Pin Configurations and Functions**

| Mode | Designer "Reserve JTAG" Selection | TAP Controller State |
|---|---|---|
| Dedicated (JTAG) | Checked | Any |
| Flexible (User I/O) | Unchecked | Test-Logic-Reset |
| Flexible (JTAG) | Unchecked | Any EXCEPT Test-Logic-Reset |

## TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

# Pin Description

**CLKA/B, I/O Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

**QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

**GND Ground**

Low supply voltage.

**HCLK Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

**I/O Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

**NC No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

**PRA/B, I/O Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK, I/O Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI, I/O Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO, I/O Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

**TMS Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**TRST, I/O Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

**$V_{CCI}$ Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All $V_{CCI}$ power pins in the device should be connected.

**$V_{CCA}$ Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All $V_{CCA}$ power pins in the device should be connected.

## Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) =f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 2-14*

where:

$\theta_{CS}$ = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

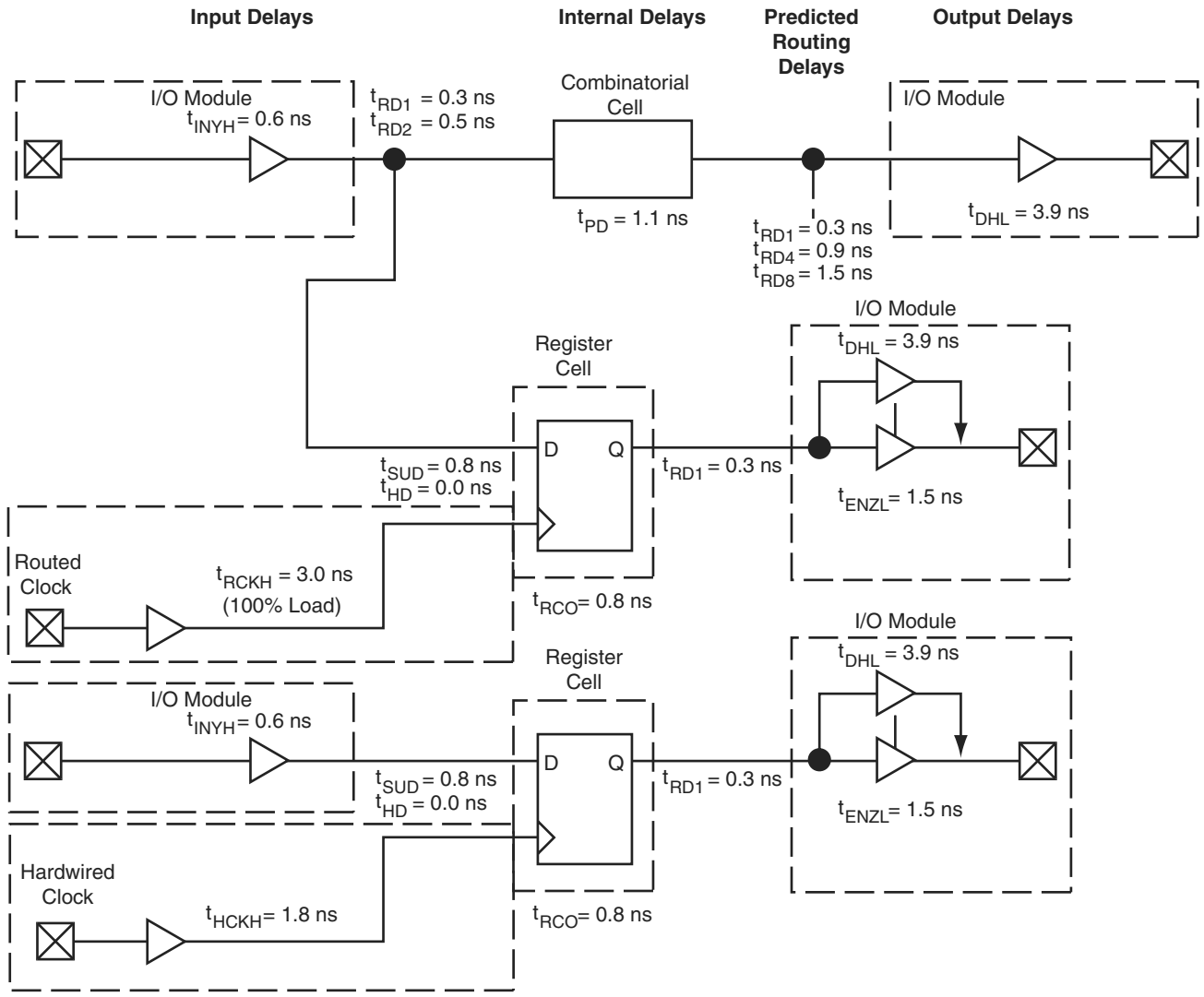
$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

# SX-A Timing Model




***Note:*** **Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route.*

*Figure 2-3* • **SX-A Timing Model**

# Sample Path Calculations

## Hardwired Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH}$
= 0.6 + 0.3 + 0.8 - 1.8 = – 0.1 ns

Clock-to-Out (Pad-to-Pad) = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 ns

## Routed Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH}$
= 0.6 + 0.3 + 0.8 - 3.0 = –1.3 ns

Clock-to-Out (Pad-to-Pad) = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 ns

# Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

## Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

## Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

## Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

# Temperature and Voltage Derating Factors

*Table 2-13* • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, $T_J$ = 70°C, $V_{CCA}$ = 2.25 V)**

| | **Junction Temperature ($T_J$)** | | | | | | |
|---|---|---|---|---|---|---|---|
| **$V_{CCA}$** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 2.250 V | 0.79 | 0.80 | 0.87 | 0.89 | 1.00 | 1.04 | 1.14 |
| 2.500 V | 0.74 | 0.75 | 0.82 | 0.83 | 0.94 | 0.97 | 1.07 |
| 2.750 V | 0.68 | 0.69 | 0.75 | 0.77 | 0.87 | 0.90 | 0.99 |

*Table 2-20* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **5 V PCI Output Module Timing[1]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$[2] | Delta Low to High | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[2] | Delta High to Low | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[3]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$ | Delta High to Low—low slew | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *Delays based on 50 pF loading.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})$ / $(C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
3. *Delays based on 35 pF loading.*

*Table 2-21* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.6 | | 1.9 | | 2.7 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-23* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-28* • **A54SX32A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-33* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **3.3 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 1.9 | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 1.9 | | 2.2 | | 2.4 | | 2.9 | | 4.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 9.0 | | 10.4 | | 11.8 | | 13.8 | | 19.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-39* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.3 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **2.5 V LVCMOS Output Module Timing[2, 3]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.9 | | 4.5 | | 5.1 | | 6.0 | | 8.4 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 6.7 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 12.7 | | 14.6 | | 16.5 | | 19.4 | | 27.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.9 | | 4.5 | | 5.1 | | 6.0 | | 8.4 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.1 | | 3.6 | | 4.1 | | 4.8 | | 6.7 | ns |
| $d_{TLH}$[4] | Delta Low to High | | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[4] | Delta High to Low | | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[4] | Delta High to Low—low slew | | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O | I/O |
| 73 | NC | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | QCLKA |
| 75 | NC | I/O | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O | PRB,I/O |
| 77 | GND | GND | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND | GND | GND |
| 80 | NC | NC | NC | NC |
| 81 | I/O | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O | $V_{CCI}$ |
| 84 | I/O | I/O | I/O | QCLKB |
| 85 | NC | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O | I/O |
| 88 | NC | I/O | I/O | I/O |
| 89 | I/O | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O | I/O |
| 91 | NC | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O | I/O |
| 94 | NC | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O | I/O |
| 97 | NC | I/O | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O | I/O |
| 105 | GND | GND | GND | GND |

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 106 | NC | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O | I/O |
| 108 | NC | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | NC | I/O | I/O | GND |
| 117 | I/O | I/O | I/O | $V_{CCA}$ |
| 118 | I/O | I/O | I/O | I/O |
| 119 | NC | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O | I/O |
| 122 | NC | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O | I/O |
| 125 | NC | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O | I/O |
| 129 | GND | GND | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND | GND | GND |
| 132 | NC | NC | NC | I/O |
| 133 | I/O | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O | I/O |
| 135 | NC | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O | I/O |
| 138 | NC | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | NC | NC | NC |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | TRST, I/O | TRST, I/O | TRST, I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |
| 37 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | NC | NC | NC |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |

| 144-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| G1 | I/O | I/O | I/O |
| G2 | GND | GND | GND |
| G3 | I/O | I/O | I/O |
| G4 | I/O | I/O | I/O |
| G5 | GND | GND | GND |
| G6 | GND | GND | GND |
| G7 | GND | GND | GND |
| G8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| G9 | I/O | I/O | I/O |
| G10 | I/O | I/O | I/O |
| G11 | I/O | I/O | I/O |
| G12 | I/O | I/O | I/O |
| H1 | TRST, I/O | TRST, I/O | TRST, I/O |
| H2 | I/O | I/O | I/O |
| H3 | I/O | I/O | I/O |
| H4 | I/O | I/O | I/O |
| H5 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H6 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| H9 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| H10 | I/O | I/O | I/O |
| H11 | I/O | I/O | I/O |
| H12 | NC | NC | NC |
| J1 | I/O | I/O | I/O |
| J2 | I/O | I/O | I/O |
| J3 | I/O | I/O | I/O |
| J4 | I/O | I/O | I/O |
| J5 | I/O | I/O | I/O |
| J6 | PRB, I/O | PRB, I/O | PRB, I/O |
| J7 | I/O | I/O | I/O |
| J8 | I/O | I/O | I/O |
| J9 | I/O | I/O | I/O |
| J10 | I/O | I/O | I/O |
| J11 | I/O | I/O | I/O |
| J12 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |

| 144-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| K1 | I/O | I/O | I/O |
| K2 | I/O | I/O | I/O |
| K3 | I/O | I/O | I/O |
| K4 | I/O | I/O | I/O |
| K5 | I/O | I/O | I/O |
| K6 | I/O | I/O | I/O |
| K7 | GND | GND | GND |
| K8 | I/O | I/O | I/O |
| K9 | I/O | I/O | I/O |
| K10 | GND | GND | GND |
| K11 | I/O | I/O | I/O |
| K12 | I/O | I/O | I/O |
| L1 | GND | GND | GND |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | HCLK | HCLK | HCLK |
| L8 | I/O | I/O | I/O |
| L9 | I/O | I/O | I/O |
| L10 | I/O | I/O | I/O |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| M8 | I/O | I/O | I/O |
| M9 | I/O | I/O | I/O |
| M10 | I/O | I/O | I/O |
| M11 | TDO, I/O | TDO, I/O | TDO, I/O |
| M12 | I/O | I/O | I/O |

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v4.0 (continued) | Table 2-12 was updated. | 2-11 |
| | The was updated. | 2-14 |
| | The "Sample Path Calculations" were updated. | 2-14 |
| | Table 2-13 was updated. | 2-17 |
| | Table 2-13 was updated. | 2-17 |
| | All timing tables were updated. | 2-18 to 2-52 |
| v3.0 | The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated. | 1-i |
| | The "Ordering Information" section was updated. | 1-ii |
| | The "Temperature Grade Offering" section was updated. | 1-iii |
| | The Figure 1-1 • SX-A Family Interconnect Elements was updated. | 1-1 |
| | The ""Clock Resources" section"was updated | 1-5 |
| | The Table 1-1 • SX-A Clock Resources is new. | 1-5 |
| | The "User Security" section is new. | 1-7 |
| | The "I/O Modules" section was updated. | 1-7 |
| | The Table 1-2 • I/O Features was updated. | 1-8 |
| | The Table 1-3 • I/O Characteristics for All I/O Configurations is new. | 1-8 |
| | The Table 1-4 • Power-Up Time at which I/Os Become Active is new | 1-8 |
| | The Figure 1-12 • Device Selection Wizard is new. | 1-9 |
| | The "Boundary-Scan Pin Configurations and Functions" section is new. | 1-9 |
| | The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new. | 1-11 |
| | The "SX-A Probe Circuit Control Pins" section was updated. | 1-12 |
| | The "Design Considerations" section was updated. | 1-12 |
| | The Figure 1-13 • Probe Setup was updated. | 1-12 |
| | The Design Environment was updated. | 1-13 |
| | The Figure 1-13 • Design Flow is new. | 1-11 |
| | The "Absolute Maximum Ratings*" section was updated. | 1-12 |
| | The "Recommended Operating Conditions" section was updated. | 1-12 |
| | The "Electrical Specifications" section was updated. | 1-12 |
| | The "2.5V LVCMOS2 Electrical Specifications" section was updated. | 1-13 |
| | The "SX-A Timing Model" and "Sample Path Calculations" equations were updated. | 1-23 |
| | The "Pin Description" section was updated. | 1-15 |
| v2.0.1 | The "Design Environment" section has been updated. | 1-13 |
| | The "I/O Modules" section, and Table 1-2 • I/O Features have been updated. | 1-8 |
| | The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers. | 1-23 |

# Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

## Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

## Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

## Unmarked (production)

This datasheet version contains information that is considered to be final.

## Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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