



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

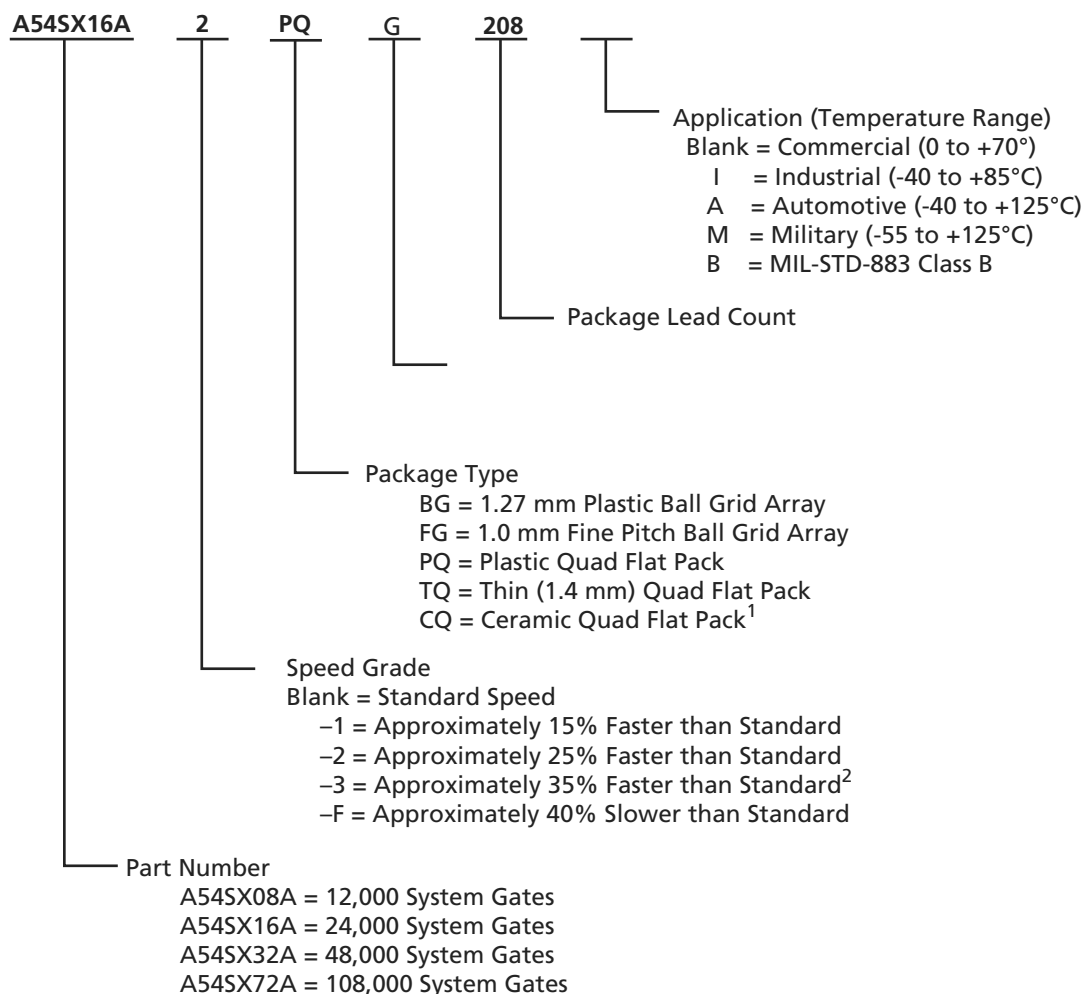
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-1tq100

Ordering Information



Notes:

- For more information about the CQFP package options, refer to the HiRel SX-A datasheet.
- All -3 speed grades have been discontinued.

Device Resources

Device	User I/Os (Including Clock Buffers)							
	208-Pin PQFP	100-Pin TQFP	144-Pin TQFP	176-Pin TQFP	329-Pin PBGA	144-Pin FBGA	256-Pin FBGA	484-Pin FBGA
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

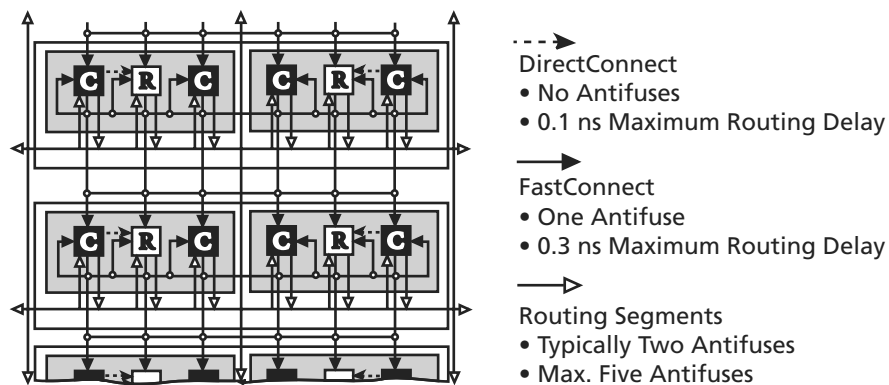


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

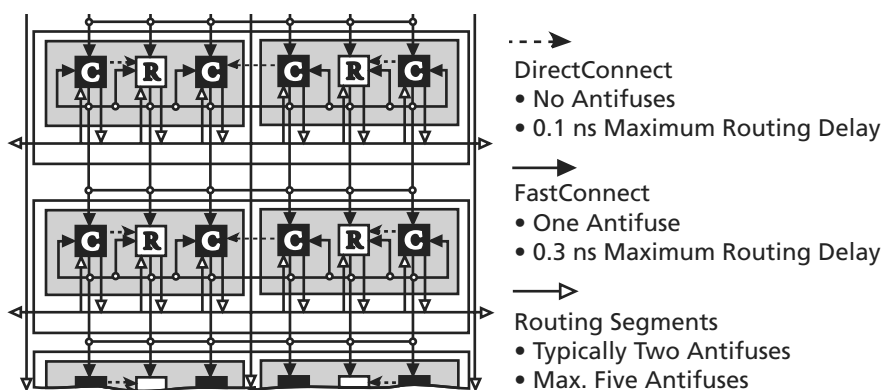


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

Where:

- C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
 C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
 C_{EQI} = Equivalent capacitance of input buffers in pF
 C_{EQO} = Equivalent capacitance of output buffers in pF
 C_{EQCR} = Equivalent capacitance of CLKA/B in pF
 C_{EQHV} = Variable capacitance of HCLK in pF
 C_{EQHF} = Fixed capacitance of HCLK in pF
 C_L = Output lead capacitance in pF
 f_m = Average logic module switching rate in MHz
 f_n = Average input buffer switching rate in MHz
 f_p = Average output buffer switching rate in MHz
 f_{q1} = Average CLKA rate in MHz
 f_{q2} = Average CLKB rate in MHz
 f_{s1} = Average HCLK rate in MHz
 m = Number of logic modules switching at f_m
 n = Number of input buffers switching at f_n
 p = Number of output buffers switching at f_p
 q_1 = Number of clock loads on CLKA
 q_2 = Number of clock loads on CLKB
 r_1 = Fixed capacitance due to CLKA
 r_2 = Fixed capacitance due to CLKB
 s_1 = Number of clock loads on HCLK
 x = Number of I/Os at logic low
 y = Number of I/Os at logic high

Table 2-11 • CEQ Values for SX-A Devices

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQSM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_C = Ambient temperature
- P = total power dissipated by the device

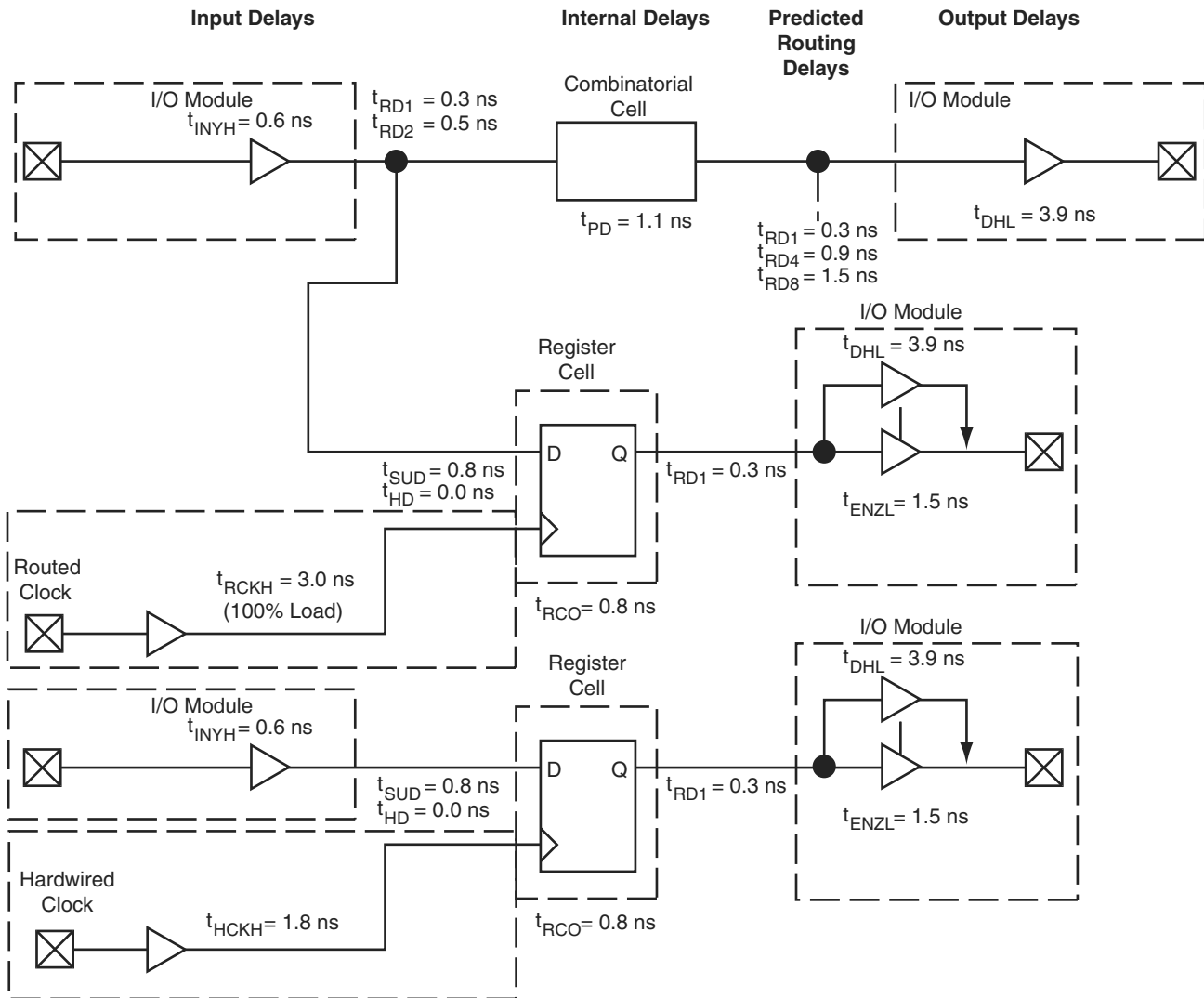
Table 2-12 • Package Thermal Characteristics

Package Type	Pin Count	θ_{JC}	θ_{JA}			Units
			Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP) ¹	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader ²	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

- The A54SX08A PQ208 has no heat spreader.
- The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

SX-A Timing Model



Note: *Values shown for A54SX72A, -2, worst-case commercial conditions at 5 V PCI with standard place-and-route.

Figure 2-3 • SX-A Timing Model

Sample Path Calculations

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH} \\ &= 0.6 + 0.3 + 0.8 - 1.8 = -0.1 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.8 + 0.8 + 0.3 + 3.9 = 6.8 \text{ ns} \end{aligned}$$

Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH} \\ &= 0.6 + 0.3 + 0.8 - 3.0 = -1.3 \text{ ns} \\ \text{Clock-to-Out (Pad-to-Pad)} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 3.0 + 0.8 + 0.3 + 3.9 = 8.0 \text{ ns} \end{aligned}$$

Input Buffer Delays

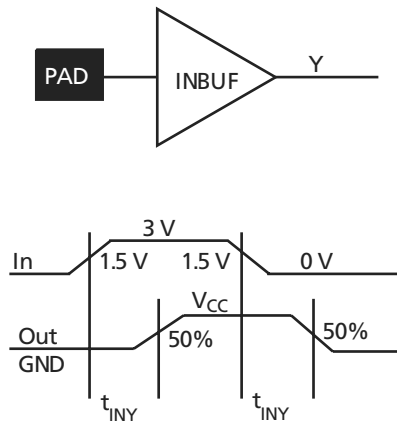


Figure 2-6 • Input Buffer Delays

C-Cell Delays

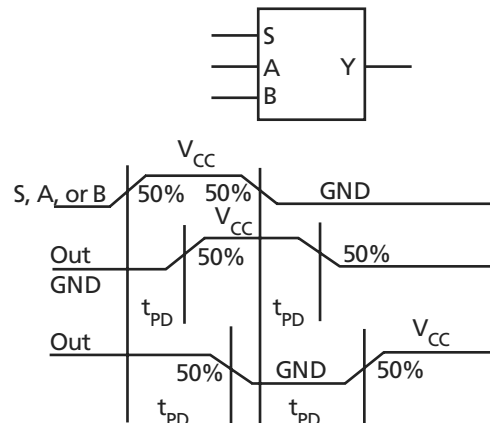


Figure 2-7 • C-Cell Delays

Cell Timing Characteristics

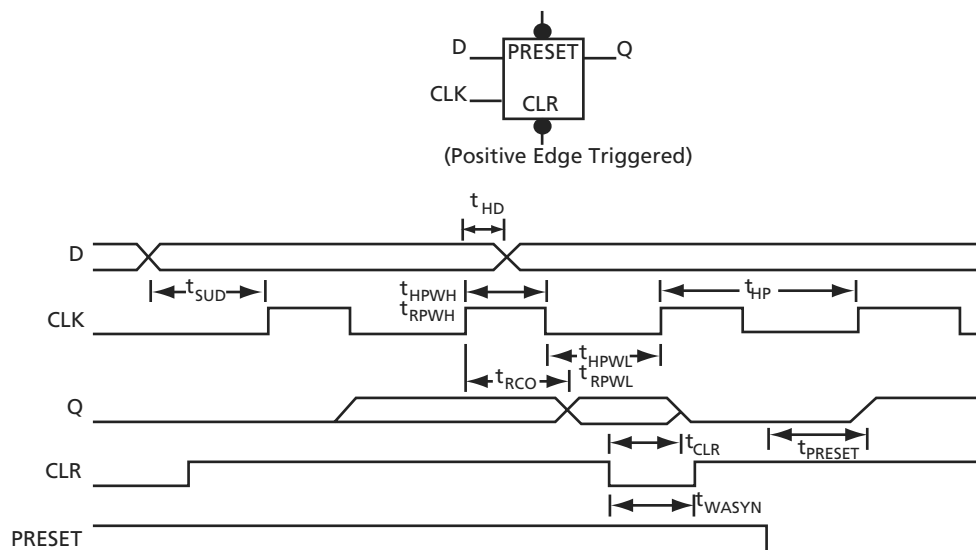


Figure 2-8 • Flip-Flops

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{1,2}										
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-22 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-30 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.3		2.7		3.1		3.6		5	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.1	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-36 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing ²												
t _{DLH}	Data-to-Pad Low to High	2.7		3.1		3.5		4.1		5.7		ns
t _{DHL}	Data-to-Pad High to Low	3.4		3.9		4.4		5.1		7.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.7		3.1		3.5		4.1		5.7		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.4		3.9		4.4		5.1		7.2		ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032		ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052		ns/pF
5 V TTL Output Module Timing ⁴												
t _{DLH}	Data-to-Pad Low to High	2.4		2.8		3.1		3.7		5.1		ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.5		4.0		4.7		6.6		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	7.4		8.5		9.7		11.4		15.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.4		2.8		3.1		3.7		5.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.5		4.0		4.7		6.6		ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031		ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051		ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089		ns/pF

Notes:

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[HL|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

176-Pin TQFP

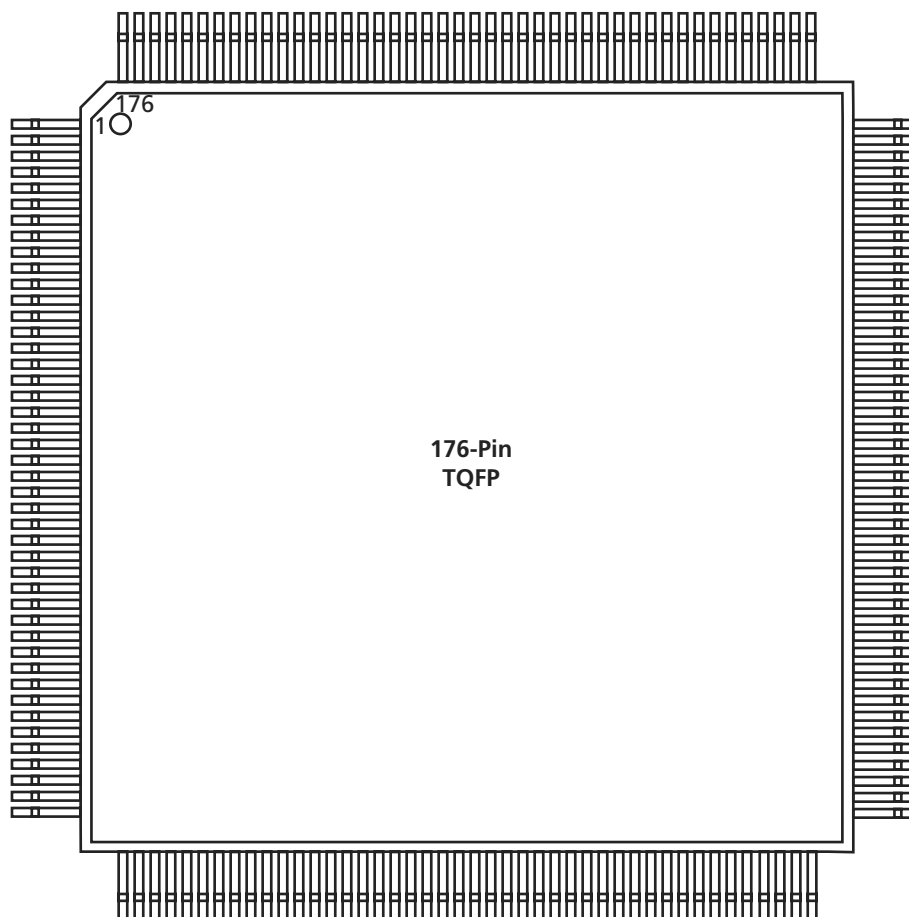


Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin FBGA

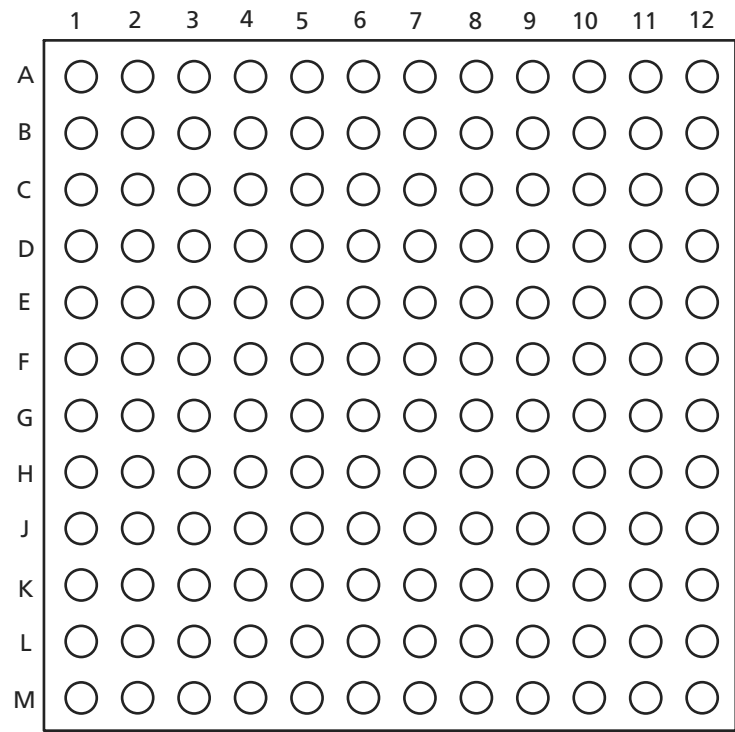


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V _{CCA}	V _{CCA}	V _{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D1	I/O	I/O	I/O
D2	V _{CCI}	V _{CCI}	V _{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V _{CCI}	V _{CCI}	V _{CCI}
E7	V _{CCI}	V _{CCI}	V _{CCI}
E8	V _{CCI}	V _{CCI}	V _{CCI}
E9	V _{CCA}	V _{CCA}	V _{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A545X16A Function	A545X32A Function	A545X72A Function
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V _{CCI}	V _{CCI}	V _{CCI}
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	V _{CCI}	V _{CCI}	V _{CCI}
F10	V _{CCI}	V _{CCI}	V _{CCI}
F11	I/O	I/O	I/O
F12	V _{CCA}	V _{CCA}	V _{CCA}
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V _{CCI}	V _{CCI}	V _{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V _{CCI}	V _{CCI}	V _{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V _{CCA}	V _{CCA}	V _{CCA}

256-Pin FBGA			
Pin Number	A545X16A Function	A545X32A Function	A545X72A Function
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V _{CCA}	V _{CCA}	V _{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V _{CCI}	V _{CCI}	V _{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V _{CCI}	V _{CCI}	V _{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V _{CCI}	V _{CCI}	V _{CCI}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V _{CCI}	V _{CCI}	V _{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V _{CCA}	V _{CCA}	V _{CCA}

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V _{CCI}	V _{CCI}
AD24	NC*	I/O
AD25	NC*	I/O
AD26	NC*	I/O
AE1	NC*	NC
AE2	I/O	I/O
AE3	NC*	I/O
AE4	NC*	I/O
AE5	NC*	I/O
AE6	NC*	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	NC*	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	NC*	I/O
AE16	NC*	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	NC*	I/O
AE22	NC*	I/O
AE23	NC*	I/O
AE24	NC*	I/O
AE25	NC*	NC
AE26	NC*	NC

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AF1	NC*	NC
AF2	NC*	NC
AF3	NC	I/O
AF4	NC*	I/O
AF5	NC*	I/O
AF6	NC*	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	NC*	I/O
AF12	NC*	NC
AF13	HCLK	HCLK
AF14	I/O	QCLKB
AF15	NC*	I/O
AF16	NC*	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	NC*	I/O
AF21	NC*	I/O
AF22	NC*	I/O
AF23	NC*	I/O
AF24	NC*	I/O
AF25	NC*	NC
AF26	NC*	NC
B1	NC*	NC
B2	NC*	NC
B3	NC*	I/O
B4	NC*	I/O
B5	NC*	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
B10	I/O	I/O
B11	NC*	I/O
B12	NC*	I/O
B13	V _{CCI}	V _{CCI}
B14	CLKA	CLKA
B15	NC*	I/O
B16	NC*	I/O
B17	I/O	I/O
B18	V _{CCI}	V _{CCI}
B19	I/O	I/O
B20	I/O	I/O
B21	NC*	I/O
B22	NC*	I/O
B23	NC*	I/O
B24	NC*	I/O
B25	I/O	I/O
B26	NC*	NC
C1	NC*	I/O
C2	NC*	I/O
C3	NC*	I/O
C4	NC*	I/O
C5	I/O	I/O
C6	V _{CCI}	V _{CCI}
C7	I/O	I/O
C8	I/O	I/O
C9	V _{CCI}	V _{CCI}
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	PRA, I/O	PRA, I/O
C14	I/O	I/O
C15	I/O	QCLKD
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC *	NC
K25	NC *	I/O
K26	NC *	I/O
L1	NC *	I/O
L2	NC *	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC *	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC *	I/O
M26	NC *	I/O
N1	I/O	I/O
N2	V _{CCI}	V _{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V _{CCA}	V _{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC *	NC
P1	NC *	I/O
P2	NC *	I/O
P3	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
P4	I/O	I/O
P5	V _{CCA}	V _{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V _{CCI}	V _{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC *	I/O
R2	NC *	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	NC *	I/O
R26	NC *	I/O
T1	NC *	I/O
T2	NC *	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC *	I/O
T26	NC *	I/O
U1	I/O	I/O
U2	V _{CCI}	V _{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V _{CCI}	V _{CCI}
U26	I/O	I/O
V1	NC *	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
V2	NC *	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V _{CCA}	V _{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC *	I/O
V26	NC *	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V _{CCA}	V _{CCA}
W24	I/O	I/O
W25	NC *	I/O
W26	NC *	I/O
Y1	NC *	I/O
Y2	NC *	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC *	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V _{CCI}	V _{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.