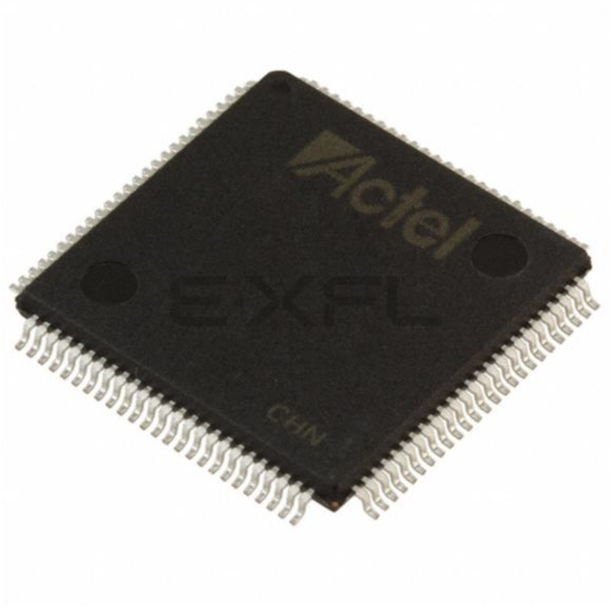

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-1tq100m

General Description

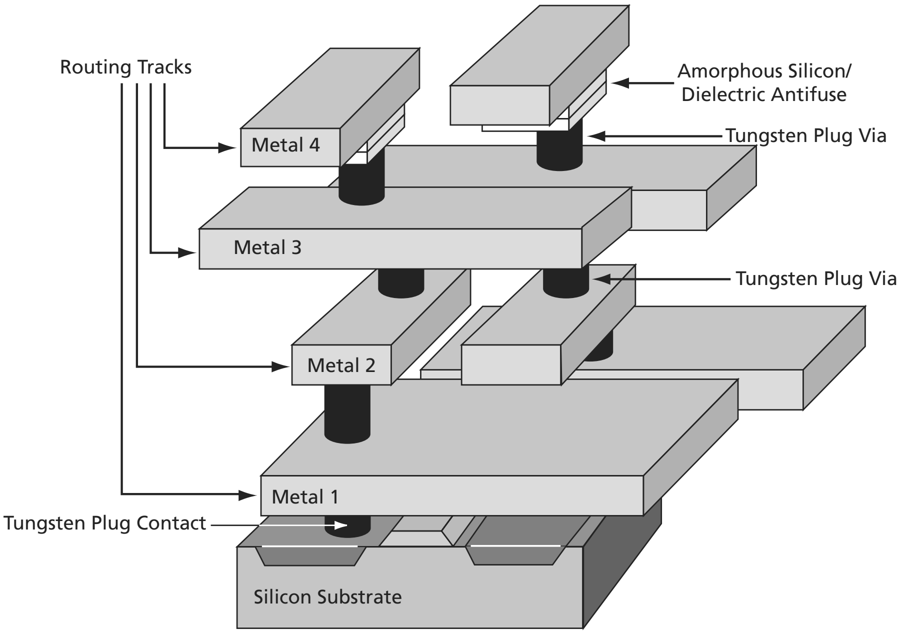
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 µm / 0.25 µm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: *The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.*

Figure 1-1 • **SX-A Family Interconnect Elements**

Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

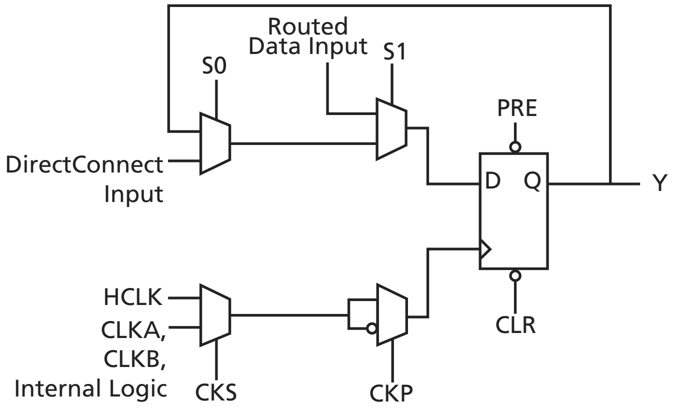


Figure 1-2 • **R-Cell**

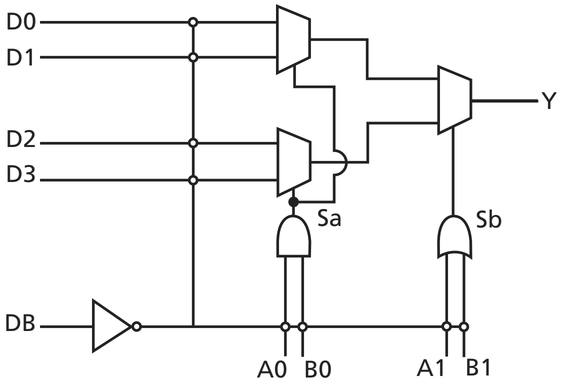


Figure 1-3 • **C-Cell**

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • **Device Configuration Options for Probe Capability (TRST Pin Reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	Low	No	User I/O[3]	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O[3]	User I/O[3]
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

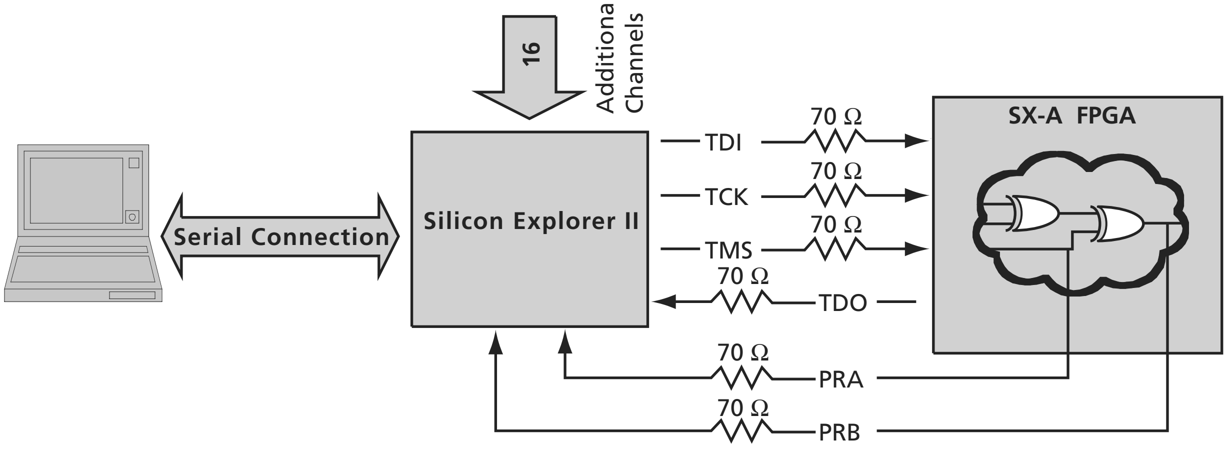


Figure 1-13 • **Probe Setup**

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices
http://www.actel.com/documents/GlobalClk_AN.pdf
Using A54SX72A and RT54SX72S Quadrant Clocks
http://www.actel.com/documents/QCLK_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.actel.com/documents/Antifuse_Security_AN.pdf
Actel eX, SX-A, and RTSX-S I/Os
http://www.actel.com/documents/AntifuseIO_AN.pdf
Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications
http://www.actel.com/documents/HotSwapColdSparing_AN.pdf
Programming Antifuse Devices
http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs
http://www.actel.com/documents/HRSXA_DS.pdf
SX-A Automotive Family FPGAs
http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide
http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Electrical Specifications

Table 2-5 • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	**Max.**	**Min.**	**Max.**	
V_{OH}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	0.9 V_{CCI}		0.9 V_{CCI}		V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –8 mA)	2.4		2.4		V
V_{OL}	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{CCI} = Minimum $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12 mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0	5.75	2.0	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Table 2-6 • **2.5 V LVCMOS2 Electrical Specifications**

Symbol	Parameter		Commercial		Industrial		Units
			Min.	**Max.**	**Min.**	**Max.**	
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –100 µA)	2.1		2.1		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = –1 mA)	2.0		2.0		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} =–-2 mA)	1.7		1.7		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 100 µA)		0.2		0.2	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1 mA)		0.4		0.4	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \leq V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \geq V_{VOH(min)}$		1.7	5.75	1.7	5.75	V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–10	10	–10	10	µA
I_{OZ}	Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

Note: **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

Where:

C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of CLKA/B in pF
C_{EQHV} = Variable capacitance of HCLK in pF
C_{EQHF} = Fixed capacitance of HCLK in pF
C_{L} = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average CLKA rate in MHz
f_{q2} = Average CLKB rate in MHz
f_{s1} = Average HCLK rate in MHz
m = Number of logic modules switching at fm
n = Number of input buffers switching at fn
p = Number of output buffers switching at fp
q_1 = Number of clock loads on CLKA
q_2 = Number of clock loads on CLKB
r_1 = Fixed capacitance due to CLKA
r_2 = Fixed capacitance due to CLKB
s_1 = Number of clock loads on HCLK
x = Number of I/Os at logic low
y = Number of I/Os at logic high

Table 2-11 • **CEQ Values for SX-A Devices**

	A54SX08A	**A54SX16A**	**A54SX32A**	**A54SX72A**
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

θ_{JA} = 17.1°C/W is taken from Table 2-12 on page 2-11

T_A = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°\text{C} - 125°\text{C}}{17.1°\text{C/W}} = 1.46\ \text{W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

T_J = 110°C

T_A = 70°C

From the datasheet:

θ_{JA} = 18.0°C/W

θ_{JC} = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°\text{C} - 70°\text{C}}{18.0°\text{C/W}} = 2.22\ \text{W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°\text{C} - 70°\text{C}}{3.00\ \text{W}} = 13.33°\text{C/W}$$

EQ 2-13

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

θ_{CS} = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
θ_{SA} = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 2-13 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.25 V)**

V_{CCA}	Junction Temperature (T_J)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Table 2-18 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)

		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V LVCMOS Output Module Timing[1,2]										
t_{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[3]	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-24 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-37 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed* Min.	–3 Speed* Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-37 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	**Description**	**–3 Speed***		**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		**Units**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: **All –3 speed grades have been discontinued.*

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V_{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

100-Pin TQFP

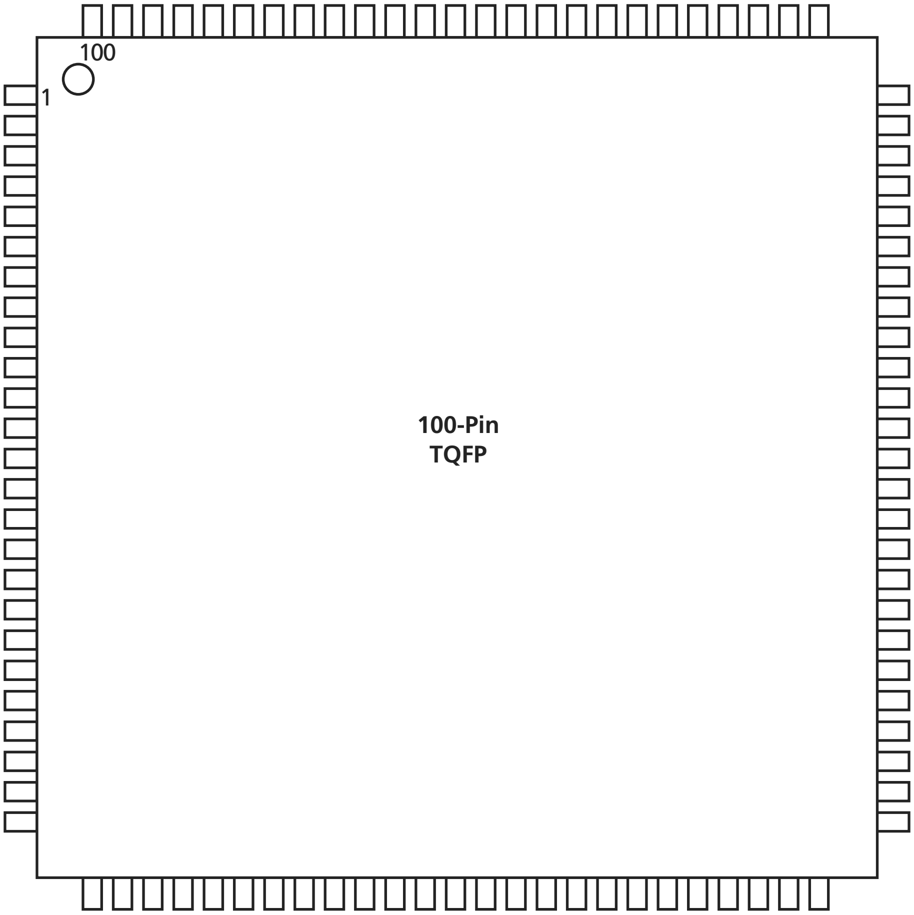


Figure 3-2 • **100-Pin TQFP**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

329-Pin PBGA

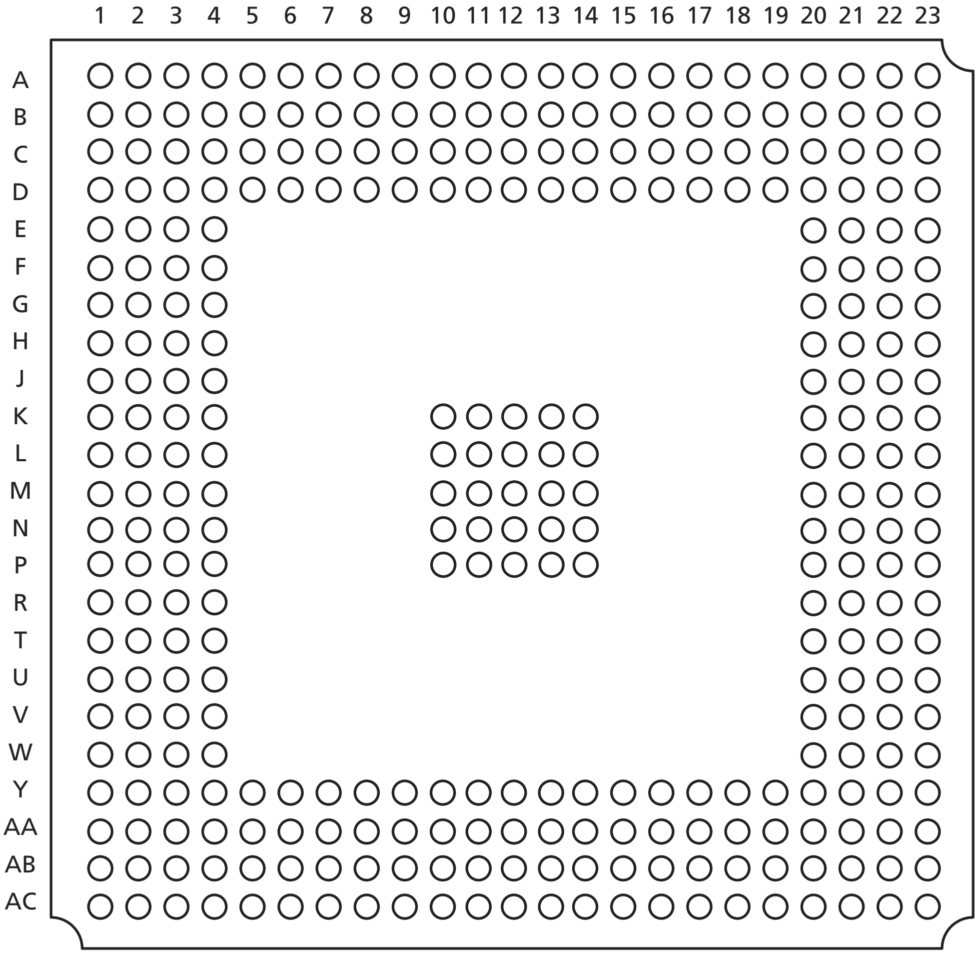


Figure 3-5 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA	
Pin Number	**A54SX32A Function**
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O

144-Pin FBGA

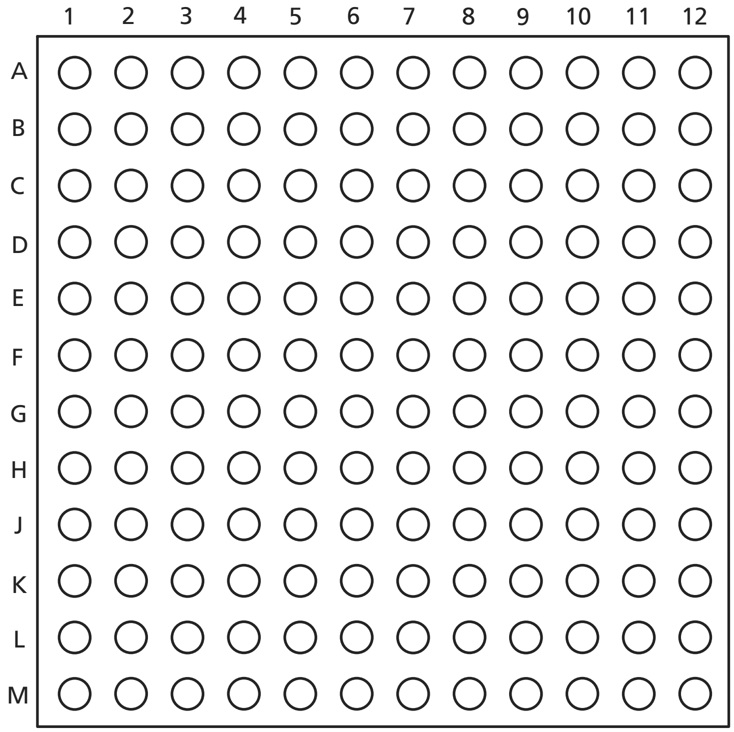


Figure 3-6 • **144-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.