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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 81 |
| Number of Gates | 24000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TC) |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-1tqg100m |

## Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

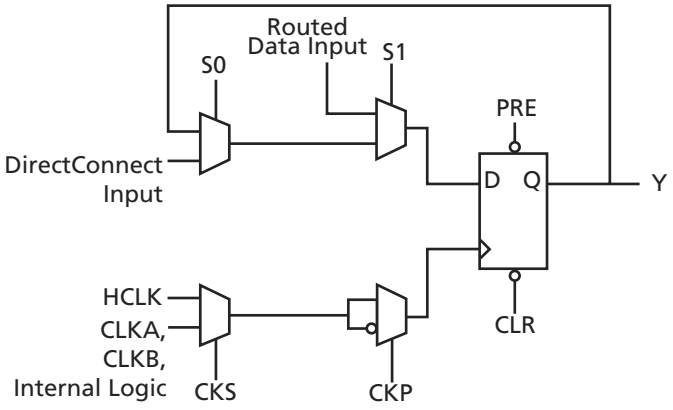


*Figure 1-2* • **R-Cell**

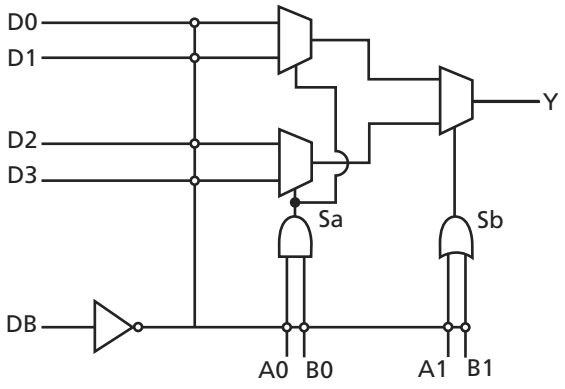


*Figure 1-3* • **C-Cell**

# Pin Description

**CLKA/B, I/O Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

**QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

**GND Ground**

Low supply voltage.

**HCLK Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

**I/O Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

**NC No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

**PRA/B, I/O Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK, I/O Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI, I/O Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO, I/O Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

**TMS Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**TRST, I/O Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

**$V_{CCI}$ Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All $V_{CCI}$ power pins in the device should be connected.

**$V_{CCA}$ Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All $V_{CCA}$ power pins in the device should be connected.

# Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

## Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

## Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

## Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

# Temperature and Voltage Derating Factors

*Table 2-13* • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, $T_J$ = 70°C, $V_{CCA}$ = 2.25 V)**

| | **Junction Temperature ($T_J$)** | | | | | | |
|---|---|---|---|---|---|---|---|
| **$V_{CCA}$** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 2.250 V | 0.79 | 0.80 | 0.87 | 0.89 | 1.00 | 1.04 | 1.14 |
| 2.500 V | 0.74 | 0.75 | 0.82 | 0.83 | 0.94 | 0.97 | 1.07 |
| 2.750 V | 0.68 | 0.69 | 0.75 | 0.77 | 0.87 | 0.90 | 0.99 |

# Timing Characteristics

*Table 2-14* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |

***Notes:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-17* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.5 | | 2.3 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 1.0 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-18* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.3 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **2.5 V LVCMOS Output Module Timing[1,2]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 13.3 | | 15.1 | | 17.7 | | 24.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.9 | | 4.4 | | 5.2 | | 7.2 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

*Table 2-21* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.6 | | 1.9 | | 2.7 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-26* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **3.3 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 9.5 | | 10.9 | | 12.4 | | 14.6 | | 20.4 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-28* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[2]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.8 | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$ , $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$ , or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-30* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.3 | | 2.7 | | 3.1 | | 3.6 | | 5 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-37* • **A54SX72A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{QCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.5 | ns |
| $t_{QCHKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| $t_{QPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{QPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{QCKSW}$ | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{QCKSW}$ | Maximum Skew (50% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{QCKSW}$ | Maximum Skew (100% Load) | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-40* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **3.3 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 10.3 | | 11.9 | | 13.5 | | 15.8 | | 22.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-41* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **5 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 7.4 | | 8.5 | | 9.7 | | 11.4 | | 15.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | NC | NC | NC |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | NC | NC | NC |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| A1 | GND |
| A2 | GND |
| A3 | $V_{CCI}$ |
| A4 | NC |
| A5 | I/O |
| A6 | I/O |
| A7 | $V_{CCI}$ |
| A8 | NC |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| A13 | CLKB |
| A14 | I/O |
| A15 | I/O |
| A16 | I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | I/O |
| A20 | I/O |
| A21 | NC |
| A22 | $V_{CCI}$ |
| A23 | GND |
| AA1 | $V_{CCI}$ |
| AA2 | I/O |
| AA3 | GND |
| AA4 | I/O |
| AA5 | I/O |
| AA6 | I/O |
| AA7 | I/O |
| AA8 | I/O |
| AA9 | I/O |
| AA10 | I/O |
| AA11 | I/O |
| AA12 | I/O |
| AA13 | I/O |
| AA14 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| AA15 | I/O |
| AA16 | I/O |
| AA17 | I/O |
| AA18 | I/O |
| AA19 | I/O |
| AA20 | TDO, I/O |
| AA21 | $V_{CCI}$ |
| AA22 | I/O |
| AA23 | $V_{CCI}$ |
| AB1 | I/O |
| AB2 | GND |
| AB3 | I/O |
| AB4 | I/O |
| AB5 | I/O |
| AB6 | I/O |
| AB7 | I/O |
| AB8 | I/O |
| AB9 | I/O |
| AB10 | I/O |
| AB11 | PRB, I/O |
| AB12 | I/O |
| AB13 | HCLK |
| AB14 | I/O |
| AB15 | I/O |
| AB16 | I/O |
| AB17 | I/O |
| AB18 | I/O |
| AB19 | I/O |
| AB20 | I/O |
| AB21 | I/O |
| AB22 | GND |
| AB23 | I/O |
| AC1 | GND |
| AC2 | $V_{CCI}$ |
| AC3 | NC |
| AC4 | I/O |
| AC5 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| AC6 | I/O |
| AC7 | I/O |
| AC8 | I/O |
| AC9 | $V_{CCI}$ |
| AC10 | I/O |
| AC11 | I/O |
| AC12 | I/O |
| AC13 | I/O |
| AC14 | I/O |
| AC15 | NC |
| AC16 | I/O |
| AC17 | I/O |
| AC18 | I/O |
| AC19 | I/O |
| AC20 | I/O |
| AC21 | NC |
| AC22 | $V_{CCI}$ |
| AC23 | GND |
| B1 | $V_{CCI}$ |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | I/O |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | I/O |
| B12 | PRA, I/O |
| B13 | CLKA |
| B14 | I/O |
| B15 | I/O |
| B16 | I/O |
| B17 | I/O |
| B18 | I/O |
| B19 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| B20 | I/O |
| B21 | I/O |
| B22 | GND |
| B23 | $V_{CCI}$ |
| C1 | NC |
| C2 | TDI, I/O |
| C3 | GND |
| C4 | I/O |
| C5 | I/O |
| C6 | I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |
| C13 | I/O |
| C14 | I/O |
| C15 | I/O |
| C16 | I/O |
| C17 | I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| C21 | $V_{CCI}$ |
| C22 | GND |
| C23 | NC |
| D1 | I/O |
| D2 | I/O |
| D3 | I/O |
| D4 | TCK, I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| D11 | $V_{CCA}$ |
| D12 | NC |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | $V_{CCI}$ |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | $V_{CCA}$ |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | NC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| L14 | GND |
| L20 | NC |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | $V_{CCA}$ |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | $V_{CCA}$ |
| M21 | I/O |
| M22 | I/O |
| M23 | $V_{CCI}$ |
| N1 | I/O |
| N2 | TRST, I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |
| T22 | I/O |
| T23 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | $V_{CCA}$ |
| U4 | I/O |
| U20 | I/O |
| U21 | $V_{CCA}$ |
| U22 | I/O |
| U23 | I/O |
| V1 | $V_{CCI}$ |
| V2 | I/O |
| V3 | I/O |
| V4 | I/O |
| V20 | I/O |
| V21 | I/O |

# 256-Pin FBGA

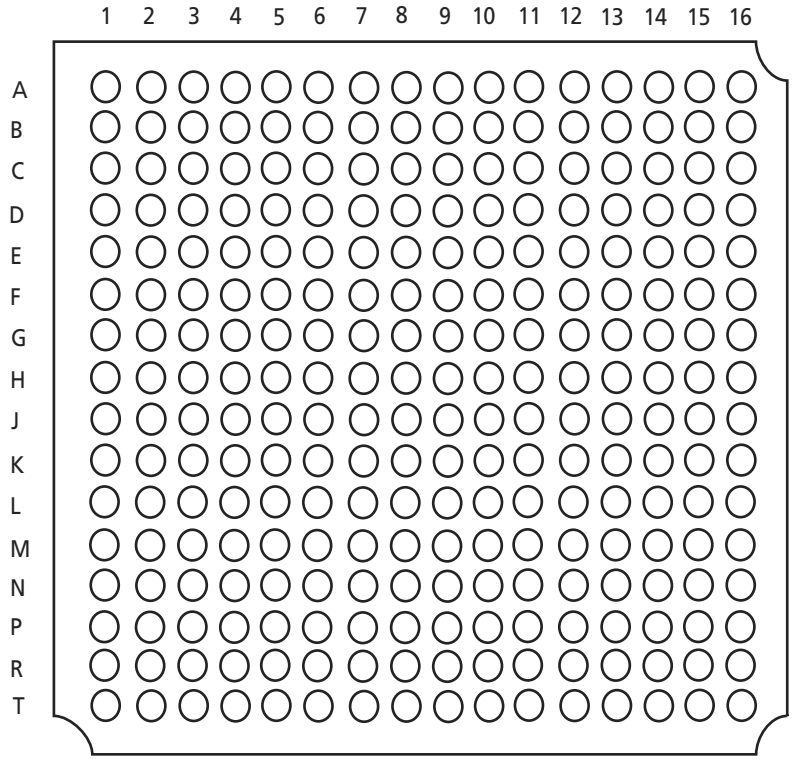


*Figure 3-7* • **256-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| K5 | I/O | I/O | I/O |
| K6 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K7 | GND | GND | GND |
| K8 | GND | GND | GND |
| K9 | GND | GND | GND |
| K10 | GND | GND | GND |
| K11 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| K12 | I/O | I/O | I/O |
| K13 | I/O | I/O | I/O |
| K14 | I/O | I/O | I/O |
| K15 | NC | I/O | I/O |
| K16 | I/O | I/O | I/O |
| L1 | I/O | I/O | I/O |
| L2 | I/O | I/O | I/O |
| L3 | I/O | I/O | I/O |
| L4 | I/O | I/O | I/O |
| L5 | I/O | I/O | I/O |
| L6 | I/O | I/O | I/O |
| L7 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L9 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| L11 | I/O | I/O | I/O |
| L12 | I/O | I/O | I/O |
| L13 | I/O | I/O | I/O |
| L14 | I/O | I/O | I/O |
| L15 | I/O | I/O | I/O |
| L16 | NC | I/O | I/O |
| M1 | I/O | I/O | I/O |
| M2 | I/O | I/O | I/O |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | I/O |
| M5 | I/O | I/O | I/O |
| M6 | I/O | I/O | I/O |
| M7 | I/O | I/O | QCLKA |
| M8 | PRB, I/O | PRB, I/O | PRB, I/O |
| M9 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| M10 | I/O | I/O | I/O |
| M11 | I/O | I/O | I/O |
| M12 | NC | I/O | I/O |
| M13 | I/O | I/O | I/O |
| M14 | NC | I/O | I/O |
| M15 | I/O | I/O | I/O |
| M16 | I/O | I/O | I/O |
| N1 | I/O | I/O | I/O |
| N2 | I/O | I/O | I/O |
| N3 | I/O | I/O | I/O |
| N4 | I/O | I/O | I/O |
| N5 | I/O | I/O | I/O |
| N6 | I/O | I/O | I/O |
| N7 | I/O | I/O | I/O |
| N8 | I/O | I/O | I/O |
| N9 | I/O | I/O | I/O |
| N10 | I/O | I/O | I/O |
| N11 | I/O | I/O | I/O |
| N12 | I/O | I/O | I/O |
| N13 | I/O | I/O | I/O |
| N14 | I/O | I/O | I/O |
| N15 | I/O | I/O | I/O |
| N16 | I/O | I/O | I/O |
| P1 | I/O | I/O | I/O |
| P2 | GND | GND | GND |
| P3 | I/O | I/O | I/O |
| P4 | I/O | I/O | I/O |
| P5 | NC | I/O | I/O |
| P6 | I/O | I/O | I/O |
| P7 | I/O | I/O | I/O |
| P8 | I/O | I/O | I/O |
| P9 | I/O | I/O | I/O |
| P10 | NC | I/O | I/O |
| P11 | I/O | I/O | I/O |
| P12 | I/O | I/O | I/O |
| P13 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| P14 | I/O | I/O | I/O |

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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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## Unmarked (production)

This datasheet version contains information that is considered to be final.

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