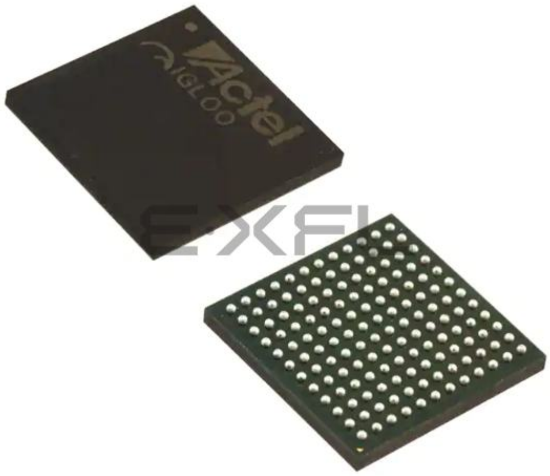
# Microsemi Corporation - A54SX16A-2FGG144I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 111 |
| Number of Gates | 24000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx16a-2fgg144i |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# Ordering Information

A54SX16A 2 PQ G 208 ___

Application (Temperature Range)
Blank = Commercial (0 to +70°)
I = Industrial (-40 to +85°C)
A = Automotive (-40 to +125°C)
M = Military (-55 to +125°C)
B = MIL-STD-883 Class B

Package Lead Count

Package Type
BG = 1.27 mm Plastic Ball Grid Array
FG = 1.0 mm Fine Pitch Ball Grid Array
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
CQ = Ceramic Quad Flat Pack[1]

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard[2]
–F = Approximately 40% Slower than Standard

Part Number
A54SX08A = 12,000 System Gates
A54SX16A = 24,000 System Gates
A54SX32A = 48,000 System Gates
A54SX72A = 108,000 System Gates

***Notes:***

1. *For more information about the CQFP package options, refer to the* HiRel SX-A datasheet*.*
2. *All –3 speed grades have been discontinued.*

# Device Resources

| | User I/Os (Including Clock Buffers) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Device** | **208-Pin PQFP** | **100-Pin TQFP** | **144-Pin TQFP** | **176-Pin TQFP** | **329-Pin PBGA** | **144-Pin FBGA** | **256-Pin FBGA** | **484-Pin FBGA** |
| A54SX08A | 130 | 81 | 113 | – | – | 111 | – | – |
| A54SX16A | 175 | 81 | 113 | – | – | 111 | 180 | – |
| A54SX32A | 174 | 81 | 113 | 147 | 249 | 111 | 203 | 249 |
| A54SX72A | 171 | – | – | – | – | – | 203 | 360 |

***Notes:*** *Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array*

## Temperature Grade Offering

| **Package** | **A54SX08A** | **A54SX16A** | **A54SX32A** | **A54SX72A** |
|---|---|---|---|---|
| PQ208 | C,I,A,M | C,I,A,M | C,I,A,M | C,I,A,M |
| TQ100 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ176 | | | C,I,M | |
| BG329 | | | C,I,M | |
| FG144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| FG256 | | C,I,A,M | C,I,A,M | C,I,A,M |
| FG484 | | | C,I,M | C,I,A,M |
| CQ208 | | | C,M,B | C,M,B |
| CQ256 | | | C,M,B | C,M,B |

***Notes:***

1. *C = Commercial*
2. *I = Industrial*
3. *A = Automotive*
4. *M = Military*
5. *B = MIL-STD-883 Class B*
6. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
7. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

## Speed Grade and Temperature Grade Matrix

| | **F** | **Std** | **–1** | **–2** | **–3** |
|---|---|---|---|---|---|
| Commercial | ✓ | ✓ | ✓ | ✓ | Discontinued |
| Industrial | | ✓ | ✓ | ✓ | Discontinued |
| Automotive | | ✓ | | | |
| Military | | ✓ | ✓ | | |
| MIL-STD-883B | | ✓ | ✓ | | |

***Notes:***

1. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
2. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Contact your Actel Sales representative for more information on availability.

# General Description

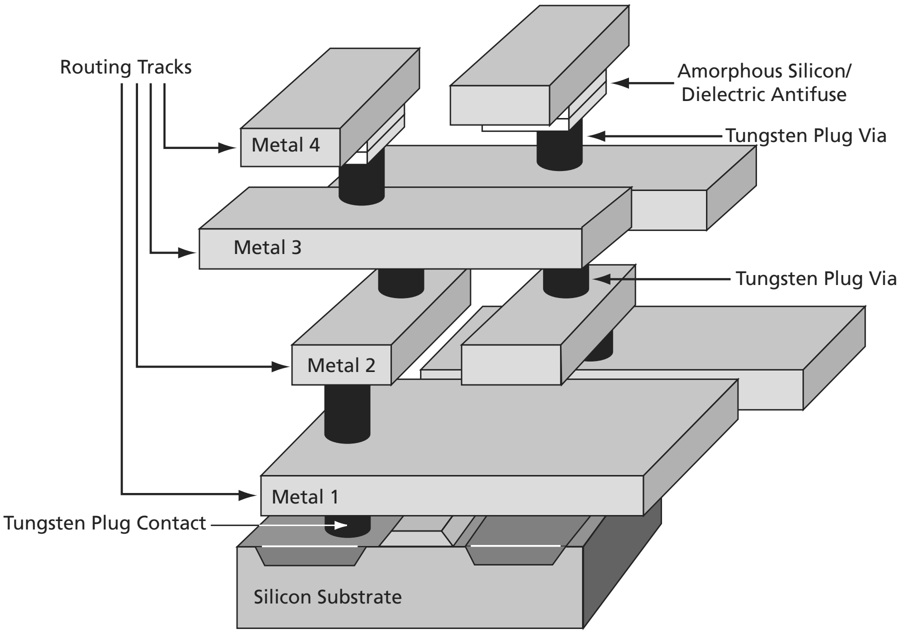
## Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

## SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



***Note:*** *The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.*

*Figure 1-1* • **SX-A Family Interconnect Elements**

# Detailed Specifications

## Operating Conditions

*Table 2-1* • **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CCI}$ | DC Supply Voltage for I/Os | –0.3 to +6.0 | V |
| $V_{CCA}$ | DC Supply Voltage for Arrays | –0.3 to +3.0 | V |
| $V_I$ | Input Voltage | –0.5 to +5.75 | V |
| $V_O$ | Output Voltage | –0.5 to + $V_{CCI}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".*

*Table 2-2* • **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Units |
|---|---|---|---|
| Temperature Range | 0 to +70 | –40 to +85 | °C |
| 2.5 V Power Supply Range ($V_{CCA}$ and $V_{CCI}$) | 2.25 to 2.75 | 2.25 to 2.75 | V |
| 3.3 V Power Supply Range ($V_{CCI}$) | 3.0 to 3.6 | 3.0 to 3.6 | V |
| 5 V Power Supply Range ($V_{CCI}$) | 4.75 to 5.25 | 4.75 to 5.25 | V |

## Typical SX-A Standby Current

*Table 2-3* • **Typical Standby Current for SX-A at 25°C with $V_{CCA}$ = 2.5 V**

| Product | $V_{CCI}$ = 2.5 V | $V_{CCI}$ = 3.3 V | $V_{CCI}$ = 5 V |
|---|---|---|---|
| A54SX08A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX16A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX32A | 0.9 mA | 1.0 mA | 3.0 mA |
| A54SX72A | 3.6 mA | 3.8 mA | 4.5 mA |

*Table 2-4* • **Supply Voltages**

| $V_{CCA}$ | $V_{CCI}$* | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|
| 2. 5 V | 2.5 V | 5.75 V | 2.7 V |
| 2.5 V | 3.3 V | 5.75 V | 3.6 V |
| 2.5 V | 5 V | 5.75 V | 5.25 V |

**Note:** **3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.*

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

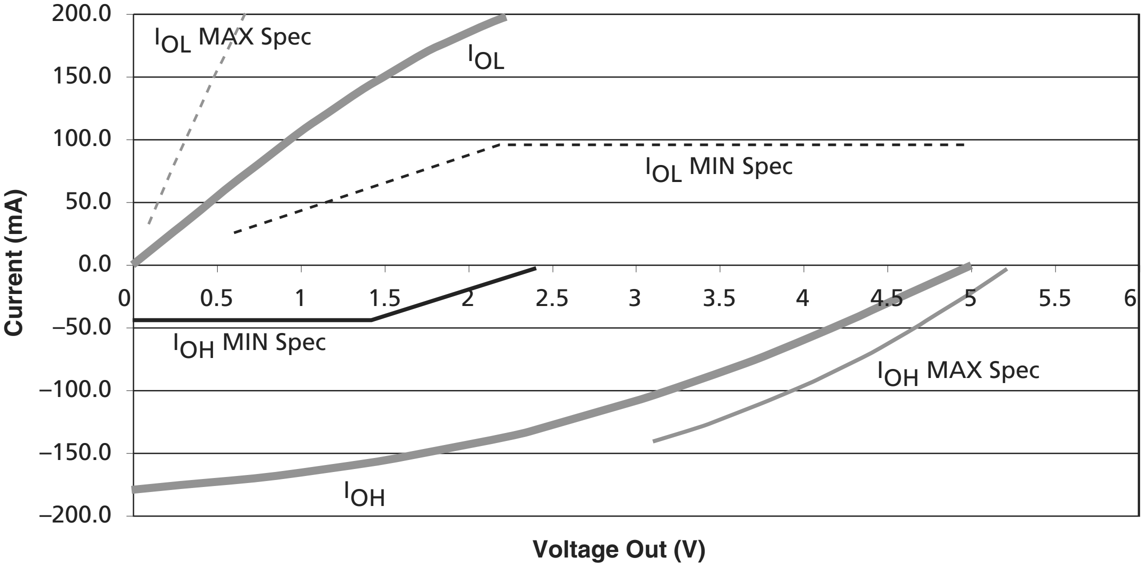


*Figure 2-1* • **5 V PCI V/I Curve for SX-A Family**

$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$
for $V_{CCI} > V_{OUT} > 3.1V$

*EQ 2-1*

$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$
for $0V < V_{OUT} < 0.71V$

*EQ 2-2*

*Table 2-9* • **DC Specifications (3.3 V PCI Operation)**

| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Units** |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 2.25 | 2.75 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 3.0 | 3.6 | V |
| $V_{IH}$ | Input High Voltage | | $0.5V_{CCI}$ | $V_{CCI} + 0.5$ | V |
| $V_{IL}$ | Input Low Voltage | | –0.5 | $0.3V_{CCI}$ | V |
| $I_{IPU}$ | Input Pull-up Voltage[1] | | $0.7V_{CCI}$ | – | V |
| $I_{IL}$ | Input Leakage Current[2] | $0 < V_{IN} < V_{CCI}$ | –10 | +10 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT} = -500$ µA | $0.9V_{CCI}$ | – | V |
| $V_{OL}$ | Output Low Voltage | $I_{OUT} = 1{,}500$ µA | | $0.1V_{CCI}$ | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | – | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |

***Notes:***

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

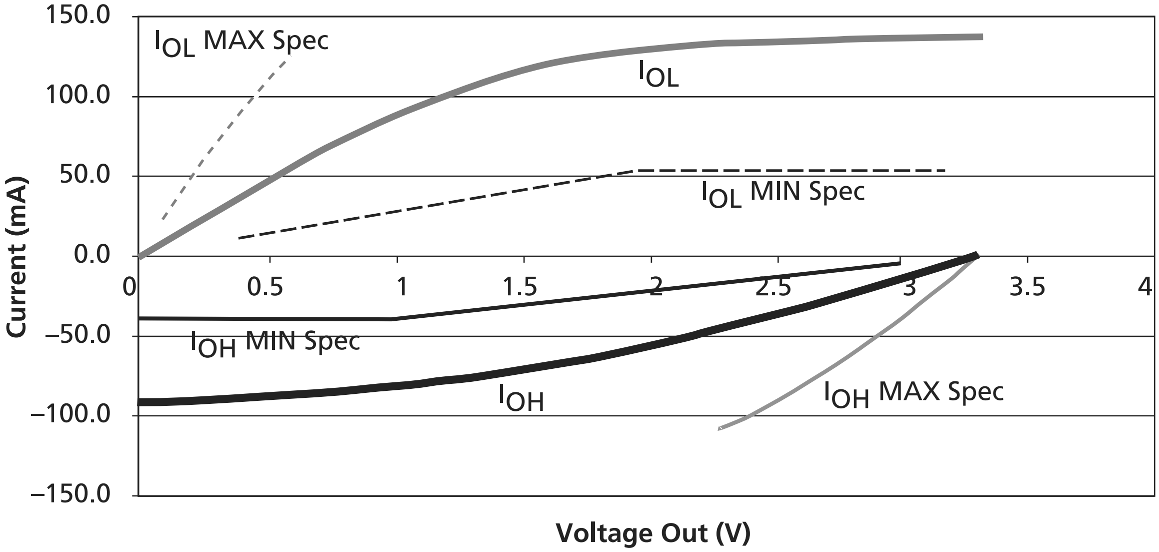


*Figure 2-2* • **3.3 V PCI V/I Curve for SX-A Family**

$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$

for $0.7\ V_{CCI} < V_{OUT} < V_{CCI}$

*EQ 2-3*

$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$

for $0V < V_{OUT} < 0.18\ V_{CCI}$

*EQ 2-4*

# Output Buffer Delays

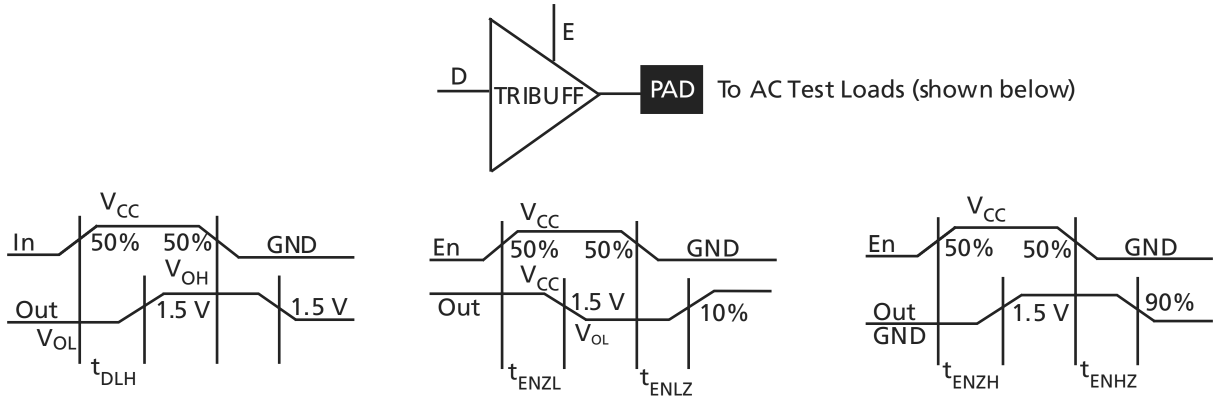


*Figure 2-4* • **Output Buffer Delays**

# AC Test Loads

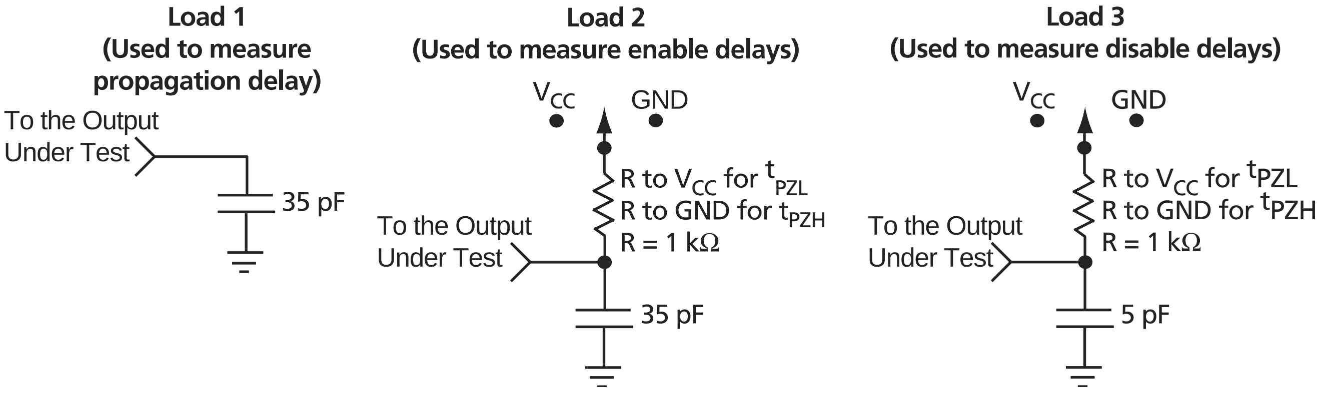


*Figure 2-5* • **AC Test Loads**

*Table 2-15* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-20* • **A54SX08A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **5 V PCI Output Module Timing[1]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$[2] | Delta Low to High | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[2] | Delta High to Low | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[3]** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.2 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$ | Delta High to Low—low slew | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *Delays based on 50 pF loading.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
3. *Delays based on 35 pF loading.*

*Table 2-23* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-25* • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| | | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **2.5 V LVCMOS Output Module Timing [2, 3]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 11.6 | | 13.4 | | 15.2 | | 17.9 | | 25.0 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{ENZLS}$ | Data-to-Pad, Z to L—low slew | | 11.8 | | 13.7 | | 15.5 | | 18.2 | | 25.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.4 | | 3.9 | | 4.5 | | 5.2 | | 7.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.1 | | 2.5 | | 2.8 | | 3.3 | | 4.7 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $d_{TLH}$[4] | Delta Low to High | | 0.031 | | 0.037 | | 0.043 | | 0.051 | | 0.071 | ns/pF |
| $d_{THL}$[4] | Delta High to Low | | 0.017 | | 0.017 | | 0.023 | | 0.023 | | 0.037 | ns/pF |
| $d_{THLS}$[4] | Delta High to Low—low slew | | 0.057 | | 0.06 | | 0.071 | | 0.086 | | 0.117 | ns/pF |

***Note:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

*Table 2-28* • **A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions, $V_{CCA} = 2.25$ V, $V_{CCI} = 3.0$ V, $T_J = 70°C$)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays**[2] | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.8 | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays**[3] | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.5 | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use* $t_{PD} + t_{RD1} + t_{PDn}$ , $t_{RCO} + t_{RD1} + t_{PDn}$ , *or* $t_{PD1} + t_{RD1} + t_{SUD}$ , *whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-28* • **A54SX32A Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{INYH}$ | Input Data Pad to Y High 5 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V PCI | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 5 V TTL | | 0.9 | | 1.1 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 5 V TTL | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Input Module Predicted Routing Delays[3]** | | | | | | | | | | | | |
| $t_{IRD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{IRD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IRD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{IRD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{IRD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{IRD12}$ | FO = 12 Routing Delay | | 1.7 | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use* $t_{PD} + t_{RD1} + t_{PDn}$ *,* $t_{RCO} + t_{RD1} + t_{PDn}$ *, or* $t_{PD1} + t_{RD1} + t_{SUD}$ *, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-35* • **A54SX72A Timing Characteristics**
**(Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | **–3 Speed**[1] | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **–F Speed** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **C-Cell Propagation Delays**[2] | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.0 | ns |
| **Predicted Routing Delays**[3] | | | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 1 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.5 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.7 | | 0.9 | | 1 | | 1.1 | | 1.5 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.2 | | 1.5 | | 1.7 | | 2.1 | | 2.9 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 1.7 | | 2.2 | | 2.5 | | 3 | | 4.2 | ns |
| **R-Cell Timing** | | | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Minimum Pulse Width | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 0.8 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$ , $t_{RCO} + t_{RD1} + t_{PDn}$ , or $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-40* • **A54SX72A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| **Parameter** | **Description** | **–3 Speed[1]** | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **–F Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| **3.3 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 10.3 | | 11.9 | | 13.5 | | 15.8 | | 22.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.2 | | 3.7 | | 4.2 | | 5.0 | | 6.9 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.2 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] =* $(0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   *where* $C_{load}$ *is the load capacitance driven by the I/O in pF*
   $d_{T[LH|HL|HLS]}$ *is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

# Package Pin Assignments

## 208-Pin PQFP

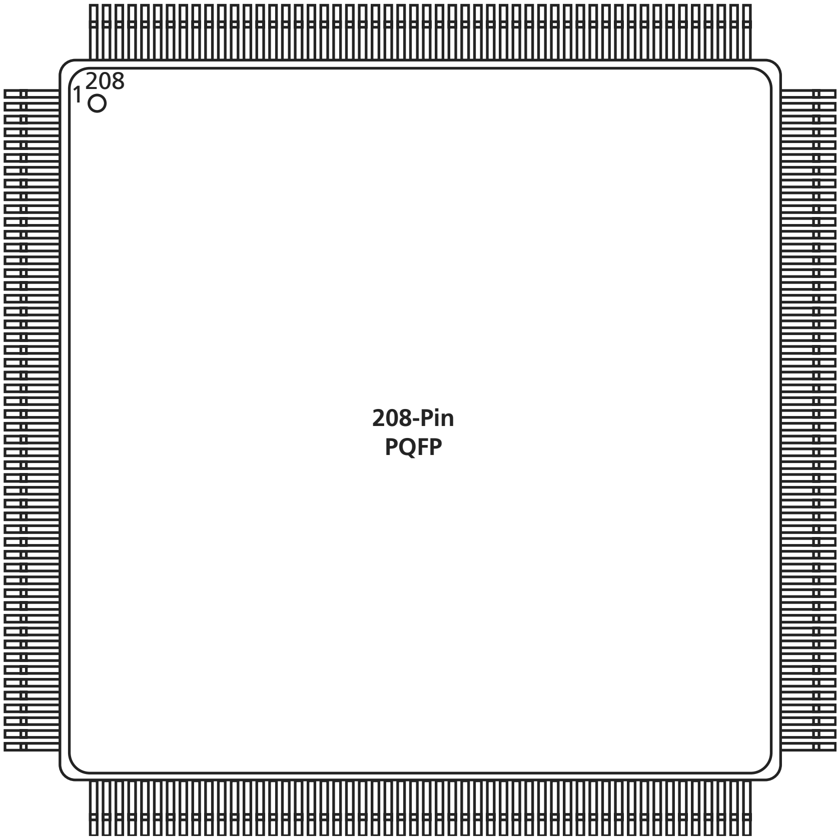


*Figure 3-1* • **208-Pin PQFP (Top View)**

### Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 1 | GND | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O | I/O |
| 4 | NC | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O | I/O |
| 6 | NC | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O | I/O |
| 10 | I/O | I/O | I/O | I/O |
| 11 | TMS | TMS | TMS | TMS |
| 12 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 13 | I/O | I/O | I/O | I/O |
| 14 | NC | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O | I/O |
| 17 | NC | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O | GND |
| 19 | I/O | I/O | I/O | $V_{CCA}$ |
| 20 | NC | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O | I/O |
| 23 | NC | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O | I/O |
| 25 | NC | NC | NC | I/O |
| 26 | GND | GND | GND | GND |
| 27 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 28 | GND | GND | GND | GND |
| 29 | I/O | I/O | I/O | I/O |
| 30 | TRST, I/O | TRST, I/O | TRST, I/O | TRST, I/O |
| 31 | NC | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O | I/O |
| 35 | NC | I/O | I/O | I/O |

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 36 | I/O | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O | I/O |
| 39 | NC | I/O | I/O | I/O |
| 40 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 41 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 42 | I/O | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O | I/O |
| 44 | I/O | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O | I/O |
| 48 | NC | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O | I/O |
| 50 | NC | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O | I/O |
| 52 | GND | GND | GND | GND |
| 53 | I/O | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 61 | NC | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O | I/O |
| 64 | NC | I/O | I/O | I/O |
| 65 | I/O | I/O | NC | I/O |
| 66 | I/O | I/O | I/O | I/O |
| 67 | NC | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O | I/O |
| 70 | NC | I/O | I/O | I/O |

| 100-TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | TMS | TMS | TMS |
| 8 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 9 | GND | GND | GND |
| 10 | I/O | I/O | I/O |
| 11 | I/O | I/O | I/O |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | TRST, I/O | TRST, I/O | TRST, I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | I/O | I/O | I/O |
| 20 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | I/O | I/O | I/O |
| 29 | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O | PRB, I/O |
| 35 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |

| 100-TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 36 | GND | GND | GND |
| 37 | NC | NC | NC |
| 38 | I/O | I/O | I/O |
| 39 | HCLK | HCLK | HCLK |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | TDO, I/O | TDO, I/O | TDO, I/O |
| 50 | I/O | I/O | I/O |
| 51 | GND | GND | GND |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 58 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 59 | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 68 | GND | GND | GND |
| 69 | GND | GND | GND |
| 70 | I/O | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| A1 | GND | GND | GND |
| A2 | TCK, I/O | TCK, I/O | TCK, I/O |
| A3 | I/O | I/O | I/O |
| A4 | I/O | I/O | I/O |
| A5 | I/O | I/O | I/O |
| A6 | I/O | I/O | I/O |
| A7 | I/O | I/O | I/O |
| A8 | I/O | I/O | I/O |
| A9 | CLKB | CLKB | CLKB |
| A10 | I/O | I/O | I/O |
| A11 | I/O | I/O | I/O |
| A12 | NC | I/O | I/O |
| A13 | I/O | I/O | I/O |
| A14 | I/O | I/O | I/O |
| A15 | GND | GND | GND |
| A16 | GND | GND | GND |
| B1 | I/O | I/O | I/O |
| B2 | GND | GND | GND |
| B3 | I/O | I/O | I/O |
| B4 | I/O | I/O | I/O |
| B5 | I/O | I/O | I/O |
| B6 | NC | I/O | I/O |
| B7 | I/O | I/O | I/O |
| B8 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| B9 | I/O | I/O | I/O |
| B10 | I/O | I/O | I/O |
| B11 | NC | I/O | I/O |
| B12 | I/O | I/O | I/O |
| B13 | I/O | I/O | I/O |
| B14 | I/O | I/O | I/O |
| B15 | GND | GND | GND |
| B16 | I/O | I/O | I/O |
| C1 | I/O | I/O | I/O |
| C2 | TDI, I/O | TDI, I/O | TDI, I/O |
| C3 | GND | GND | GND |
| C4 | I/O | I/O | I/O |
| C5 | NC | I/O | I/O |

| 256-Pin FBGA | | | |
|---|---|---|---|
| **Pin Number** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| C6 | I/O | I/O | I/O |
| C7 | I/O | I/O | I/O |
| C8 | I/O | I/O | I/O |
| C9 | CLKA | CLKA | CLKA |
| C10 | I/O | I/O | I/O |
| C11 | I/O | I/O | I/O |
| C12 | I/O | I/O | I/O |
| C13 | I/O | I/O | I/O |
| C14 | I/O | I/O | I/O |
| C15 | I/O | I/O | I/O |
| C16 | I/O | I/O | I/O |
| D1 | I/O | I/O | I/O |
| D2 | I/O | I/O | I/O |
| D3 | I/O | I/O | I/O |
| D4 | I/O | I/O | I/O |
| D5 | I/O | I/O | I/O |
| D6 | I/O | I/O | I/O |
| D7 | I/O | I/O | I/O |
| D8 | PRA, I/O | PRA, I/O | PRA, I/O |
| D9 | I/O | I/O | QCLKD |
| D10 | I/O | I/O | I/O |
| D11 | NC | I/O | I/O |
| D12 | I/O | I/O | I/O |
| D13 | I/O | I/O | I/O |
| D14 | I/O | I/O | I/O |
| D15 | I/O | I/O | I/O |
| D16 | I/O | I/O | I/O |
| E1 | I/O | I/O | I/O |
| E2 | I/O | I/O | I/O |
| E3 | I/O | I/O | I/O |
| E4 | I/O | I/O | I/O |
| E5 | I/O | I/O | I/O |
| E6 | I/O | I/O | I/O |
| E7 | I/O | I/O | QCLKC |
| E8 | I/O | I/O | I/O |
| E9 | I/O | I/O | I/O |
| E10 | I/O | I/O | I/O |