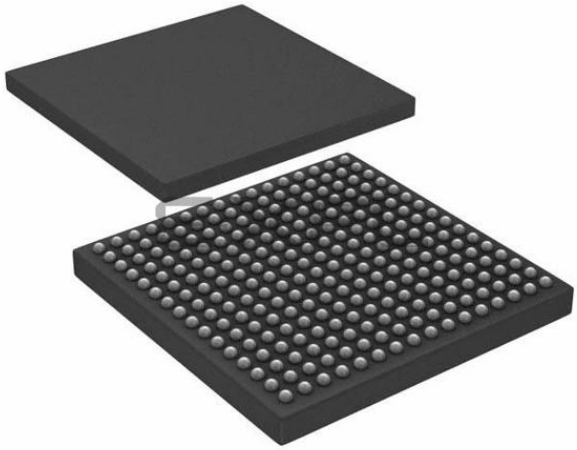
Microsemi Corporation - A54SX16A-FFG256 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	180
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16a-ffg256

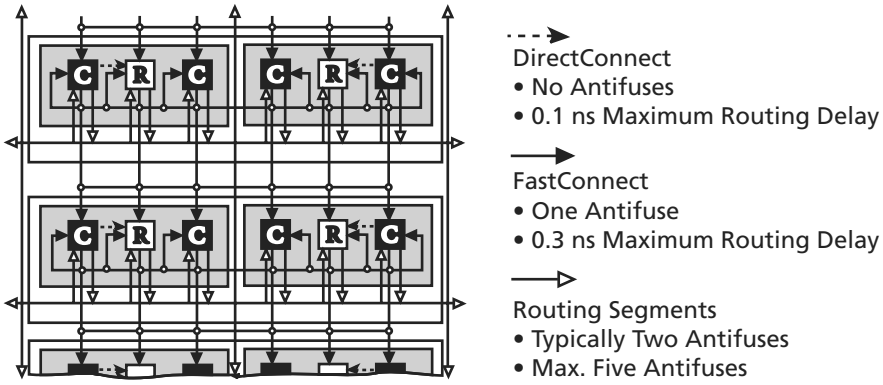


Figure 1-5 • **DirectConnect and FastConnect for Type 1 SuperClusters**

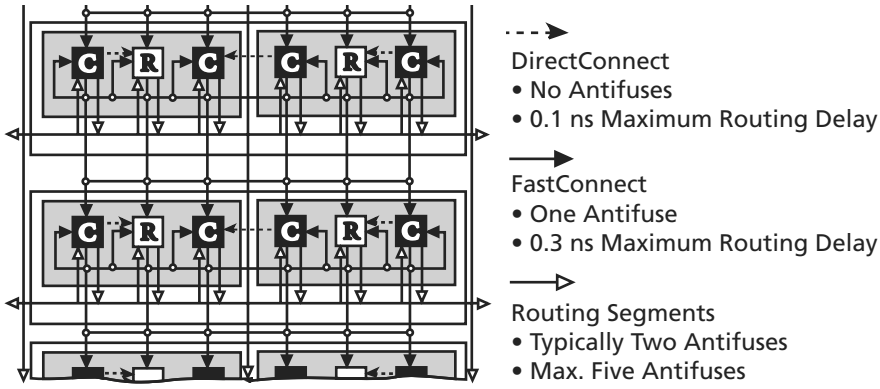


Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selections	• 5 V: PCI, TTL • 3.3 V: PCI, LVTTL • 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	• 5 V: PCI, TTL • 3.3 V: PCI, LVTTL • 2.5 V: LVCMOS2 (commercial only)
Output Buffer	"Hot-Swap" Capability (3.3 V PCI is not hot swappable) • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • **I/O Characteristics for All I/O Configurations**

	Hot Swappable	Slew Rate Control	Power-Up Resistor
TTL, LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down

Table 1-4 • **Power-Up Time at which I/Os Become Active**

Supply Ramp Rate	0.25 V/µs	0.025 V/µs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Figure 1-12 • **Device Selection Wizard**

Table 1-5 • **Reserve Pin Definitions**

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • **Boundary-Scan Pin Configurations and Functions**

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage for I/Os	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage for Arrays	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.75	V
V_O	Output Voltage	–0.5 to + V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
2.5 V Power Supply Range (V_{CCA} and V_{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V_{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V_{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • **Typical Standby Current for SX-A at 25°C with V_{CCA} = 2.5 V**

Product	V_{CCI} = 2.5 V	V_{CCI} = 3.3 V	V_{CCI} = 5 V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • **Supply Voltages**

V_{CCA}	V_{CCI}*	Maximum Input Tolerance	Maximum Output Drive
2. 5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

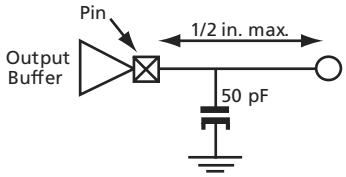
Note: **3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.*

Table 2-8 • **AC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44	–	mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ [3]	–	–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95	–	mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ [1, 3]	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ [3]	–	206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



Timing Characteristics

Table 2-14 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.9		1.1		1.2		1.7	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{RD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.6		0.8		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.7		0.9		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.5		1.8		2.5		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Pulse Width	1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.0		1.2		1.4		1.9	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.6		0.7		1.0	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.3	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.9		1.2	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.1		1.3		1.8	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-18 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing[1,2]										
t_{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[3]	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-24 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-27 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.5		2.8		3.3		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.7		7.7		8.7		10.2		14.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-34 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.1		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.5		2.9		4.1	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.6		7.6		8.6		10.1		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-38 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.3		2.6		3.0		3.5		4.9	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.2		3.6		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.2		3.6		4.1		4.8		6.8	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.2		2.5		3.0		4.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.2		2.5		3.0		4.1	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.4		1.6		1.8		2.1		3.0	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.4		1.7		1.9		2.2		3.1	ns

Note: **All –3 speed grades have been discontinued.*

100-TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin TQFP

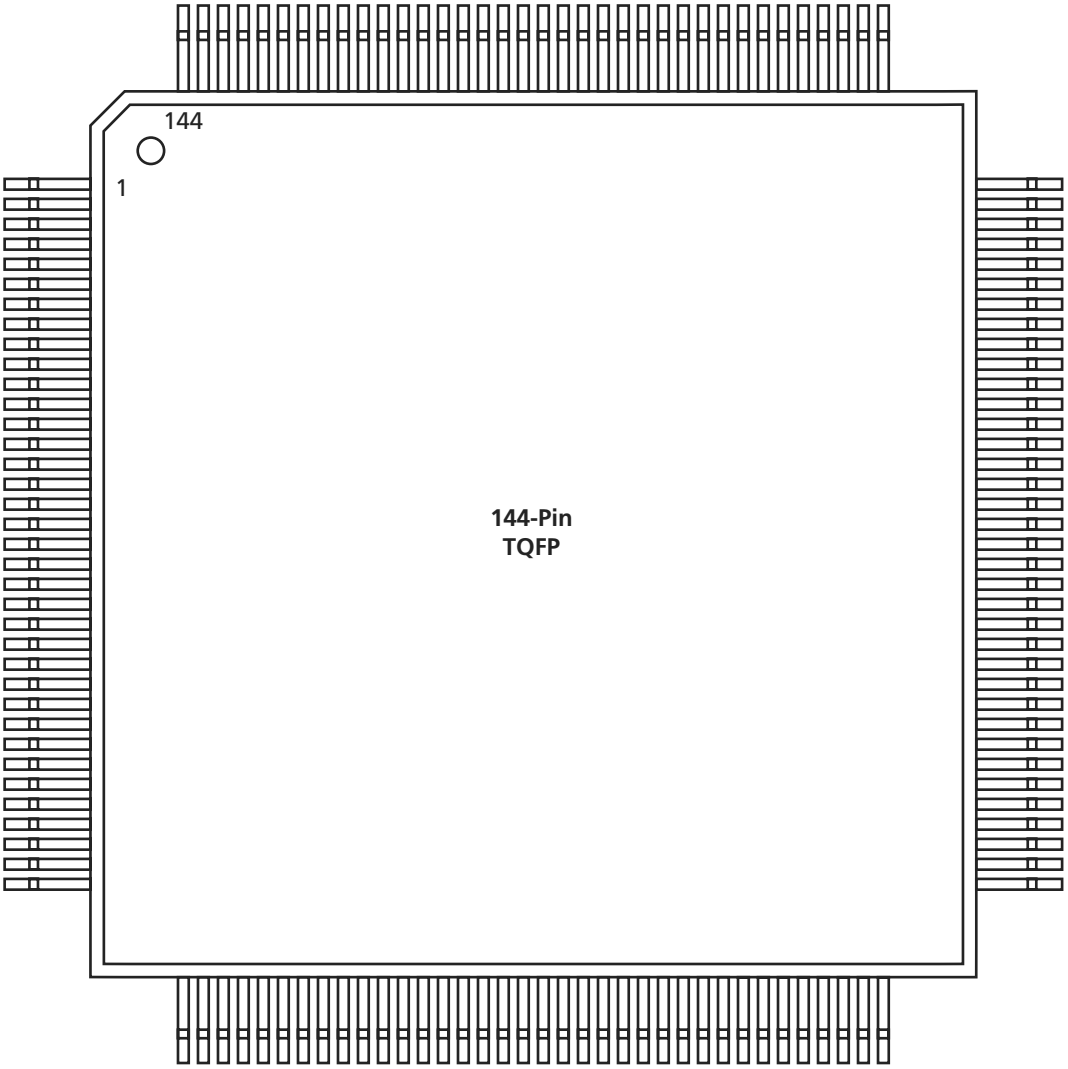


Figure 3-3 • **144-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O

144-Pin FBGA			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V_{CCI}	V_{CCI}	V_{CCI}
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V_{CCA}	V_{CCA}	V_{CCA}
H6	V_{CCA}	V_{CCA}	V_{CCA}
H7	V_{CCI}	V_{CCI}	V_{CCI}
H8	V_{CCI}	V_{CCI}	V_{CCI}
H9	V_{CCA}	V_{CCA}	V_{CCA}
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V_{CCA}	V_{CCA}	V_{CCA}

144-Pin FBGA			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V_{CCA}	V_{CCA}	V_{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V_{CCI}	V_{CCI}	V_{CCI}
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	V_{CCI}	V_{CCI}	V_{CCI}
F10	V_{CCI}	V_{CCI}	V_{CCI}
F11	I/O	I/O	I/O
F12	VCCA	VCCA	VCCA
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V_{CCI}	V_{CCI}	V_{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V_{CCI}	V_{CCI}	V_{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V_{CCA}	V_{CCA}	V_{CCA}

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V_{CCA}	V_{CCA}	V_{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V_{CCI}	V_{CCI}	V_{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V_{CCI}	V_{CCI}	V_{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V_{CCI}	V_{CCI}	V_{CCI}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V_{CCI}	V_{CCI}	V_{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V_{CCA}	V_{CCA}	V_{CCA}

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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