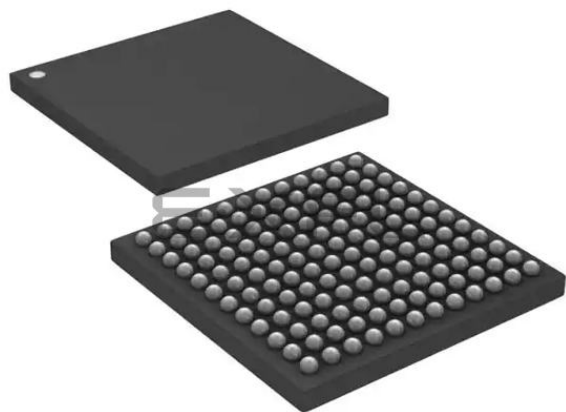




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx16a-fg144m

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Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.



Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CC} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-7 lists the supported instructions with the corresponding IR codes for SX-A devices.

Table 1-8 lists the codes returned after executing the IDCODE instruction for SX-A devices. Note that bit 0 is always '1'. Bits 11-1 are always '02F', which is the Actel manufacturer code.

Table 1-7 • JTAG Instruction Code

Instructions (IR4:IR0)	Binary Code
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HighZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-8 • JTAG Instruction Code

Device	Process	Revision	Bits 31-28	Bits 27-12
A54SX08A	0.22 μ	0	8, 9	40B4, 42B4
		1	A, B	40B4, 42B4
A54SX16A	0.22 μ	0	9	40B8, 42B8
		1	B	40B8, 42B8
	0.25 μ	1	B	22B8
A54SX32A	0.2 2 μ	0	9	40BD, 42BD
		1	B	40BD, 42BD
	0.25 μ	1	B	22BD
A54SX72A	0.22 μ	0	9	40B2, 42B2
		1	B	40B2, 42B2
	0.25 μ	1	B	22B2

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

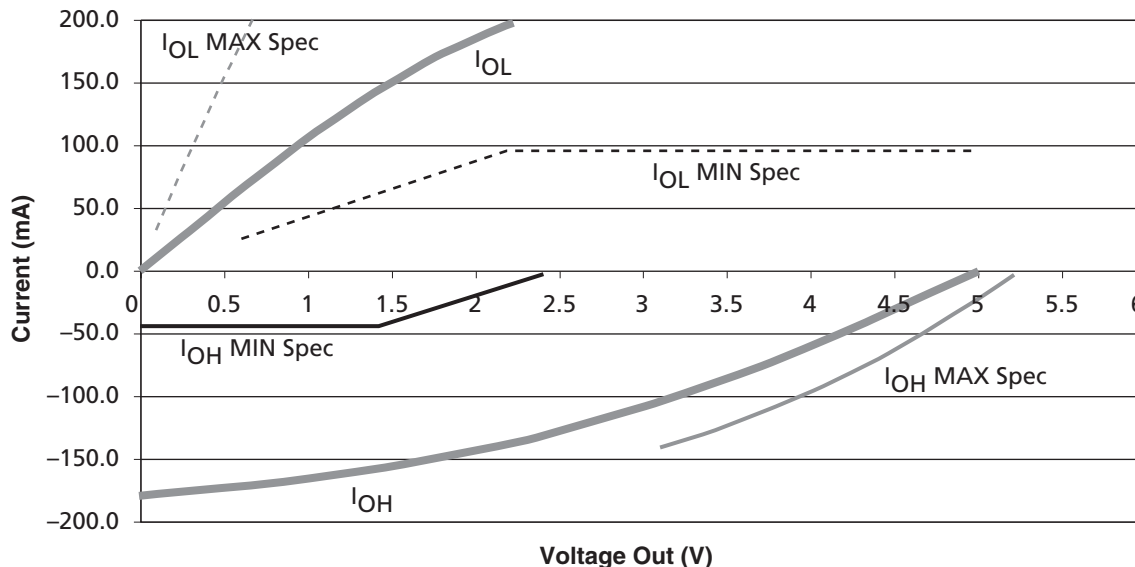


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CCI}$	–	V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CCI}$	-10	+10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$	–	V
V_{OL}	Output Low Voltage	$I_{OUT} = 1,500 \mu A$		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance ³		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

$$\theta_{CS} = 0.37^{\circ}\text{C/W}$$

= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{thermal resistance of the heat sink in } ^{\circ}\text{C/W}$$

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33^{\circ}\text{C/W} - 3.20^{\circ}\text{C/W} - 0.37^{\circ}\text{C/W}$$

$$\theta_{SA} = 9.76^{\circ}\text{C/W}$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Table 2-14 • A54SX08A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays²										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-16 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)	1.3		1.5		1.7		2.6		ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)	1.1		1.3		1.5		2.2		ns
t _{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew	0.4		0.5		0.5		0.8		ns
t _{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency	313		278		238		172		MHz
Routed Array Clock Networks										
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)	0.8		0.9		1.1		1.5		ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.2		1.4		2		ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)	0.8		0.9		1.1		1.5		ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.2		1.4		2		ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)	1.1		1.2		1.4		1.9		ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)	1.2		1.3		1.6		2.2		ns
t _{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)	0.7		0.8		0.9		1.3		ns
t _{RCKSW}	Maximum Skew (50% Load)	0.7		0.8		0.9		1.3		ns
t _{RCKSW}	Maximum Skew (100% Load)	0.8		0.9		1.1		1.5		ns

Table 2-21 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	0.9		1.0		1.2		1.4		1.9		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.8		0.9		1		1.4		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2		2.2		2.6		3.6		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.8		1.0		1.4		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.6		1.9		2.7		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.4		1.7		1.9		2.2		3.0		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.5		0.6		0.7		0.8		1.1		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	0.8		0.9		1.0		1.1		1.6		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.0		1.4		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTL	0.7		0.7		0.8		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL	0.9		1.1		1.2		1.4		2.0		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-21 • A54SX16A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.7		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.7		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays²												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.4		1.5		0.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-28 • A54SX32A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	0.8		0.9		1.1		1.2		1.7		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	1.2		1.3		1.5		1.8		2.5		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.6		0.7		0.8		0.9		1.3		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.8		0.9		1.0		1.2		1.6		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	1.4		1.6		1.8		2.2		3.0		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-29 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.25\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-35 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed ¹		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ²												
t _{PD}	Internal Array Module	1.0		1.1		1.3		1.5		2.0		ns
Predicted Routing Delays ³												
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.7		ns
t _{RD2}	FO = 2 Routing Delay	0.4		0.5		0.6		0.7		1		ns
t _{RD3}	FO = 3 Routing Delay	0.5		0.7		0.8		0.9		1.3		ns
t _{RD4}	FO = 4 Routing Delay	0.7		0.9		1		1.1		1.5		ns
t _{RD8}	FO = 8 Routing Delay	1.2		1.5		1.7		2.1		2.9		ns
t _{RD12}	FO = 12 Routing Delay	1.7		2.2		2.5		3		4.2		ns
R-Cell Timing												
t _{RCO}	Sequential Clock-to-Q	0.7		0.8		0.9		1.1		1.5		ns
t _{CLR}	Asynchronous Clear-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.8		1.0		1.4		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
t _{RECASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.3		ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS	0.8		1.0		1.1		1.3		1.7		ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI	0.6		0.7		0.7		0.9		1.2		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI	0.7		0.8		0.9		1.0		1.4		ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTTL	0.7		0.7		0.8		1.0		1.4		ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTTL	1.0		1.2		1.3		1.5		2.1		ns

Notes:

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-37 • A54SX72A Timing Characteristics (Continued)
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	-3 Speed*		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All -3 speed grades have been discontinued.

Table 2-39 • A54SX72A Timing Characteristics
(Worst-Case Commercial Conditions $V_{CCA} = 2.25\text{ V}$, $V_{CCI} = 2.3\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	–3 Speed ¹		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing ^{2, 3}												
t _{DLH}	Data-to-Pad Low to High	3.9		4.5		5.1		6.0		8.4		ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.6		4.1		4.8		6.7		ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12.7		14.6		16.5		19.4		27.2		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8		3.2		3.7		5.2		ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8		13.7		15.5		18.2		25.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.9		4.5		5.1		6.0		8.4		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5		2.8		3.3		4.7		ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.6		4.1		4.8		6.7		ns
d _{TLH} ⁴	Delta Low to High	0.031		0.037		0.043		0.051		0.071		ns/pF
d _{THL} ⁴	Delta High to Low	0.017		0.017		0.023		0.023		0.037		ns/pF
d _{THLS} ⁴	Delta High to Low—low slew	0.057		0.06		0.071		0.086		0.117		ns/pF

Note:

1. All –3 speed grades have been discontinued.
2. Delays based on 35 pF loading.
3. The equivalent IO Attribute settings for 2.5 V LVC MOS is 2.5 V LV TTL in the software.
4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$$
 where C_{load} is the load capacitance driven by the I/O in pF
 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V _{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

176-Pin TQFP	
Pin Number	A54SX32A Function
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	TMS
11	V _{CCI}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	V _{CCA}
23	GND
24	I/O
25	TRST, I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	V _{CCI}
33	V _{CCA}
34	I/O
35	I/O
36	I/O

176-Pin TQFP	
Pin Number	A54SX32A Function
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	GND
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	V _{CCI}
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	PRB, I/O
65	GND
66	V _{CCA}
67	NC
68	I/O
69	HCLK
70	I/O
71	I/O
72	I/O

176-Pin TQFP	
Pin Number	A54SX32A Function
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V _{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	TDO, I/O
88	I/O
89	GND
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V _{CCA}
99	V _{CCI}
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	GND

176-Pin TQFP	
Pin Number	A54SX32A Function
109	V _{CCA}
110	GND
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	V _{CCA}
123	GND
124	V _{CCI}
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	GND
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	V _{CCI}
141	I/O
142	I/O
143	I/O
144	I/O

144-Pin FBGA

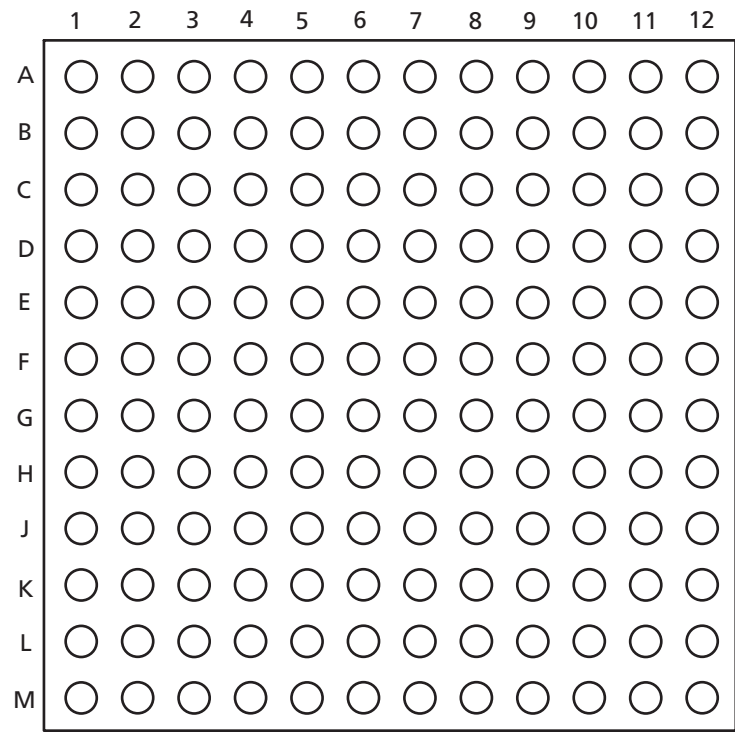


Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
K5	I/O	I/O	I/O
K6	V _{CCI}	V _{CCI}	V _{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V _{CCI}	V _{CCI}	V _{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V _{CCI}	V _{CCI}	V _{CCI}
L8	V _{CCI}	V _{CCI}	V _{CCI}
L9	V _{CCI}	V _{CCI}	V _{CCI}
L10	V _{CCI}	V _{CCI}	V _{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V _{CCA}	V _{CCA}	V _{CCA}
P14	I/O	I/O	I/O

484-Pin FBGA

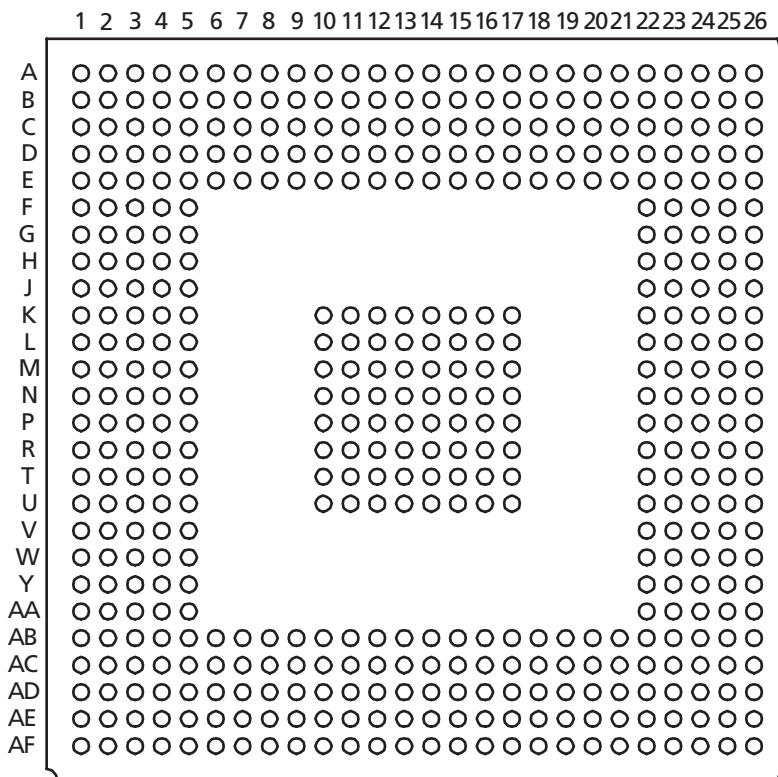


Figure 3-8 • 484-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

