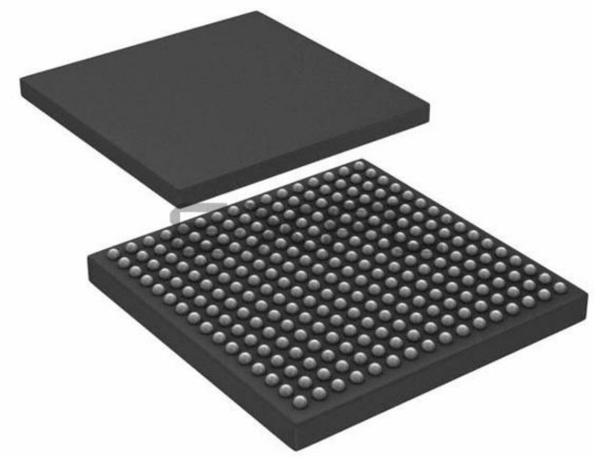
# Microsemi Corporation - A54SX16A-FG256M Datasheet



**Welcome to** E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 180 |
| Number of Gates | 24000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TC) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a54sx16a-fg256m |

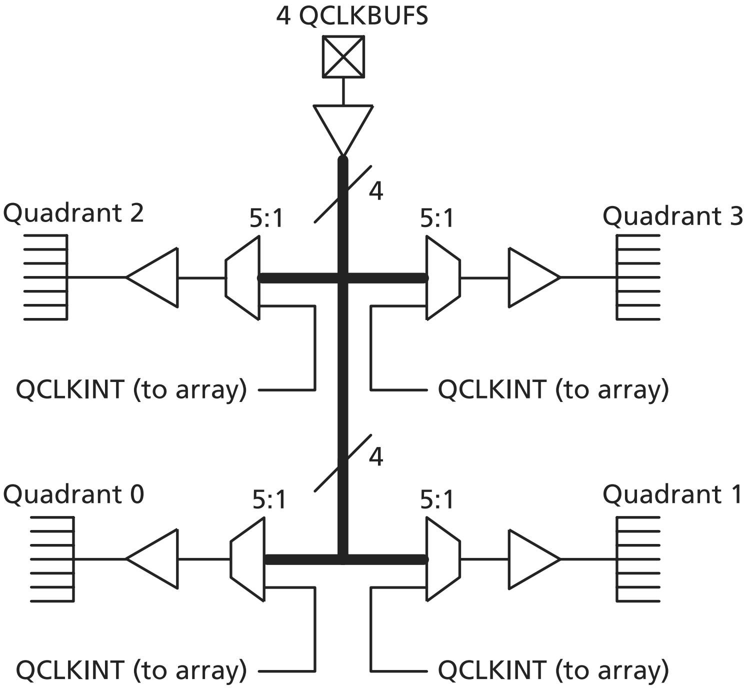


*Figure 1-9* • **SX-A QCLK Architecture**

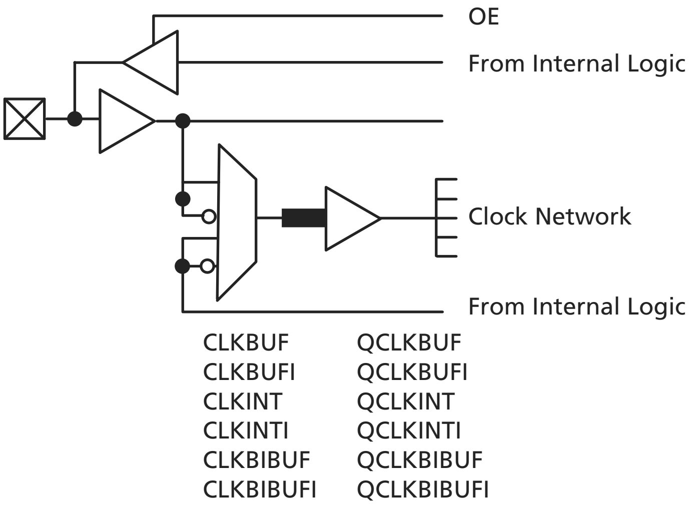


*Figure 1-10* • **A54SX72A Routed Clock and QCLK Buffer**

## Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

*Table 1-9* • **Device Configuration Options for Probe Capability (TRST Pin Reserved)**

| **JTAG Mode** | **TRST**[1] | **Security Fuse Programmed** | **PRA, PRB**[2] | **TDI, TCK, TDO**[2] |
|---|---|---|---|---|
| Dedicated | Low | No | User I/O[3] | JTAG Disabled |
| | High | No | Probe Circuit Outputs | JTAG I/O |
| Flexible | Low | No | User I/O[3] | User I/O[3] |
| | High | No | Probe Circuit Outputs | JTAG I/O |
| | | Yes | Probe Circuit Secured | Probe Circuit Secured |

***Notes:***

1. *If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

# Detailed Specifications

## Operating Conditions

*Table 2-1* • **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CCI}$ | DC Supply Voltage for I/Os | –0.3 to +6.0 | V |
| $V_{CCA}$ | DC Supply Voltage for Arrays | –0.3 to +3.0 | V |
| $V_I$ | Input Voltage | –0.5 to +5.75 | V |
| $V_O$ | Output Voltage | –0.5 to + $V_{CCI}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

**Note:** **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".*

*Table 2-2* • **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Units |
|---|---|---|---|
| Temperature Range | 0 to +70 | –40 to +85 | °C |
| 2.5 V Power Supply Range ($V_{CCA}$ and $V_{CCI}$) | 2.25 to 2.75 | 2.25 to 2.75 | V |
| 3.3 V Power Supply Range ($V_{CCI}$) | 3.0 to 3.6 | 3.0 to 3.6 | V |
| 5 V Power Supply Range ($V_{CCI}$) | 4.75 to 5.25 | 4.75 to 5.25 | V |

## Typical SX-A Standby Current

*Table 2-3* • **Typical Standby Current for SX-A at 25°C with $V_{CCA}$ = 2.5 V**

| Product | $V_{CCI}$ = 2.5 V | $V_{CCI}$ = 3.3 V | $V_{CCI}$ = 5 V |
|---|---|---|---|
| A54SX08A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX16A | 0.8 mA | 1.0 mA | 2.9 mA |
| A54SX32A | 0.9 mA | 1.0 mA | 3.0 mA |
| A54SX72A | 3.6 mA | 3.8 mA | 4.5 mA |

*Table 2-4* • **Supply Voltages**

| $V_{CCA}$ | $V_{CCI}$* | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|
| 2. 5 V | 2.5 V | 5.75 V | 2.7 V |
| 2.5 V | 3.3 V | 5.75 V | 3.6 V |
| 2.5 V | 5 V | 5.75 V | 5.25 V |

**Note:** **3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.*

# Electrical Specifications

*Table 2-5* • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

| | | | Commercial | | Industrial | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | $V_{CCI}$ = Minimum<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 0.9 $V_{CCI}$ | | 0.9 $V_{CCI}$ | | V |
| | $V_{CCI}$ = Minimum<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –8 mA) | 2.4 | | 2.4 | | V |
| $V_{OL}$ | $V_{CCI}$ = Minimum<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{CCI}$ = Minimum<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 12 mA) | | 0.4 | | 0.4 | V |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | 5.75 | 2.0 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN}$ = $V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

*Table 2-6* • **2.5 V LVCMOS2 Electrical Specifications**

| | | | Commercial | | Industrial | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –100 µA) | 2.1 | | 2.1 | | V |
| | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 2.0 | | 2.0 | | V |
| | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OH}$ =–-2 mA) | 1.7 | | 1.7 | | V |
| $V_{OL}$ | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 100 µA) | | 0.2 | | 0.2 | V |
| | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{DD}$ = MIN,<br>$V_I$ = $V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 2 mA) | | 0.7 | | 0.7 | V |
| $V_{IL}$ | Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$ | | -0.3 | 0.7 | -0.3 | 0.7 | V |
| $V_{IH}$ | Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$ | | 1.7 | 5.75 | 1.7 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN}$ = $V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current, $V_{OUT}$ = $V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

# PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

*Table 2-7* • **DC Specifications (5 V PCI Operation)**

| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Units** |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 2.25 | 2.75 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 4.75 | 5.25 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | 5.75 | V |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.8 | V |
| $I_{IH}$ | Input High Leakage Current[1] | $V_{IN}$ = 2.7 | – | 70 | µA |
| $I_{IL}$ | Input Low Leakage Current[1] | $V_{IN}$ = 0.5 | – | –70 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –2 mA | 2.4 | – | V |
| $V_{OL}$ | Output Low Voltage[2] | $I_{OUT}$ = 3 mA, 6 mA | – | 0.55 | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | – | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |

***Notes:***

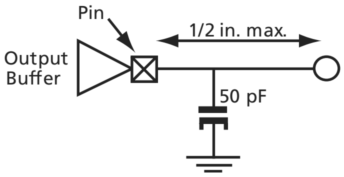
1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

*Table 2-8* • **AC Specifications (5 V PCI Operation)**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4$ [1] | –44 | – | mA |
| | | $1.4 \leq V_{OUT} < 2.4$ [1, 2] | $(–44 + (V_{OUT} – 1.4)/0.024)$ | – | mA |
| | | $3.1 < V_{OUT} < V_{CCI}$ [1, 3] | – | EQ 2-1 on page 2-5 | – |
| | (Test Point) | $V_{OUT} = 3.1$ [3] | – | –142 | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{OUT} \geq 2.2$ [1] | 95 | – | mA |
| | | $2.2 > V_{OUT} > 0.55$ [1] | $(V_{OUT}/0.023)$ | – | mA |
| | | $0.71 > V_{OUT} > 0$ [1, 3] | – | EQ 2-2 on page 2-5 | – |
| | (Test Point) | $V_{OUT} = 0.71$ [3] | – | 206 | mA |
| $I_{CL}$ | Low Clamp Current | $–5 < V_{IN} \leq –1$ | $–25 + (V_{IN} + 1)/0.015$ | – | mA |
| $slew_R$ | Output Rise Slew Rate | 0.4 V to 2.4 V load [4] | 1 | 5 | V/ns |
| $slew_F$ | Output Fall Slew Rate | 2.4 V to 0.4 V load [4] | 1 | 5 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*



# Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 2-5*

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{DC} = I_{Standby} * V_{CCA}$$

*EQ 2-6*

Note: For other combinations of temperature and voltage settings, refer to the *eX, SX-A and RT54SX-S Power Calculator*.

## AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{C\text{-cells}} + P_{R\text{-cells}} + P_{CLKA} + P_{CLKB} + P_{HCLK} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

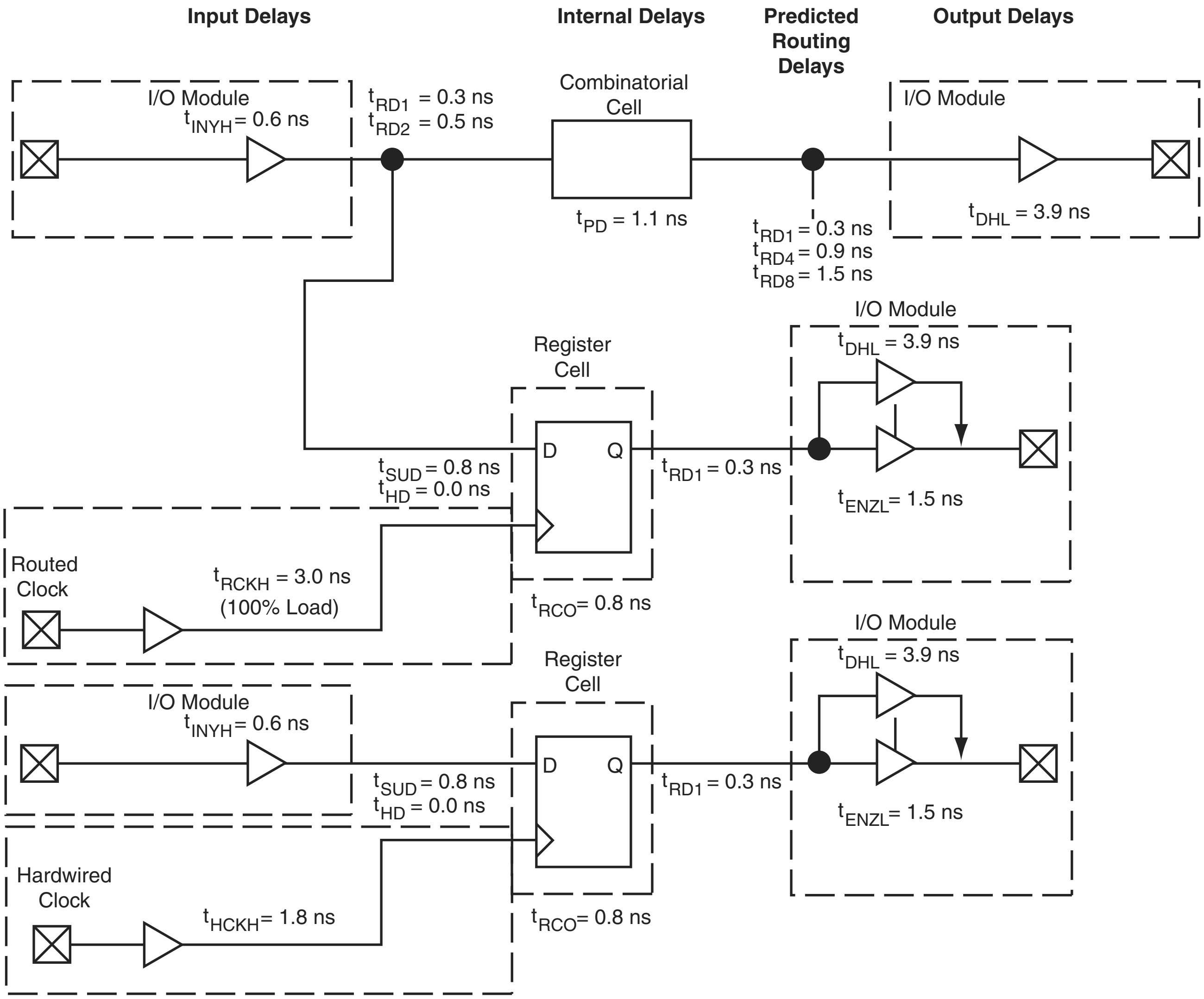
*EQ 2-7*

or:

$$\begin{aligned} P_{AC} = {} & V_{CCA}^2 * [(m * C_{EQCM} * fm)_{C\text{-cells}} + (m * C_{EQSM} * fm)_{R\text{-cells}} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} \\ & + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{CLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{CLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + \\ & (C_{EQHF} * f_{s1}))_{HCLK}] \end{aligned}$$

*EQ 2-8*

# SX-A Timing Model



***Note:*** **Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route.*

*Figure 2-3* • **SX-A Timing Model**

# Sample Path Calculations

## Hardwired Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKH}$
= $0.6 + 0.3 + 0.8 - 1.8 = -0.1$ ns

Clock-to-Out (Pad-to-Pad) = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= $1.8 + 0.8 + 0.3 + 3.9 = 6.8$ ns

## Routed Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH}$
= $0.6 + 0.3 + 0.8 - 3.0 = -1.3$ ns

Clock-to-Out (Pad-to-Pad) = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= $3.0 + 0.8 + 0.3 + 3.9 = 8.0$ ns

*Table 2-26* • **A54SX16A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | **–3 Speed**[1] | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **–F Speed** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3 V PCI Output Module Timing**[2] | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.0 | | 2.3 | | 2.6 | | 3.1 | | 4.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.5 | | 2.8 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| **3.3 V LVTTL Output Module Timing**[4] | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 9.5 | | 10.9 | | 12.4 | | 14.6 | | 20.4 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 15.8 | | 18.9 | | 21.3 | | 25.4 | | 34.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.025 | | 0.03 | | 0.03 | | 0.04 | | 0.045 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.015 | | 0.015 | | 0.015 | | 0.015 | | 0.025 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.053 | | 0.053 | | 0.067 | | 0.073 | | 0.107 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

*Table 2-28* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed[1] |  | –2 Speed |  | –1 Speed |  | Std. Speed |  | –F Speed |  | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |  |
| **C-Cell Propagation Delays[2]** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{PD}$ | Internal Array Module |  | 0.8 |  | 0.9 |  | 1.1 |  | 1.2 |  | 1.7 | ns |
| **Predicted Routing Delays[3]** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect |  | 0.1 |  | 0.1 |  | 0.1 |  | 0.1 |  | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect |  | 0.3 |  | 0.3 |  | 0.3 |  | 0.4 |  | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay |  | 0.3 |  | 0.3 |  | 0.4 |  | 0.5 |  | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay |  | 0.4 |  | 0.5 |  | 0.5 |  | 0.6 |  | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay |  | 0.5 |  | 0.6 |  | 0.7 |  | 0.8 |  | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay |  | 0.7 |  | 0.8 |  | 0.9 |  | 1.0 |  | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay |  | 1.2 |  | 1.4 |  | 1.5 |  | 1.8 |  | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay |  | 1.7 |  | 2.0 |  | 2.2 |  | 2.6 |  | 3.6 | ns |
| **R-Cell Timing** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{RCO}$ | Sequential Clock-to-Q |  | 0.6 |  | 0.7 |  | 0.8 |  | 0.9 |  | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q |  | 0.5 |  | 0.6 |  | 0.6 |  | 0.8 |  | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q |  | 0.6 |  | 0.7 |  | 0.7 |  | 0.9 |  | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.6 |  | 0.7 |  | 0.8 |  | 0.9 |  | 1.2 |  | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 |  | 0.0 |  | 0.0 |  | 0.0 |  | 0.0 |  | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.2 |  | 1.4 |  | 1.5 |  | 1.8 |  | 2.5 |  | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.3 |  | 0.4 |  | 0.4 |  | 0.5 |  | 0.7 |  | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | 0.3 |  | 0.3 |  | 0.3 |  | 0.4 |  | 0.6 |  | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.4 |  | 1.6 |  | 1.8 |  | 2.1 |  | 2.9 |  | ns |
| **Input Module Propagation Delays** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS |  | 0.6 |  | 0.7 |  | 0.8 |  | 0.9 |  | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS |  | 1.2 |  | 1.3 |  | 1.5 |  | 1.8 |  | 2.5 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI |  | 0.5 |  | 0.6 |  | 0.6 |  | 0.7 |  | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI |  | 0.6 |  | 0.7 |  | 0.8 |  | 0.9 |  | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL |  | 0.8 |  | 0.9 |  | 1.0 |  | 1.2 |  | 1.6 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL |  | 1.4 |  | 1.6 |  | 1.8 |  | 2.2 |  | 3.0 | ns |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-30* • **A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.7 | | 2.0 | | 2.2 | | 2.6 | | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.8 | | 3.3 | | 4.6 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.3 | | 2.7 | | 3.1 | | 3.6 | | 5 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.2 | | 2.5 | | 2.9 | | 3.4 | | 4.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-31* • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* |  | –2 Speed |  | –1 Speed |  | Std. Speed |  | –F Speed |  | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |  |
| **Dedicated (Hardwired) Array Clock Networks** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) |  | 1.7 |  | 1.9 |  | 2.2 |  | 2.6 |  | 4.0 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) |  | 1.7 |  | 2.0 |  | 2.2 |  | 2.6 |  | 4.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 |  | 1.6 |  | 1.8 |  | 2.1 |  | 2.9 |  | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 |  | 1.6 |  | 1.8 |  | 2.1 |  | 2.9 |  | ns |
| $t_{HCKSW}$ | Maximum Skew |  | 0.6 |  | 0.6 |  | 0.7 |  | 0.8 |  | 1.3 | ns |
| $t_{HP}$ | Minimum Period | 2.8 |  | 3.2 |  | 3.6 |  | 4.2 |  | 5.8 |  | ns |
| $f_{HMAX}$ | Maximum Frequency |  | 357 |  | 313 |  | 278 |  | 238 |  | 172 | MHz |
| **Routed Array Clock Networks** |  |  |  |  |  |  |  |  |  |  |  |  |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) |  | 2.2 |  | 2.5 |  | 2.8 |  | 3.3 |  | 4.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) |  | 2.1 |  | 2.5 |  | 2.8 |  | 3.3 |  | 4.5 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) |  | 2.4 |  | 2.7 |  | 3.1 |  | 3.6 |  | 5.1 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) |  | 2.2 |  | 2.6 |  | 2.9 |  | 3.4 |  | 4.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) |  | 2.5 |  | 2.8 |  | 3.2 |  | 3.8 |  | 5.3 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) |  | 2.4 |  | 2.8 |  | 3.1 |  | 3.7 |  | 5.2 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 |  | 1.6 |  | 1.8 |  | 2.1 |  | 2.9 |  | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 |  | 1.6 |  | 1.8 |  | 2.1 |  | 2.9 |  | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) |  | 1.0 |  | 1.1 |  | 1.3 |  | 1.5 |  | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) |  | 1.0 |  | 1.1 |  | 1.3 |  | 1.5 |  | 2.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) |  | 1.0 |  | 1.1 |  | 1.3 |  | 1.5 |  | 2.1 | ns |

**Note:** **All –3 speed grades have been discontinued.*

*Table 2-36* • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 2.25 V, $T_J$ = 70°C)**

| Parameter | Description | –3 Speed* Min. | –3 Speed* Max. | –2 Speed Min. | –2 Speed Max. | –1 Speed Min. | –1 Speed Max. | Std. Speed Min. | Std. Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| $t_{HP}$ | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.7 | | 4.3 | | 6.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.4 | | 2.8 | | 3.2 | | 3.7 | | 5.2 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.9 | | 3.3 | | 3.8 | | 4.5 | | 6.2 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.1 | | 3.6 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| **Quadrant Array Clock Networks** | | | | | | | | | | | | |
| $t_{QCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | ns |
| $t_{QCHKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{QCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{QCHKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.9 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

| 100-TQFP | | | |
|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | I/O | I/O | I/O |
| 80 | I/O | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | CLKA | CLKA | CLKA |
| 88 | CLKB | CLKB | CLKB |
| 89 | NC | NC | NC |
| 90 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 91 | GND | GND | GND |
| 92 | PRA, I/O | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | I/O | I/O | I/O |
| 99 | I/O | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O | TCK, I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | NC | NC | NC |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | NC | NC | NC |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| D11 | $V_{CCA}$ |
| D12 | NC |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | $V_{CCI}$ |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | $V_{CCA}$ |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | NC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| L14 | GND |
| L20 | NC |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | $V_{CCA}$ |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | $V_{CCA}$ |
| M21 | I/O |
| M22 | I/O |
| M23 | $V_{CCI}$ |
| N1 | I/O |
| N2 | TRST, I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |
| T22 | I/O |
| T23 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | $V_{CCA}$ |
| U4 | I/O |
| U20 | I/O |
| U21 | $V_{CCA}$ |
| U22 | I/O |
| U23 | I/O |
| V1 | $V_{CCI}$ |
| V2 | I/O |
| V3 | I/O |
| V4 | I/O |
| V20 | I/O |
| V21 | I/O |

| 329-Pin PBGA | |
|---|---|
| **Pin Number** | **A54SX32A Function** |
| V22 | I/O |
| V23 | I/O |
| W1 | I/O |
| W2 | I/O |
| W3 | I/O |
| W4 | I/O |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |
| W23 | NC |
| Y1 | NC |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | GND |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | I/O |
| Y12 | $V_{CCA}$ |
| Y13 | NC |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | GND |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v5.2<br>(June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1<br>February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| | Table 2-11 was updated. | 2-9 |

# Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

## Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

## Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

## Unmarked (production)

This datasheet version contains information that is considered to be final.

## Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

# International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.

www.actel.com

**Actel Corporation**
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
**Phone** 650.318.4200
**Fax** 650.318.4600

**Actel Europe Ltd.**
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom
**Phone** +44 (0) 1276 609 300
**Fax** +44 (0) 1276 607 540

**Actel Japan**
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
**Phone** +81.03.3445.7671
**Fax** +81.03.3445.7668
www.jp.actel.com

**Actel Hong Kong**
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
**Phone** +852 2185 6460
**Fax** +852 2185 6488
www.actel.com.cn

5172147-10/2.07