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Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-ftq144

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Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using $0.22\,\mu$ / $0.25\,\mu$ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).

Figure 1-11 • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Figure 1-12 • **Device Selection Wizard**

Table 1-5 • **Reserve Pin Definitions**

Pin	Function
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up
Reserve Probe	Keeps pins from being used or regular I/O

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V$_{CCI}$ should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6 • **Boundary-Scan Pin Configurations and Functions**

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Pin Description

CLKA/B, I/O   **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O   **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND   **Ground**

Low supply voltage.

HCLK   **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O   **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC   **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O   **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O   **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O   **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O   **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS   **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O   **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V$_{CCI}$ **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V$_{CCI}$ power pins in the device should be connected.

V$_{CCA}$ **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V$_{CCA}$ power pins in the device should be connected.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • **DC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	5.75	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{IH}	Input High Leakage Current[1]	$V_{IN} = 2.7$	–	70	µA
I_{IL}	Input Low Leakage Current[1]	$V_{IN} = 0.5$	–	–70	µA
V_{OH}	Output High Voltage	$I_{OUT} = –2$ mA	2.4	–	V
V_{OL}	Output Low Voltage[2]	$I_{OUT} = 3$ mA, 6 mA	–	0.55	V
C_{IN}	Input Pin Capacitance[3]		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*

2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*

3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

θ_{JA} = 17.1°C/W is taken from Table 2-12 on page 2-11

T_A = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°C - 125°C}{17.1°C/W} = 1.46\ W$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

T_J = 110°C

T_A = 70°C

From the datasheet:

θ_{JA} = 18.0°C/W

θ_{JC} = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°C - 70°C}{18.0°C/W} = 2.22\ W$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°C - 70°C}{3.00\ W} = 13.33°C/W$$

EQ 2-13

Table 2-14 • **A54SX08A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V$_{CCA}$ = 2.25 V, V$_{CCI}$ = 3.0 V, T$_J$ = 70°C)

Parameter	Description	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
t$_{INYH}$	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t$_{INYL}$	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t$_{INYH}$	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t$_{INYL}$	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays[2]										
t$_{IRD1}$	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t$_{IRD2}$	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t$_{IRD3}$	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t$_{IRD4}$	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t$_{IRD8}$	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t$_{IRD12}$	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. *For dual-module macros, use t$_{PD}$ + t$_{RD1}$ + t$_{PDn}$, t$_{RCO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-24 • **A54SX16A Timing Characteristics**
   (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} =4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed* Min.	–3 Speed* Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.*

Table 2-27 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V$_{CCA}$ = 2.25 V, V$_{CCI}$ = 4.75 V, T$_J$ = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t$_{DLH}$	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t$_{DHL}$	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		2.2		2.5		2.8		3.3		4.6	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d$_{TLH}$[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d$_{THL}$[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t$_{DLH}$	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t$_{DHL}$	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t$_{DHLS}$	Data-to-Pad High to Low—low slew		6.7		7.7		8.7		10.2		14.3	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t$_{ENZLS}$	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d$_{TLH}$[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d$_{THL}$[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d$_{THLS}$[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*

2. *Delays based on 50 pF loading.*

3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V$_{CCI}$ value into the following equation:*

   Slew Rate [V/ns] = (0.1*V$_{CCI}$ – 0.9*V$_{CCI}$)/ (C$_{load}$ * d$_{T[LH|HL|HLS]}$)

   where C$_{load}$ is the load capacitance driven by the I/O in pF

   $\quad\quad$ *d$_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*

4. *Delays based on 35 pF loading.*

Table 2-31 • **A54SX32A Timing Characteristics**
   (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed* Min.	–3 Speed* Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.*

Table 2-35 • **A54SX72A Timing Characteristics**
   (Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[2]												
t_{PD}	Internal Array Module		1.0		1.1		1.3		1.5		2.0	ns
Predicted Routing Delays[3]												
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{RD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{RD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{RD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{RD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{RD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.1		1.5	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.7		0.7		0.9		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Minimum Pulse Width	1.5		1.7		2.0		2.3		3.2		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.6		0.7		0.8		0.9		1.3	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		1.0		1.1		1.3		1.7	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.7		0.7		0.9		1.2	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.2		1.3		1.5		2.1	ns

Notes:

1. *All –3 speed grades have been discontinued.*

2. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*

3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-38 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.*

208-Pin PQFP					208-Pin PQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function	Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND	36	I/O	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O	37	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O	38	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O	39	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O	40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
6	NC	I/O	I/O	I/O	41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
7	I/O	I/O	I/O	I/O	42	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O	43	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O	44	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O	45	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS	46	I/O	I/O	I/O	I/O
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}	47	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	48	NC	I/O	I/O	I/O
14	NC	I/O	I/O	I/O	49	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	50	NC	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O	51	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O	52	GND	GND	GND	GND
18	I/O	I/O	I/O	GND	53	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	V_{CCA}	54	I/O	I/O	I/O	I/O
20	NC	I/O	I/O	I/O	55	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O	56	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O	57	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O	58	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O	59	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O	60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
26	GND	GND	GND	GND	61	NC	I/O	I/O	I/O
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}	62	I/O	I/O	I/O	I/O
28	GND	GND	GND	GND	63	I/O	I/O	I/O	I/O
29	I/O	I/O	I/O	I/O	64	NC	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O	65	I/O	I/O	NC	I/O
31	NC	I/O	I/O	I/O	66	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O	67	NC	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O	68	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O	69	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O	70	NC	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin TQFP

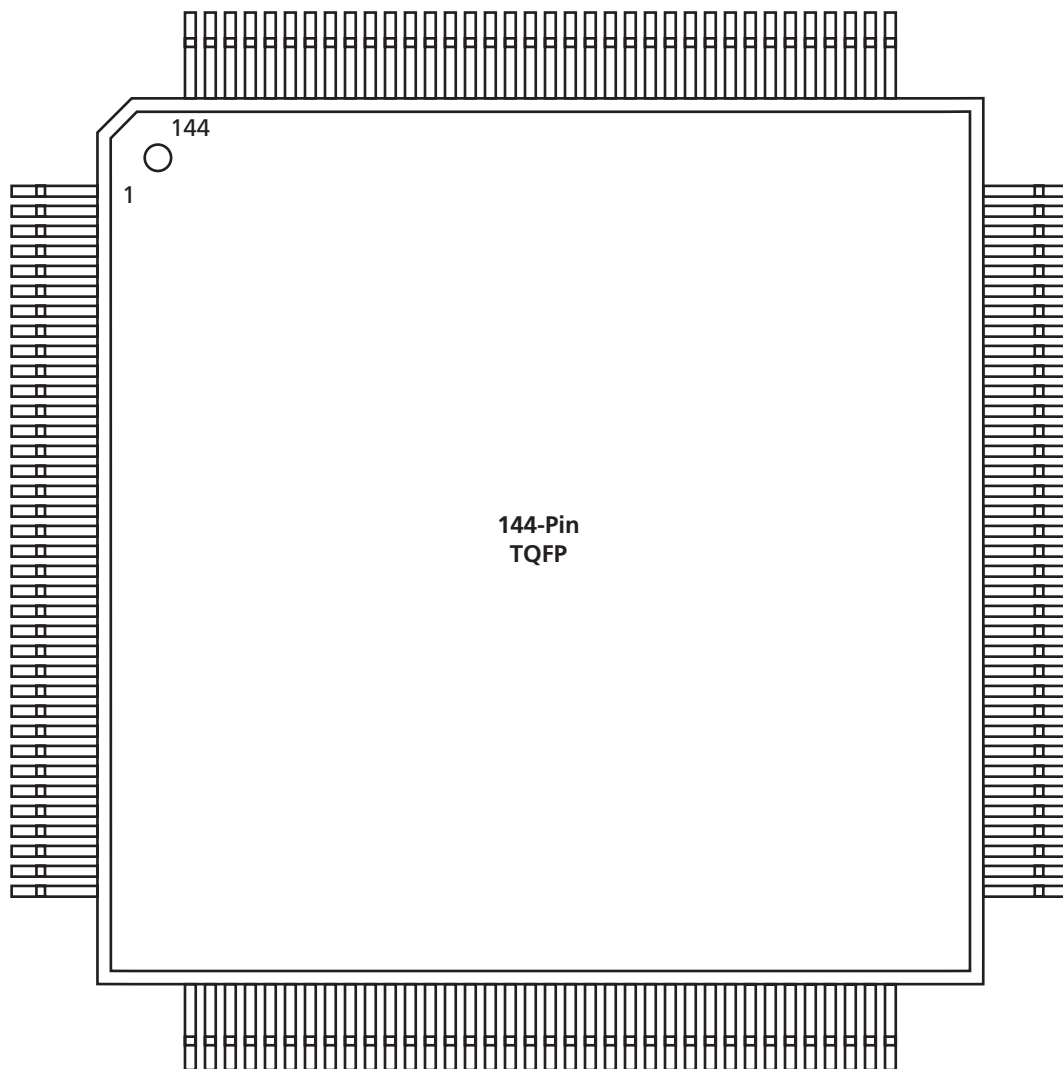*Figure 3-3* • **144-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at
http://www.actel.com/products/rescenter/package/index.html.

144-Pin TQFP				144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND	38	I/O	I/O	I/O
2	TDI, I/O	TDI, I/O	TDI, I/O	39	I/O	I/O	I/O
3	I/O	I/O	I/O	40	I/O	I/O	I/O
4	I/O	I/O	I/O	41	I/O	I/O	I/O
5	I/O	I/O	I/O	42	I/O	I/O	I/O
6	I/O	I/O	I/O	43	I/O	I/O	I/O
7	I/O	I/O	I/O	44	V_{CCI}	V_{CCI}	V_{CCI}
8	I/O	I/O	I/O	45	I/O	I/O	I/O
9	TMS	TMS	TMS	46	I/O	I/O	I/O
10	V_{CCI}	V_{CCI}	V_{CCI}	47	I/O	I/O	I/O
11	GND	GND	GND	48	I/O	I/O	I/O
12	I/O	I/O	I/O	49	I/O	I/O	I/O
13	I/O	I/O	I/O	50	I/O	I/O	I/O
14	I/O	I/O	I/O	51	I/O	I/O	I/O
15	I/O	I/O	I/O	52	I/O	I/O	I/O
16	I/O	I/O	I/O	53	I/O	I/O	I/O
17	I/O	I/O	I/O	54	PRB, I/O	PRB, I/O	PRB, I/O
18	I/O	I/O	I/O	55	I/O	I/O	I/O
19	NC	NC	NC	56	V_{CCA}	V_{CCA}	V_{CCA}
20	V_{CCA}	V_{CCA}	V_{CCA}	57	GND	GND	GND
21	I/O	I/O	I/O	58	NC	NC	NC
22	TRST, I/O	TRST, I/O	TRST, I/O	59	I/O	I/O	I/O
23	I/O	I/O	I/O	60	HCLK	HCLK	HCLK
24	I/O	I/O	I/O	61	I/O	I/O	I/O
25	I/O	I/O	I/O	62	I/O	I/O	I/O
26	I/O	I/O	I/O	63	I/O	I/O	I/O
27	I/O	I/O	I/O	64	I/O	I/O	I/O
28	GND	GND	GND	65	I/O	I/O	I/O
29	V_{CCI}	V_{CCI}	V_{CCI}	66	I/O	I/O	I/O
30	V_{CCA}	V_{CCA}	V_{CCA}	67	I/O	I/O	I/O
31	I/O	I/O	I/O	68	V_{CCI}	V_{CCI}	V_{CCI}
32	I/O	I/O	I/O	69	I/O	I/O	I/O
33	I/O	I/O	I/O	70	I/O	I/O	I/O
34	I/O	I/O	I/O	71	TDO, I/O	TDO, I/O	TDO, I/O
35	I/O	I/O	I/O	72	I/O	I/O	I/O
36	GND	GND	GND	73	GND	GND	GND
37	I/O	I/O	I/O	74	I/O	I/O	I/O

484-Pin FBGA				484-Pin FBGA				484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function		Pin Number	A54SX32A Function	A54SX72A Function		Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O		E2	NC*	I/O		G1	NC*	I/O
C20	V_{CCI}	V_{CCI}		E3	I/O	I/O		G2	NC*	I/O
C21	I/O	I/O		E4	I/O	I/O		G3	NC*	I/O
C22	I/O	I/O		E5	GND	GND		G4	I/O	I/O
C23	I/O	I/O		E6	TDI, IO	TDI, IO		G5	I/O	I/O
C24	I/O	I/O		E7	I/O	I/O		G22	I/O	I/O
C25	NC*	I/O		E8	I/O	I/O		G23	V_{CCA}	V_{CCA}
C26	NC*	I/O		E9	I/O	I/O		G24	I/O	I/O
D1	NC*	I/O		E10	I/O	I/O		G25	NC*	I/O
D2	TMS	TMS		E11	I/O	I/O		G26	NC*	I/O
D3	I/O	I/O		E12	I/O	I/O		H1	NC*	I/O
D4	V_{CCI}	V_{CCI}		E13	V_{CCA}	V_{CCA}		H2	NC*	I/O
D5	NC*	I/O		E14	CLKB	CLKB		H3	I/O	I/O
D6	TCK, I/O	TCK, I/O		E15	I/O	I/O		H4	I/O	I/O
D7	I/O	I/O		E16	I/O	I/O		H5	I/O	I/O
D8	I/O	I/O		E17	I/O	I/O		H22	I/O	I/O
D9	I/O	I/O		E18	I/O	I/O		H23	I/O	I/O
D10	I/O	I/O		E19	I/O	I/O		H24	I/O	I/O
D11	I/O	I/O		E20	I/O	I/O		H25	NC*	I/O
D12	I/O	QCLKC		E21	I/O	I/O		H26	NC*	I/O
D13	I/O	I/O		E22	I/O	I/O		J1	NC*	I/O
D14	I/O	I/O		E23	I/O	I/O		J2	NC*	I/O
D15	I/O	I/O		E24	I/O	I/O		J3	I/O	I/O
D16	I/O	I/O		E25	V_{CCI}	V_{CCI}		J4	I/O	I/O
D17	I/O	I/O		E26	GND	GND		J5	I/O	I/O
D18	I/O	I/O		F1	V_{CCI}	V_{CCI}		J22	I/O	I/O
D19	I/O	I/O		F2	NC*	I/O		J23	I/O	I/O
D20	I/O	I/O		F3	NC*	I/O		J24	I/O	I/O
D21	V_{CCI}	V_{CCI}		F4	I/O	I/O		J25	V_{CCI}	V_{CCI}
D22	GND	GND		F5	I/O	I/O		J26	NC*	I/O
D23	I/O	I/O		F22	I/O	I/O		K1	I/O	I/O
D24	I/O	I/O		F23	I/O	I/O		K2	V_{CCI}	V_{CCI}
D25	NC*	I/O		F24	I/O	I/O		K3	I/O	I/O
D26	NC*	I/O		F25	I/O	I/O		K4	I/O	I/O
E1	NC*	I/O		F26	NC*	I/O		K5	V_{CCA}	V_{CCA}

Note: *These pins must be left floating on the A54SX32A device.*

484-Pin FBGA			484-Pin FBGA			484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND	M5	I/O	I/O	P4	I/O	I/O
K11	GND	GND	M10	GND	GND	P5	V$_{CCA}$	V$_{CCA}$
K12	GND	GND	M11	GND	GND	P10	GND	GND
K13	GND	GND	M12	GND	GND	P11	GND	GND
K14	GND	GND	M13	GND	GND	P12	GND	GND
K15	GND	GND	M14	GND	GND	P13	GND	GND
K16	GND	GND	M15	GND	GND	P14	GND	GND
K17	GND	GND	M16	GND	GND	P15	GND	GND
K22	I/O	I/O	M17	GND	GND	P16	GND	GND
K23	I/O	I/O	M22	I/O	I/O	P17	GND	GND
K24	NC*	NC	M23	I/O	I/O	P22	I/O	I/O
K25	NC*	I/O	M24	I/O	I/O	P23	I/O	I/O
K26	NC*	I/O	M25	NC*	I/O	P24	V$_{CCI}$	V$_{CCI}$
L1	NC*	I/O	M26	NC*	I/O	P25	I/O	I/O
L2	NC*	I/O	N1	I/O	I/O	P26	I/O	I/O
L3	I/O	I/O	N2	V$_{CCI}$	V$_{CCI}$	R1	NC*	I/O
L4	I/O	I/O	N3	I/O	I/O	R2	NC*	I/O
L5	I/O	I/O	N4	I/O	I/O	R3	I/O	I/O
L10	GND	GND	N5	I/O	I/O	R4	I/O	I/O
L11	GND	GND	N10	GND	GND	R5	TRST, I/O	TRST, I/O
L12	GND	GND	N11	GND	GND	R10	GND	GND
L13	GND	GND	N12	GND	GND	R11	GND	GND
L14	GND	GND	N13	GND	GND	R12	GND	GND
L15	GND	GND	N14	GND	GND	R13	GND	GND
L16	GND	GND	N15	GND	GND	R14	GND	GND
L17	GND	GND	N16	GND	GND	R15	GND	GND
L22	I/O	I/O	N17	GND	GND	R16	GND	GND
L23	I/O	I/O	N22	V$_{CCA}$	V$_{CCA}$	R17	GND	GND
L24	I/O	I/O	N23	I/O	I/O	R22	I/O	I/O
L25	I/O	I/O	N24	I/O	I/O	R23	I/O	I/O
L26	I/O	I/O	N25	I/O	I/O	R24	I/O	I/O
M1	NC*	NC	N26	NC*	NC	R25	NC*	I/O
M2	I/O	I/O	P1	NC*	I/O	R26	NC*	I/O
M3	I/O	I/O	P2	NC*	I/O	T1	NC*	I/O
M4	I/O	I/O	P3	I/O	I/O	T2	NC*	I/O

Note: *These pins must be left floating on the A54SX32A device.*

| 484-Pin FBGA | | | | 484-Pin FBGA | | |
Pin Number	A54SX32A Function	A54SX72A Function		Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O		V2	NC*	I/O
T4	I/O	I/O		V3	I/O	I/O
T5	I/O	I/O		V4	I/O	I/O
T10	GND	GND		V5	I/O	I/O
T11	GND	GND		V22	V_{CCA}	V_{CCA}
T12	GND	GND		V23	I/O	I/O
T13	GND	GND		V24	I/O	I/O
T14	GND	GND		V25	NC*	I/O
T15	GND	GND		V26	NC*	I/O
T16	GND	GND		W1	I/O	I/O
T17	GND	GND		W2	I/O	I/O
T22	I/O	I/O		W3	I/O	I/O
T23	I/O	I/O		W4	I/O	I/O
T24	I/O	I/O		W5	I/O	I/O
T25	NC*	I/O		W22	I/O	I/O
T26	NC*	I/O		W23	V_{CCA}	V_{CCA}
U1	I/O	I/O		W24	I/O	I/O
U2	V_{CCI}	V_{CCI}		W25	NC*	I/O
U3	I/O	I/O		W26	NC*	I/O
U4	I/O	I/O		Y1	NC*	I/O
U5	I/O	I/O		Y2	NC*	I/O
U10	GND	GND		Y3	I/O	I/O
U11	GND	GND		Y4	I/O	I/O
U12	GND	GND		Y5	NC*	I/O
U13	GND	GND		Y22	I/O	I/O
U14	GND	GND		Y23	I/O	I/O
U15	GND	GND		Y24	V_{CCI}	V_{CCI}
U16	GND	GND		Y25	I/O	I/O
U17	GND	GND		Y26	I/O	I/O
U22	I/O	I/O				
U23	I/O	I/O				
U24	I/O	I/O				
U25	V_{CCI}	V_{CCI}				
U26	I/O	I/O				
V1	NC*	I/O				

Note: *These pins must be left floating on the A54SX32A device.*

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9