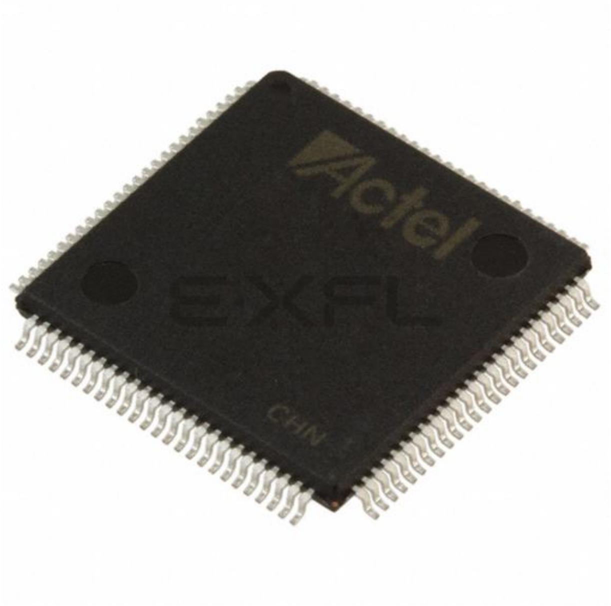
Microchip Technology - A54SX16A-TQ100A Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-tq100a

Temperature Grade Offering

Package	**A54SX08A**	**A54SX16A**	**A54SX32A**	**A54SX72A**
PQ208	C,I,A,M	C,I,A,M	C,I,A,M	C,I,A,M
TQ100	C,I,A,M	C,I,A,M	C,I,A,M	
TQ144	C,I,A,M	C,I,A,M	C,I,A,M	
TQ176			C,I,M	
BG329			C,I,M	
FG144	C,I,A,M	C,I,A,M	C,I,A,M	
FG256		C,I,A,M	C,I,A,M	C,I,A,M
FG484			C,I,M	C,I,A,M
CQ208			C,M,B	C,M,B
CQ256			C,M,B	C,M,B

Notes:

1. *C = Commercial*
2. *I = Industrial*
3. *A = Automotive*
4. *M = Military*
5. *B = MIL-STD-883 Class B*
6. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
7. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Speed Grade and Temperature Grade Matrix

	F	**Std**	**–1**	**–2**	**–3**
Commercial	✓	✓	✓	✓	Discontinued
Industrial		✓	✓	✓	Discontinued
Automotive		✓			
Military		✓	✓		
MIL-STD-883B		✓	✓		

Notes:

1. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
2. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Contact your Actel Sales representative for more information on availability.

Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 μ / 0.25 μ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).

Figure 1-11 • **FuseLock**

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os*. Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

Table 2-8 • **AC Specifications (5 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ [1]	–44	–	mA
		$1.4 \leq V_{OUT} < 2.4$ [1, 2]	$(-44 + (V_{OUT} - 1.4)/0.024)$	–	mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]	–	EQ 2-1 on page 2-5	–
	(Test Point)	$V_{OUT} = 3.1$ [3]	–	–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ [1]	95	–	mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$	–	mA
		$0.71 > V_{OUT} > 0$ [1, 3]	–	EQ 2-2 on page 2-5	–
	(Test Point)	$V_{OUT} = 0.71$ [3]	–	206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	–	mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

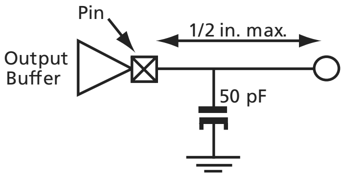


Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

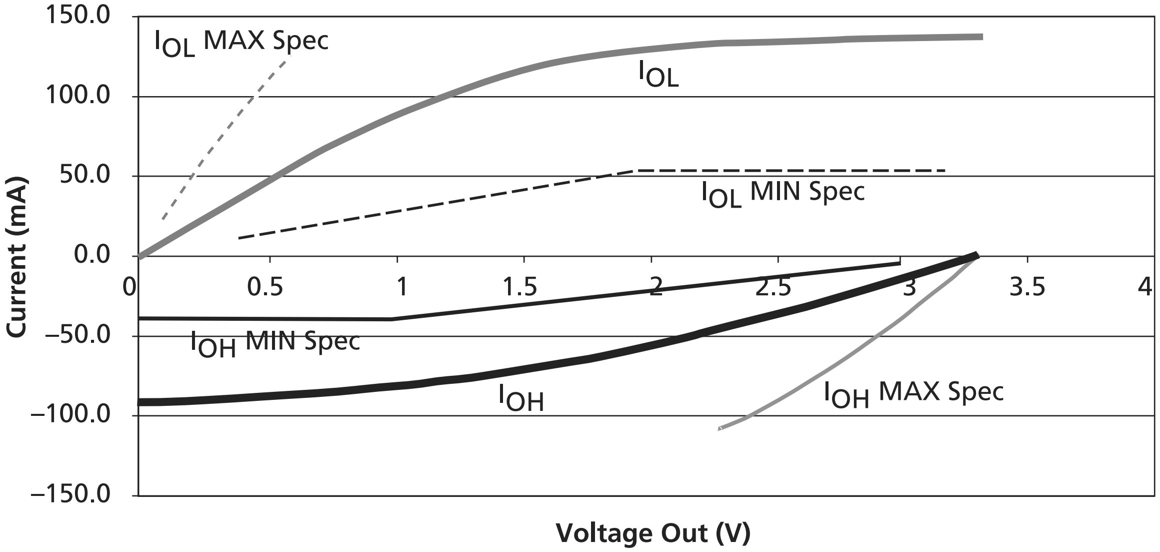


Figure 2-2 • **3.3 V PCI V/I Curve for SX-A Family**

$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$
for $0.7\ V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$
for $0V < V_{OUT} < 0.18\ V_{CCI}$

EQ 2-4

Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 2-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{DC} = I_{Standby} * V_{CCA}$$

EQ 2-6

Note: For other combinations of temperature and voltage settings, refer to the *eX, SX-A and RT54SX-S Power Calculator*.

AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{C\text{-cells}} + P_{R\text{-cells}} + P_{CLKA} + P_{CLKB} + P_{HCLK} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 2-7

or:

$$\begin{aligned} P_{AC} = \; & V_{CCA}^2 * [(m * C_{EQCM} * fm)_{C\text{-cells}} + (m * C_{EQSM} * fm)_{R\text{-cells}} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} \\ & + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{CLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{CLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + \\ & (C_{EQHF} * f_{s1}))_{HCLK}] \end{aligned}$$

EQ 2-8

Where:

C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF

C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of CLKA/B in pF

C_{EQHV} = Variable capacitance of HCLK in pF

C_{EQHF} = Fixed capacitance of HCLK in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average CLKA rate in MHz

f_{q2} = Average CLKB rate in MHz

f_{s1} = Average HCLK rate in MHz

m = Number of logic modules switching at fm

n = Number of input buffers switching at fn

p = Number of output buffers switching at fp

q_1 = Number of clock loads on CLKA

q_2 = Number of clock loads on CLKB

r_1 = Fixed capacitance due to CLKA

r_2 = Fixed capacitance due to CLKB

s_1 = Number of clock loads on HCLK

x = Number of I/Os at logic low

y = Number of I/Os at logic high

Table 2-11 • **CEQ Values for SX-A Devices**

	A54SX08A	**A54SX16A**	**A54SX32A**	**A54SX72A**
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules
Inputs Switching (n) = Number inputs/4
Outputs Switching (p) = Number of outputs/4
CLKA Loads (q1) = 20% of R-cells
CLKB Loads (q2) = 20% of R-cells
Load Capacitance (CL) = 35 pF
Average Logic Module Switching Rate (fm) = f/10
Average Input Switching Rate (fn) =f/5
Average Output Switching Rate (fp) = f/10
Average CLKA Rate (fq1) = f/2
Average CLKB Rate (fq2) = f/2
Average HCLK Rate (fs1) = f
HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

Table 2-26 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.0		2.3		2.6		3.1		4.3	ns
t_{DHL}	Data-to-Pad High to Low		2.2		2.5		2.8		3.3		4.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.0		2.3		2.6		3.1		4.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.2		2.5		2.8		3.3		4.6	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.8		3.2		3.6		4.3		6.0	ns
t_{DHL}	Data-to-Pad High to Low		2.7		3.1		3.5		4.1		5.7	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		9.5		10.9		12.4		14.6		20.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		3.2		3.6		4.3		6.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.7		3.1		3.5		4.1		5.7	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-29 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-32 • **A54SX32A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing [2,3]												
t_{DLH}	Data-to-Pad Low to High		3.3		3.8		4.2		5.0		7.0	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		11.1		12.8		14.5		17.0		23.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.3		3.8		4.2		5.0		7.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.2		3.8		5.3	ns
d_{TLH}[4]	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[4]	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[4]	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1 \cdot V_{CCI} - 0.9 \cdot V_{CCI}) / (C_{load} \cdot d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-34 • **A54SX32A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

		–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.1		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		1.9		2.2		2.5		2.9		4.1	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.6		7.6		8.6		10.1		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} *is the load capacitance driven by the I/O in pF*
   $d_{T[LH|HL|HLS]}$ *is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

Table 2-36 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

		–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-37 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed* Min.	–3 Speed* Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		1.9		2.1		2.5		3.8	ns
t_{HPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{HPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{HCKSW}	Maximum Skew		1.4		1.6		1.8		2.1		3.3	ns
t_{HP}	Minimum Period	3.0		3.4		4.0		4.6		6.4		ns
f_{HMAX}	Maximum Frequency		333		294		250		217		156	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.8		3.3		3.7		4.3		6.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.8		3.2		3.7		5.2	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.2	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.6		3.0		3.4		4.0		5.6	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		3.1		3.6		4.1		4.8		6.7	ns
t_{RPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{RPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.2		2.5		3		4.1	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.1		2.4		2.8		3.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.1		2.4		2.8		3.9	ns
Quadrant Array Clock Networks												
t_{QCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		1.9		2.7	ns
t_{QCHKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.3		1.5		1.7		2		2.8	ns
t_{QCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.5		1.7		1.9		2.2		3.1	ns
t_{QCHKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.8		2		2.3		3.2	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-39 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing[2, 3]												
t_{DLH}	Data-to-Pad Low to High		3.9		4.5		5.1		6.0		8.4	ns
t_{DHL}	Data-to-Pad High to Low		3.1		3.6		4.1		4.8		6.7	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		12.7		14.6		16.5		19.4		27.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.5		5.1		6.0		8.4	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.1		3.6		4.1		4.8		6.7	ns
d_{TLH}[4]	Delta Low to High		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[4]	Delta High to Low		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[4]	Delta High to Low—low slew		0.057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 35 pF loading.*
3. *The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
4. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1 * V_{CCI} – 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} *is the load capacitance driven by the I/O in pF*
   $d_{T[LH|HL|HLS]}$ *is the worst case delta value from the datasheet in ns/pF.*

Table 2-41 • **A54SX72A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

		–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t_{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t_{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1 * V_{CCI} – 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

176-Pin TQFP

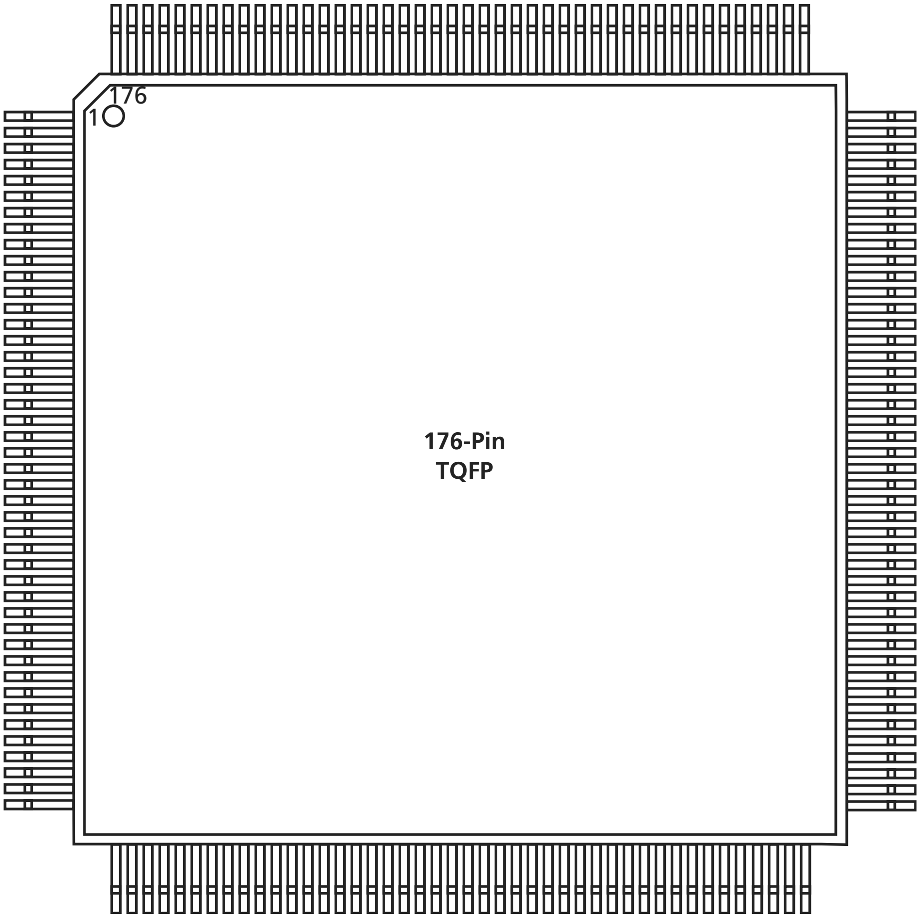


Figure 3-4 • **176-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA

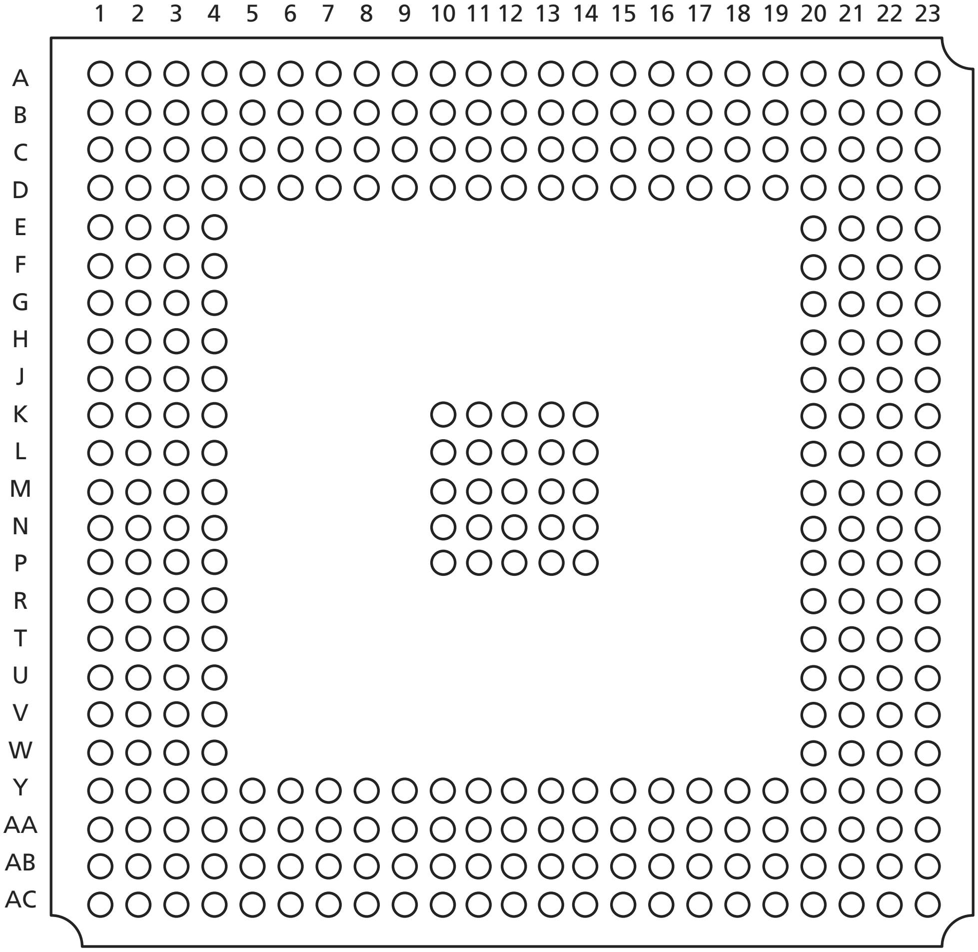


Figure 3-5 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V_{CCA}	V_{CCA}	V_{CCA}
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND
C4	I/O	I/O	I/O
C5	NC	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O
E7	I/O	I/O	QCLKC
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O

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