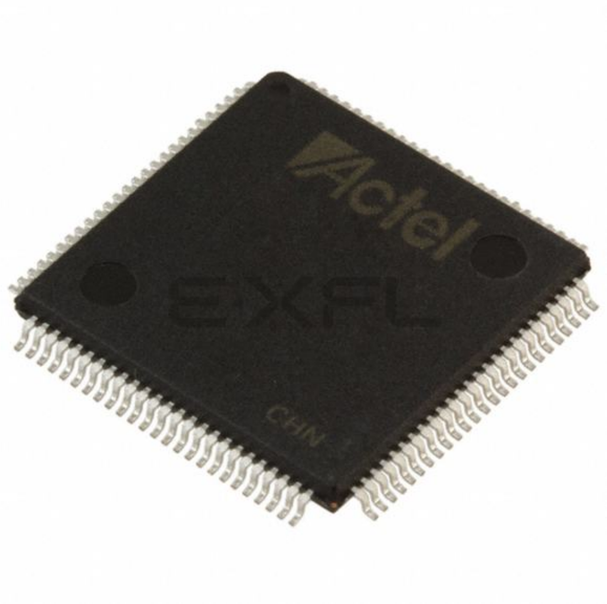


Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-tq100m

Ordering Information

A54SX16A 2 PQ G 208 __

Application (Temperature Range)
Blank = Commercial (0 to +70°)
I = Industrial (-40 to +85°C)
A = Automotive (-40 to +125°C)
M = Military (-55 to +125°C)
B = MIL-STD-883 Class B

Package Lead Count

Package Type
BG = 1.27 mm Plastic Ball Grid Array
FG = 1.0 mm Fine Pitch Ball Grid Array
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
CQ = Ceramic Quad Flat Pack[1]

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard[2]
–F = Approximately 40% Slower than Standard

Part Number
A54SX08A = 12,000 System Gates
A54SX16A = 24,000 System Gates
A54SX32A = 48,000 System Gates
A54SX72A = 108,000 System Gates

Notes:

1. *For more information about the CQFP package options, refer to the* HiRel SX-A datasheet*.*
2. *All –3 speed grades have been discontinued.*

Device Resources

	User I/Os (Including Clock Buffers)							
Device	**208-Pin PQFP**	**100-Pin TQFP**	**144-Pin TQFP**	**176-Pin TQFP**	**329-Pin PBGA**	**144-Pin FBGA**	**256-Pin FBGA**	**484-Pin FBGA**
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: *Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array*

General Description

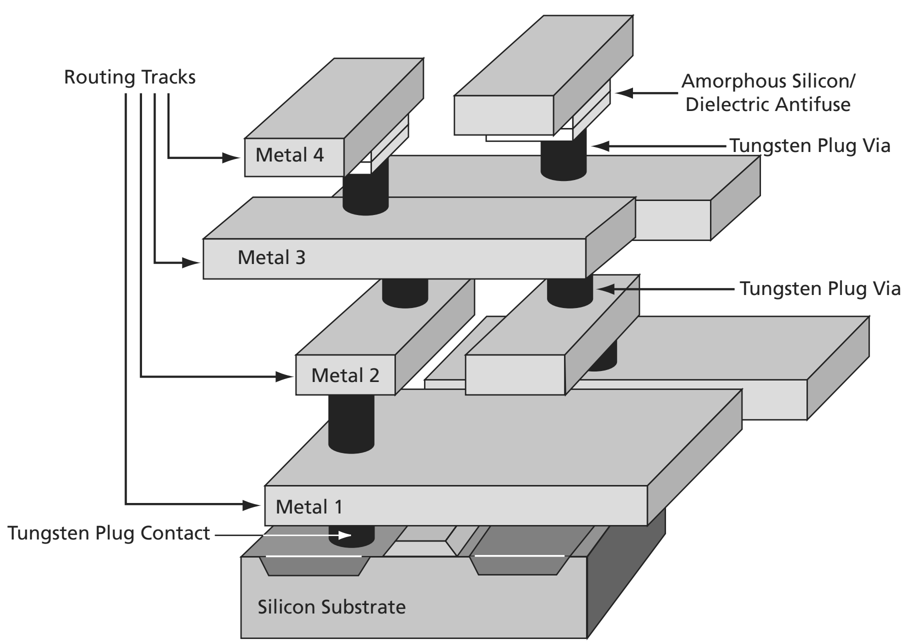
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: *The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.*

Figure 1-1 • **SX-A Family Interconnect Elements**

Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

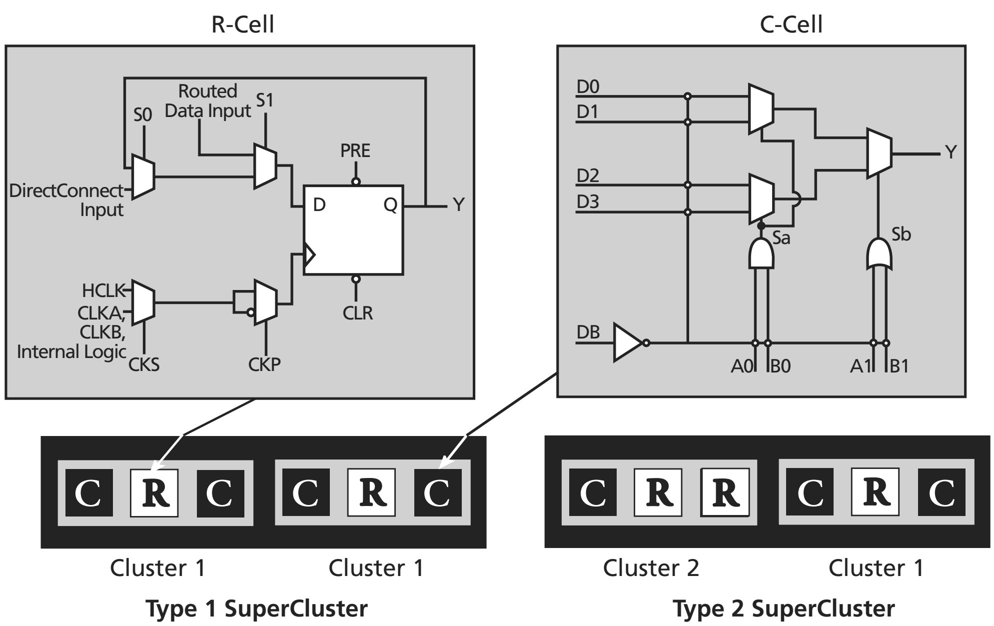


Figure 1-4 • **Cluster Organization**

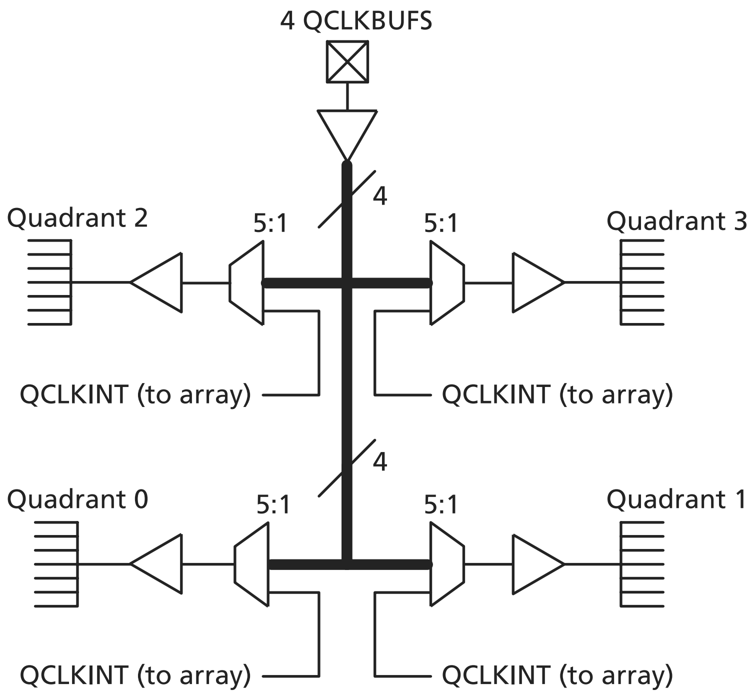


Figure 1-9 • **SX-A QCLK Architecture**

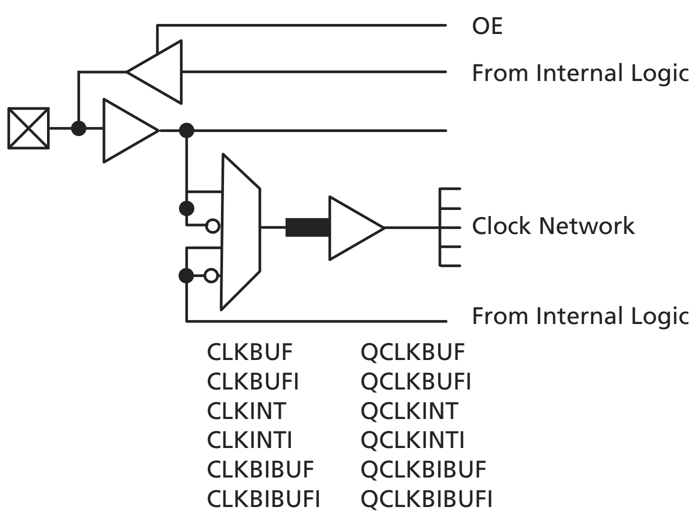


Figure 1-10 • **A54SX72A Routed Clock and QCLK Buffer**

Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel’s integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User’s Guide*.

Related Documents

Application Notes

Global Clock Networks in Actel's Antifuse Devices
http://www.actel.com/documents/GlobalClk_AN.pdf
Using A54SX72A and RT54SX72S Quadrant Clocks
http://www.actel.com/documents/QCLK_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.actel.com/documents/Antifuse_Security_AN.pdf
Actel eX, SX-A, and RTSX-S I/Os
http://www.actel.com/documents/AntifuseIO_AN.pdf
Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications
http://www.actel.com/documents/HotSwapColdSparing_AN.pdf
Programming Antifuse Devices
http://www.actel.com/documents/AntifuseProgram_AN.pdf

Datasheets

HiRel SX-A Family FPGAs
http://www.actel.com/documents/HRSXA_DS.pdf
SX-A Automotive Family FPGAs
http://www.actel.com/documents/SXA_Auto_DS.pdf

User's Guides

Silicon Sculptor User's Guide
http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf

Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

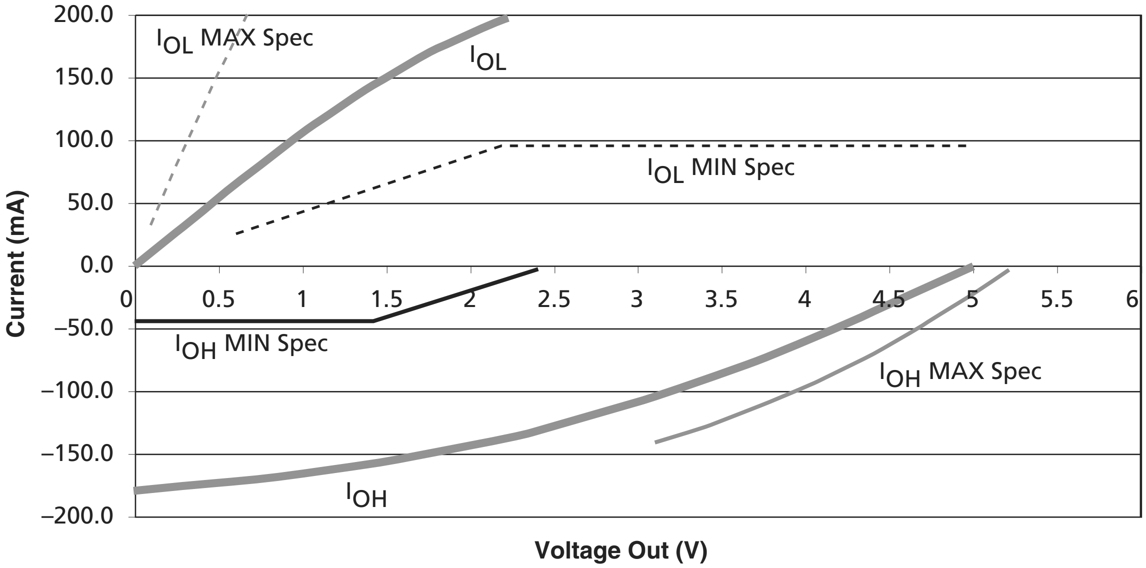


Figure 2-1 • **5 V PCI V/I Curve for SX-A Family**

$I_{OH} = 11.9 * (V_{OUT} – 5.25) * (V_{OUT} + 2.45)$

for $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$I_{OL} = 78.5 * V_{OUT} * (4.4 – V_{OUT})$

for $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • **DC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.25	2.75	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$	–	V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$	–10	+10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$	–	V
V_{OL}	Output Low Voltage	I_{OUT} = 1,500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]		–	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

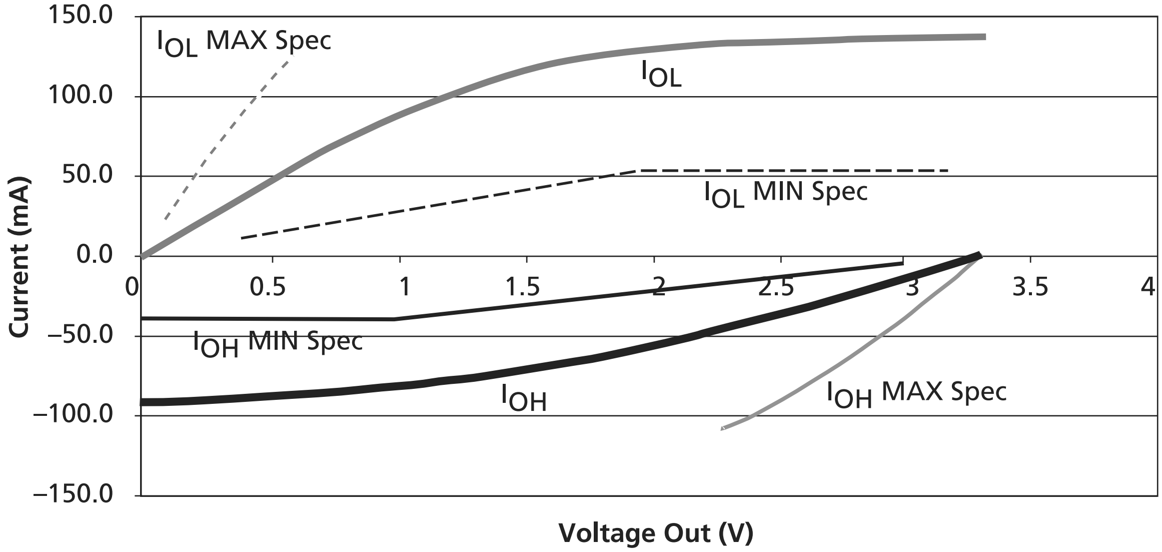


Figure 2-2 • **3.3 V PCI V/I Curve for SX-A Family**

$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$

for $0.7\ V_{CCI} < V_{OUT} < V_{CCI}$

EQ 2-3

$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$

for $0V < V_{OUT} < 0.18\ V_{CCI}$

EQ 2-4

Where:

C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF

C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of CLKA/B in pF

C_{EQHV} = Variable capacitance of HCLK in pF

C_{EQHF} = Fixed capacitance of HCLK in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average CLKA rate in MHz

f_{q2} = Average CLKB rate in MHz

f_{s1} = Average HCLK rate in MHz

m = Number of logic modules switching at fm

n = Number of input buffers switching at fn

p = Number of output buffers switching at fp

q_1 = Number of clock loads on CLKA

q_2 = Number of clock loads on CLKB

r_1 = Fixed capacitance due to CLKA

r_2 = Fixed capacitance due to CLKB

s_1 = Number of clock loads on HCLK

x = Number of I/Os at logic low

y = Number of I/Os at logic high

Table 2-11 • **CEQ Values for SX-A Devices**

	A54SX08A	**A54SX16A**	**A54SX32A**	**A54SX72A**
Combinatorial modules (C_{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C_{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C_{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C_{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C_{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C_{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r_1)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 2-9

$$\theta_{JA} = \frac{T_C - T_A}{P}$$

EQ 2-10

Where:

θ_{JA} = Junction-to-air thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_C = Ambient temperature

P = total power dissipated by the device

Table 2-12 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{JC}	θ_{JA} Still Air	θ_{JA} 1.0 m/s 200 ft./min.	θ_{JA} 2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader[2]	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

1. *The A54SX08A PQ208 has no heat spreader.*
2. *The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.*

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

θ_{JA} = 17.1°C/W is taken from Table 2-12 on page 2-11

T_A = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°C - 125°C}{17.1°C/W} = 1.46\ W$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

T_J = 110°C

T_A = 70°C

From the datasheet:

θ_{JA} = 18.0°C/W

θ_{JC} = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°C - 70°C}{18.0°C/W} = 2.22\ W$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°C - 70°C}{3.00\ W} = 13.33°C/W$$

EQ 2-13

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

θ_{CS} = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Output Buffer Delays

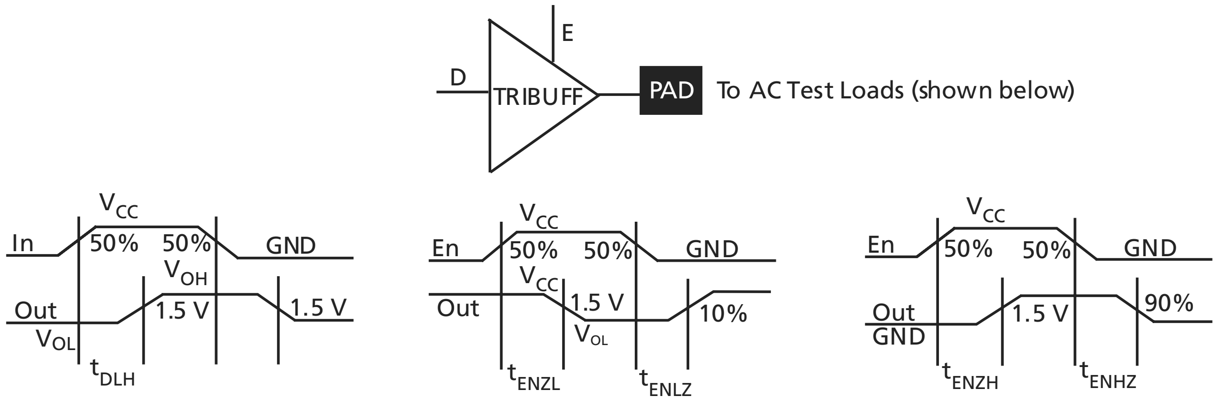


Figure 2-4 • **Output Buffer Delays**

AC Test Loads

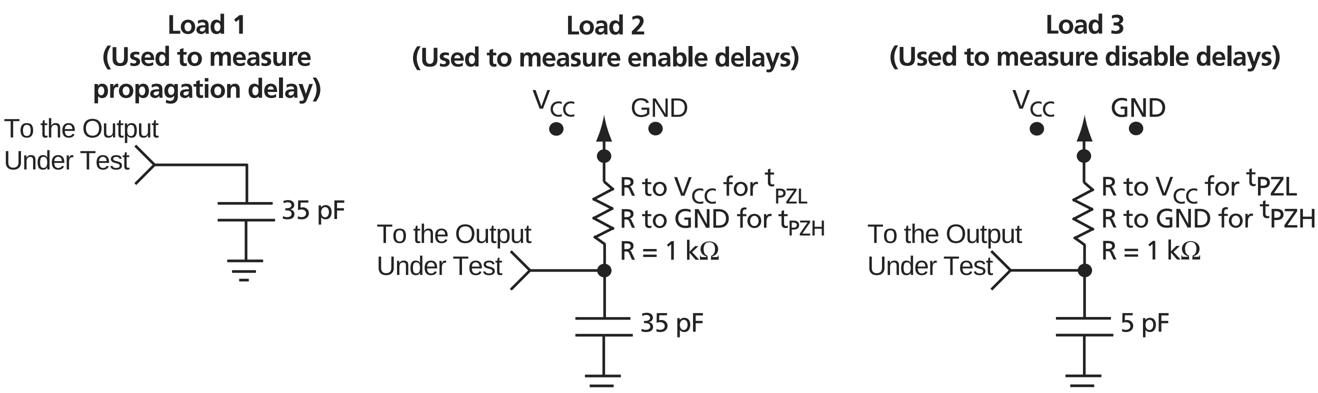


Figure 2-5 • **AC Test Loads**

Table 2-14 • **A54SX08A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.1		1.5	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.6		0.7		0.9	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.8		0.9		1.1		1.5	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t_{IRD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-18 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V LVCMOS Output Module Timing[1,2]										
t_{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d_{TLH}[3]	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d_{THL}[3]	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. *Delays based on 35 pF loading.*
2. *The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-20 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[1]										
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.6		4.2		5.9	ns
d_{TLH}[2]	Delta Low to High		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[2]	Delta High to Low		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.6		4.2		5.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		7.6		8.6		10.1		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.6		4.2		5.9	ns
d_{TLH}	Delta Low to High		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta High to Low		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta High to Low—low slew		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
3. *Delays based on 35 pF loading.*

Table 2-21 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1] Min.	–3 Speed[1] Max.	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std. Speed Min.	Std. Speed Max.	–F Speed Min.	–F Speed Max.	Units
C-Cell Propagation Delays[2]												
t_{PD}	Internal Array Module		0.9		1.0		1.2		1.4		1.9	ns
Predicted Routing Delays[3]												
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t_{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.6		1.9		2.7		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t_{MPW}	Clock Minimum Pulse Width	1.4		1.7		1.9		2.2		3.0		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		0.9		1.0		1.1		1.6	ns
t_{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t_{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		0.9		1.1		1.2		1.4		2.0	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

329-Pin PBGA

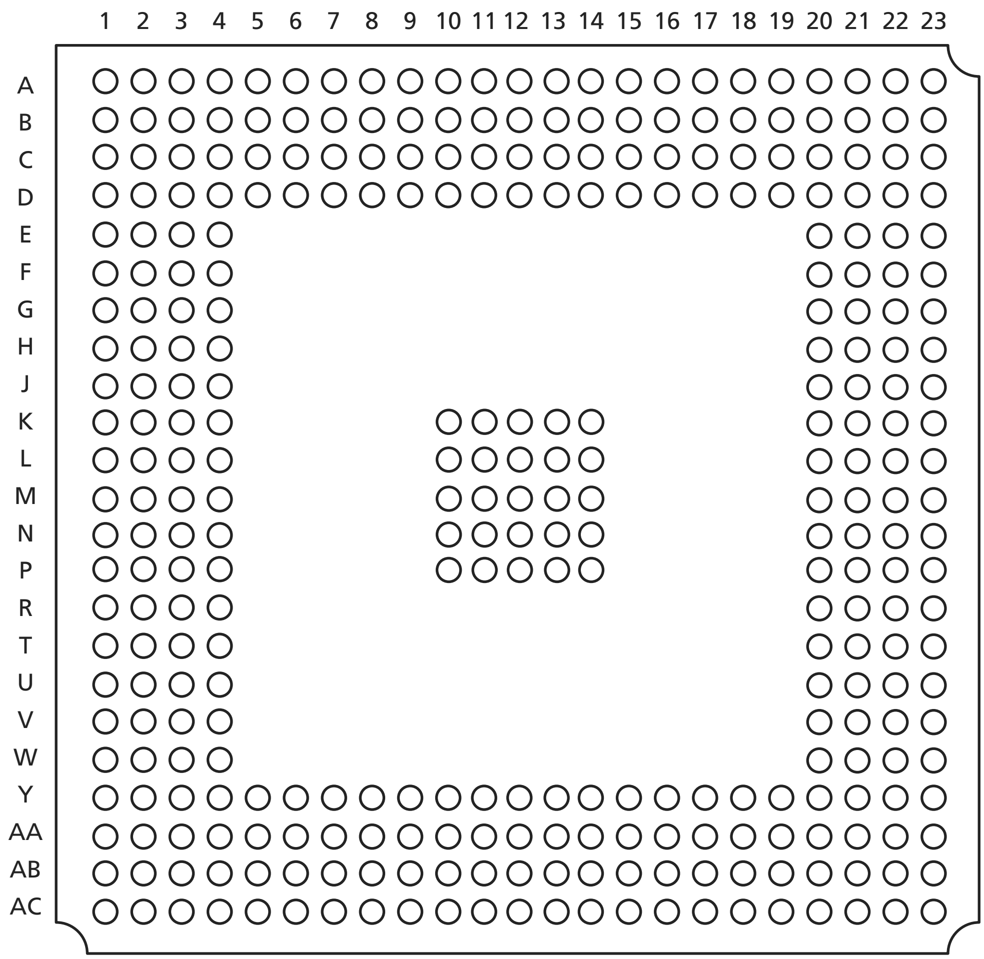


Figure 3-5 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.