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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	1452
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	24000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx16a-tqg144

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Other Architectural Features

Technology

The Actel SX-A family is implemented on a high-voltage, twin-well CMOS process using $0.22 \,\mu/0.25 \,\mu$ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ('on' state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The unique architectural features of the SX-A family enable the devices to operate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Reverse engineering is virtually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept at device power-up.

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

For more information, refer to Actel's *Implementation* of Security in Actel Antifuse FPGAs application note.

I/O Modules

For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pinto-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V_{CCI} is set to 3.3 V on the SX-A input.

Each I/O module has an available power-up resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note *Actel eX, SX-A, and RTSX-S I/Os.* Just slightly before V_{CCA} reaches 2.5 V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Power-Up/Down and Hot Swapping

SX-A I/Os are configured to be hot-swappable, with the exception of 3.3 V PCI. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and can be powered up/down in any order. When the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions

are reached. Table 1-4 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5 V. For more information on power-up and hot-swapping, refer to the application note, Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications.

Function	Description
Input Buffer Threshold Selections	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Flexible Output Driver	 5 V: PCI, TTL 3.3 V: PCI, LVTTL 2.5 V: LVCMOS2 (commercial only)
Output Buffer	 "Hot-Swap" Capability (3.3 V PCI is not hot swappable) I/O on an unpowered device does not sink current Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate; high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V _{CCA} and V _{CCI} can be powered in any order

Table 1-2 • I/O Features

Table 1-3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	bable Slew Rate Control Power-Up Resistor			
TTL, LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down		
3.3 V PCI	No	No. High slew rate only	Pull-up or pull-down		
5 V PCI	Yes	No. High slew rate only	Pull-up or pull-down		

Table 1-4 • Power-Up Time at which I/Os Become Active

Supply Ramp Rate	0.25 V/ μs	0.025 V/ μs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	μs	μs	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2



Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero[®] Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is design management environment. seamlessly а integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Svnplify[®] for Actel from Synplicity[®], ViewDraw[®] for Actel from Mentor Graphics[®], ModelSim[®] HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD[™], and Designer software from Actel. Refer to the Libero IDE flow diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

- 1. Load the .AFM file
- 2. Select the device to be programmed
- 3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V _{CCI}	DC Supply Voltage for I/Os	-0.3 to +6.0	V
V _{CCA}	DC Supply Voltage for Arrays	-0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
V _O	Output Voltage	–0.5 to + V _{CCI} + 0.5	V
T _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
2.5 V Power Supply Range (V _{CCA} and V _{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V _{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V _{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with $V_{CCA} = 2.5 V$

Product	V _{CCI} = 2.5 V	V _{CCI} = 3.3 V	V _{CCI} = 5 V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

V _{CCA}	V _{CCI} *	Maximum Input Tolerance	Maximum Output Drive
2. 5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

Note: *3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH(AC)}	Switching Current High	$0 < V_{OUT} \le 1.4^{-1}$	-44	_	mA
		$1.4 \le V_{OUT} < 2.4^{-1, 2}$	(-44 + (V _{OUT} - 1.4)/0.024)	-	mA
		3.1 < V _{OUT} < V _{CCI} ^{1, 3}	-	EQ 2-1 on page 2-5	_
	(Test Point)	V _{OUT} = 3.1 ³	-	-142	mA
I _{OL(AC)}	Switching Current Low	$V_{OUT} \ge 2.2^{-1}$	95	_	mA
		2.2 > V _{OUT} > 0.55 ¹	(V _{OUT} /0.023)	-	mA
		0.71 > V _{OUT} > 0 ^{1, 3}	-	EQ 2-2 on page 2-5	-
	(Test Point)	V _{OUT} = 0.71 ³	-	206	mA
I _{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	-25 + (V _{IN} + 1)/0.015	-	mA
slew _R	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
slew _F	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Table 2-8 • AC Specifications (5 V PCI Operation)

Notes:

1. Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.

2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.

3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.

4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.



Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules Inputs Switching (n) = Number inputs/4 Outputs Switching (p) = Number of outputs/4 CLKA Loads (q1) = 20% of R-cells CLKB Loads (q2) = 20% of R-cells Load Capacitance (CL) = 35 pF Average Logic Module Switching Rate (fm) = f/10 Average Input Switching Rate (fn) = f/5 Average Output Switching Rate (fp) = f/10 Average CLKA Rate (fq1) = f/2 Average CLKB Rate (fq2) = f/2 Average HCLK Rate (fs1) = f HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the eX, SX-A and RT54SX-S Power Calculator worksheet.

Input Buffer Delays



t INY **C-Cell Delays**



Figure 2-6 • Input Buffer Delays

GND

Figure 2-7 • C-Cell Delays

Cell Timing Characteristics

t_{INY}



Figure 2-8 • Flip-Flops

Table 2-19 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 S	peed	-1 S	peed	Std. S	Speed	–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Ou	tput Module Timing ¹									
t _{DLH}	Data-to-Pad Low to High		2.2		2.4		2.9		4.0	ns
t _{DHL}	Data-to-Pad High to Low		2.3		2.6		3.1		4.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.7		1.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.2		2.4		2.9		4.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.8		3.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.3		2.6		3.1		4.3	ns
d_{TLH}^2	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL O	Dutput Module Timing ³							-		
t _{DLH}	Data-to-Pad Low to High		3.0		3.4		4.0		5.6	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.3		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		10.4		11.8		13.8		19.3	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.6		2.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		18.9		21.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H		3		3.4		4		5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.3		3.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3		3.3		3.9		5.5	ns
d_{TLH}^{2}	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}^2	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}^2	Delta High to Low—low slew		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. Delays based on 10 pF loading and 25 Ω resistance.

2. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate $[V/ns] = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

3. Delays based on 35 pF loading.

Table 2-22 A54SX16A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V,	V _{CCI} = 2.25 V,	T _J = 70°C)
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		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Networ	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Arr	ay Clock Networks			-		-				-		
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-27 A54SX16A Timing Characteristics

		-3 Speed ¹	-2 S	peed	–1 Sp	eed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min. Max	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
5 V PCI Out	put Module Timing ²										
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6	ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.3		1.5		1.7		2.0		2.8	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.2		2.5		2.8		3.3		4.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.0		3.5		3.9		4.6		6.4	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.8		3.2		3.6		4.2		5.9	ns
d _{TLH} ³	Delta Low to High	0.016		0.016		0.02		0.022		0.032	ns/pF
d _{THL} ³	Delta High to Low	0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Out	put Module Timing ⁴								-		
t _{DLH}	Data-to-Pad Low to High	2.2		2.5		2.8		3.3		4.6	ns
t _{DHL}	Data-to-Pad High to Low	2.8		3.2		3.6		4.2		5.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	6.7		7.7		8.7		10.2		14.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.7		3.2		4.5	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4		8.4		9.5		11.0		15.4	ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9		2.2		2.5		2.9		4.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z	3.6		4.2		4.7		5.6		7.8	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.9		3.3		3.9		5.4	ns
d _{TLH} ³	Delta Low to High	0.014		0.017		0.017		0.023		0.031	ns/pF
d _{THL} ³	Delta High to Low	0.023		0.029		0.031		0.037		0.051	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 50 pF loading.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.

Table 2-32 A54SX32A Timing Characteristics

		–3 Spee	ed ¹	-2 S	peed	–1 S	peed	Std. 9	5peed	–F S	peed	
Parameter	Description	Min. M	lax.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2,3}											
t _{DLH}	Data-to-Pad Low to High	3	3.3		3.8		4.2		5.0		7.0	ns
t _{DHL}	Data-to-Pad High to Low	2	2.5		2.9		3.2		3.8		5.3	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	1	1.1		12.8		14.5		17.0		23.8	ns
t _{ENZL}	Enable-to-Pad, Z to L	2	2.4		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	1	1.8		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3	3.3		3.8		4.2		5.0		7.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2	2.1		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2	2.5		2.9		3.2		3.8		5.3	ns
d_{TLH}^{4}	Delta Low to High	0.0	031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}^{4}	Delta High to Low	0.0	017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.0	057		0.06		0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-33 • A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions	V _{CCA} = 2.25 V, V _{CCI} =	= 3.0 V, T _J = 70°C)
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		-3 Speed ¹	-2 Speed	–1 Speed	Std. Speed	-F Speed	
Parameter	Description	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Units
3.3 V PCI O	utput Module Timing ²		•	•			
t _{DLH}	Data-to-Pad Low to High	1.9	2.2	2.4	2.9	4.0	ns
t _{DHL}	Data-to-Pad High to Low	2.0	2.3	2.6	3.1	4.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4	1.7	1.9	2.2	3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H	1.9	2.2	2.4	2.9	4.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5	2.8	3.2	3.8	5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.0	2.3	2.6	3.1	4.3	ns
d _{TLH} ³	Delta Low to High	0.025	0.03	0.03	0.04	0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.015	0.015	0.015	0.025	ns/pF
3.3 V LVTTL	Output Module Timing ⁴			•	•	•	
t _{DLH}	Data-to-Pad Low to High	2.6	3.0	3.4	4.0	5.6	ns
t _{DHL}	Data-to-Pad High to Low	2.6	3.0	3.3	3.9	5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	9.0	10.4	11.8	13.8	19.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2	2.6	2.9	3.4	4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8	18.9	21.3	25.4	34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.6	3.0	3.4	4.0	5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9	3.3	3.7	4.4	6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.6	3.0	3.3	3.9	5.5	ns
d _{TLH} ³	Delta Low to High	0.025	0.03	0.03	0.04	0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.015	0.015	0.015	0.025	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053	0.053	0.067	0.073	0.107	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 10 pF loading and 25 Ω resistance.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.

Table 2-37 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_{J} =	: 70°C)
--	---------

		-3 Sp	beed*	-2 S	-2 Speed		–1 Speed		Std. Speed		-F Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.7		1.9		2.2		2.5		3.5	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.7		2		2.2		2.6		3.6	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 V$, $V_{CCI} = 4.75 V$, $T_J = 70^{\circ}$ C)

		-3 Sp	beed*	-2 S	–2 Speed		peed	Std. Speed		-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{qcksw}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{qcksw}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-39 A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 2.3 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

		-3 Speed ¹ -2 Spe		Speed	-1 Speed	Std. S	Speed	-F Speed		
Parameter	Description	Min. Ma	. Mir	. Max.	Min. Max	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2, 3}									
t _{DLH}	Data-to-Pad Low to High	3.9		4.5	5.1		6.0		8.4	ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.6	4.1		4.8		6.7	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12.	,	14.6	16.5		19.4		27.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8	3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.	3	13.7	15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.9		4.5	5.1		6.0		8.4	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5	2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.6	4.1		4.8		6.7	ns
d_{TLH}^{4}	Delta Low to High	0.03	1	0.037	0.043		0.051		0.071	ns/pF
${\sf d_{THL}}^4$	Delta High to Low	0.01	7	0.017	0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.05	7	0.06	0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.



100-TQFP										
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function							
71	I/O	I/O	I/O							
72	I/O	I/O	I/O							
73	I/O	I/O	I/O							
74	I/O	I/O	I/O							
75	I/O	I/O	I/O							
76	I/O	I/O	I/O							
77	I/O	I/O	I/O							
78	I/O	I/O	I/O							
79	I/O	I/O	I/O							
80	I/O	I/O	I/O							
81	I/O	I/O	I/O							
82	V _{CCI}	V _{CCI}	V _{CCI}							
83	I/O	I/O	I/O							
84	I/O	I/O	I/O							
85	I/O	I/O	I/O							
86	I/O	I/O	I/O							
87	CLKA	CLKA	CLKA							
88	CLKB	CLKB	CLKB							
89	NC	NC	NC							
90	V _{CCA}	V _{CCA}	V _{CCA}							
91	GND	GND	GND							
92	PRA, I/O	PRA, I/O	PRA, I/O							
93	I/O	I/O	I/O							
94	I/O	I/O	I/O							
95	I/O	I/O	I/O							
96	I/O	I/O	I/O							
97	I/O	I/O	I/O							
98	I/O	I/O	I/O							
99	I/O	I/O	I/O							
100	TCK, I/O	TCK, I/O	TCK, I/O							

329-Pin PBGA

		12	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Α	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{0}$
В	C	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
С	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D		$\frac{1}{2}$	0	0	0	0	0	Ο	0	Ο	Ο	0	0	Ο	0	Ο	Ο	0	Ο	0	0	0	0
E) 0	0	0																0	Ö	0	0
г G		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $																				\bigcirc
H		$\frac{1}{2}$	$\overline{0}$	0																$\hat{0}$	0	$\hat{0}$	$\tilde{0}$
J	Ċ	50	Õ	õ																ŏ	ŏ	õ	õ
к	C	00	0	0						Ο	0	Ο	0	0						Ο	Ο	Ο	0
L	C	00	0	0						0	0	0	0	0						0	Ο	0	0
M		$\sum_{i=1}^{i}$	0	0						Õ	Õ	Õ	Õ	Õ						Õ	Õ	Õ	0
N P		$\frac{1}{2}$		0								0								0	0	\bigcirc	\mathbf{O}
R		$\frac{1}{2}$	$\overline{0}$	õ						0	0	0	0	0						0	õ	õ	0
т	C	00	Õ	Õ																Õ	õ	Õ	Õ
U	C	00	0	0																0	0	0	0
V	C	00	0	0																0	0	0	0
W		$\frac{1}{2}$	0	0	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	0	Õ	0	0
Y A A) 0	\mathbf{O}	0	0	0	0	0	0	0	0	0 O	O	O	0	0	0	0	0	0	0	0	0
AB		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $							0	0	0		0									0
AC	$\left(\right)$	$\frac{1}{2}$	$\overline{0}$	0	0	0	0	0	0	0	õ	õ	õ	õ	0	0	0	0	õ	0	õ	õ	õ
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Figure 3-5 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA



Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

	4	484-Pin FBG							
P	A54SX72A	Pin A54SX32A A54SX72A							
Nur	Function	Function	Number						
	I/O	1/0	C19						
I	V _{CCI}	V _{CCI}	C20						
I	I/O	I/O	C21						
I	I/O	I/O	C22						
I	I/O	I/O	C23						
	I/O	I/O	C24						
	I/O	NC*	C25						
l	I/O	NC*	C26						
E	I/O	NC*	D1						
E	TMS	TMS	D2						
E	I/O	I/O	D3						
E	V _{CCI}	V _{CCI}	D4						
E	I/O	NC*	D5						
E	TCK, I/O	TCK, I/O	D6						
E	I/O	I/O	D7						
E	I/O	I/O	D8						
E	I/O	I/O	D9						
E	I/O	I/O	D10						
E	I/O	I/O	D11						
E	QCLKC	I/O	D12						
E	I/O	I/O	D13						
E	I/O	I/O	D14						
E	I/O	I/O	D15						
E	I/O	I/O	D16						
E	I/O	I/O	D17						
	I/O	I/O	D18						
	I/O	I/O	D19						
	I/O	I/O	D20						
	V _{CCI}	V _{CCI}	D21						
	GND	GND	D22						
F	I/O	I/O	D23						
F	I/O	I/O	D24						
F	I/O	NC*	D25						
F	I/O	NC*	D26						
F	I/O	NC*	E1						

484-Pin FBGA								
Pin Number	A54SX32A Function	A54SX72A Function						
E2	NC*	I/O						
E3	I/O	I/O						
E4	I/O	I/O						
E5	GND	GND						
E6	TDI, IO	TDI, IO						
E7	I/O	I/O						
E8	I/O	I/O						
E9	I/O	I/O						
E10	I/O	I/O						
E11	I/O	I/O						
E12	I/O	I/O						
E13	V _{CCA}	V _{CCA}						
E14	CLKB	CLKB						
E15	I/O	I/O						
E16	I/O	I/O						
E17	I/O	I/O						
E18	I/O	I/O						
E19	I/O	I/O						
E20	I/O	I/O						
E21	I/O	I/O						
E22	I/O	I/O						
E23	I/O	I/O						
E24	I/O	I/O						
E25	V _{CCI}	V _{CCI}						
E26	GND	GND						
F1	V _{CCI}	V _{CCI}						
F2	NC*	I/O						
F3	NC*	I/O						
F4	I/O	I/O						
F5	I/O	I/O						
F22	I/O	I/O						
F23	I/O	I/O						
F24	I/O	I/O						
F25	I/O	I/O						
F26	NC*	I/O						

484-Pin FBGA								
Pin Number	A54SX32A Function	A54SX72A Function						
G1	NC*	I/O						
G2	NC*	I/O						
G3	NC*	I/O						
G4	I/O	I/O						
G5	I/O	I/O						
G22	I/O	ΙΟ						
G23	V _{CCA}	V _{CCA}						
G24	I/O	I/O						
G25	NC*	I/O						
G26	NC*	I/O						
H1	NC*	I/O						
H2	NC*	I/O						
H3	I/O	I/O						
H4	I/O	I/O						
H5	I/O	I/O						
H22	I/O	I/O						
H23	I/O	Ι/O						
H24	I/O	Ι/O						
H25	NC*	I/O						
H26	NC*	I/O						
J1	NC*	I/O						
J2	NC*	I/O						
J3	I/O	I/O						
J4	I/O	I/O						
J5	I/O	I/O						
J22	I/O	Ι/O						
J23	I/O	Ι/O						
J24	I/O	Ι/O						
J25	V _{CCI}	V _{CCI}						
J26	NC*	I/O						
K1	I/O	I/O						
K2	V _{CCI}	V _{CCI}						
К3	I/O	I/O						
K4	I/O	I/O						
K5	V _{CCA}	V _{CCA}						

Actel°

SX-A Family FPGAs

Note: *These pins must be left floating on the A54SX32A device.