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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	329-BBGA
Supplier Device Package	329-PBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-1bg329

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General Description

Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 μm / 0.25 μm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements



Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6	٠	Boundary-Scan Pin Configurations an	d
		Functions	

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test- Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function				
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)				
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up				
Reserve Probe	Keeps pins from being used or regular I/O				

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.



Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High. When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

JTAG Mode	TRST ¹	Security Fuse Programmed	PRA, PRB ²	TDI, TCK, TDO ²
Dedicated	Low	No User I/O ³		JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O ³	User I/O ³
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved)

Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.

2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.





Figure 2-2 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

Figure 2-2 • 3.3 V PCI V/I Curve for SX-A Family

 $I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$

for 0.7 $V_{CCI} < V_{OUT} < V_{CCI}$

 $I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$ for 0V < V_{OUT} < 0.18 V_{CCI}

EQ 2-3

EQ 2-4

Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

- 1. Estimate the power consumption of the application.
- 2. Calculate the maximum power allowed for the device and package.
- 3. Compare the estimated power and maximum power values.

Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 2-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{DC} = I_{Standby} * V_{CCA}$$

EQ 2-6

Note: For other combinations of temperature and voltage settings, refer to the eX, SX-A and RT54SX-S Power Calculator.

AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{C-cells} + P_{R-cells} + P_{CLKA} + P_{CLKB} + P_{HCLK} + P_{Output Buffer} + P_{Input Buffer}$$

EQ 2-7

or:

 $P_{AC} = V_{CCA}^{2} * [(m * C_{EQCM} * fm)_{C-cells} + (m * C_{EQSM} * fm)_{R-cells} + (n * C_{EQI} * f_{n})_{Input Buffer} + (p * (C_{EQO} + C_{L}) * f_{p})_{Output Buffer} + (0.5 * (q_{1} * C_{EQCR} * f_{q1}) + (r_{1} * f_{q1}))_{CLKA} + (0.5 * (q_{2} * C_{EQCR} * f_{q2}) + (r_{2} * f_{q2}))_{CLKB} + (0.5 * (s_{1} * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))_{HCLK}]$

EQ 2-8

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction to be higher than the ambient, case, or board temperatures. EQ 2-9 and EQ 2-10 give the relationship between thermal resistance, temperature gradient and power.

 $\theta_{JA} = \frac{T_J - T_A}{P}$ EQ 2-9 $\theta_{JA} = \frac{T_C - T_A}{P}$

EQ 2-10

Where:

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_{C} = Ambient temperature
- P = total power dissipated by the device

Table 2-12 • Package Thermal Characteristics

				${\sf A}{\sf L}^{{\boldsymbol heta}}$		
Package Type	Pin Count	οι ^θ	Still Air	1.0 m/s 200 ft./min.	2.5 m/s 500 ft./min.	Units
Thin Quad Flat Pack (TQFP)	100	14	33.5	27.4	25	°C/W
Thin Quad Flat Pack (TQFP)	144	11	33.5	28	25.7	°C/W
Thin Quad Flat Pack (TQFP)	176	11	24.7	19.9	18	°C/W
Plastic Quad Flat Pack (PQFP) ¹	208	8	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader ²	208	3.8	16.2	13.3	11.9	°C/W
Plastic Ball Grid Array (PBGA)	329	3	17.1	13.8	12.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	18	14.7	13.6	°C/W

Notes:

1. The A54SX08A PQ208 has no heat spreader.

2. The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}$$
C/W is taken from Table 2-12 on page 2-11

 $T_A = 125$ °C is the maximum limit of ambient (from the datasheet)

Max. Allowed Power =
$$\frac{\text{Max Junction Temp - Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_{J} = 110^{\circ}C$$

 $T_{A} = 70^{\circ}C$

From the datasheet:

 $\theta_{JA} = 18.0^{\circ}C/W$ $\theta_{JC} = 3.2^{\circ}C/W$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{Max Junction Temp - Max. Ambient Temp}{P} = \frac{110^{\circ}C - 70^{\circ}C}{3.00 W} = 13.33^{\circ}C/W$$

EQ 2-13



To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

 $\theta_{CS} = 0.37^{\circ}C/W$

 thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

 θ_{SA} = thermal resistance of the heat sink in °C/W

 $\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$ EQ 2-15 $\theta_{SA} = 13.33^{\circ}C/W - 3.20^{\circ}C/W - 0.37^{\circ}C/W$

$$\theta_{SA} = 9.76^{\circ}C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

SX-A Timing Model



Note: *Values shown for A54SX72A, –2, worst-case commercial conditions at 5 V PCI with standard place-and-route. Figure 2-3 • SX-A Timing Model

Sample Path Calculations

Hardwired Clock

External Setup	=	(t _{INYH} + t _{RD1} + t _{SUD}) – t _{HCKH}
	=	0.6 + 0.3 + 0.8 - 1.8 = - 0.1 ns
Clock-to-Out (Pad-to-Pad)	=	t _{HCKH} + t _{RCO} + t _{RD1} + t _{DHL}
	=	1.8 + 0.8 + 0.3 + 3.9 = 6.8 ns

Routed Clock

External Setup	$= (t_{INYH} + t_{RD1} + t_{SUD}) - t_{RC}$	СКН
	= 0.6 + 0.3 + 0.8 - 3.0 = -1.	3 ns
Clock-to-Out (Pad-to-Pad	$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DH}$	L
	= 3.0 + 0.8 + 0.3 + 3.9 = 8.0) ns

Table 2-21 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		–3 Speed ¹		-2 Speed		–1 Speed		Std. Speed		-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	agation Delays ²											
t _{PD}	Internal Array Module		0.9		1.0		1.2		1.4		1.9	ns
Predicted R	outing Delays ³											
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		1.7		2		2.2		2.6		3.6	ns
R-Cell Timin	ng											
t _{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.8		1.0		1.4	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.6		1.9		2.7		ns
t _{recasyn}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Minimum Pulse Width	1.4		1.7		1.9		2.2		3.0		ns
Input Modu	le Propagation Delays											
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.5		0.6		0.7		0.8		1.1	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		0.8		0.9		1.0		1.1		1.6	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.5		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.0		1.4	ns
t _{INYH}	lnput Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.8		1.0		1.4	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		0.9		1.1		1.2		1.4		2.0	ns

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-21 A54SX16A Timing Characteristics (Continued)

-		
(Moust Case Commonsial Conditions	V 225V	
(worst-case commercial conditions	. VccA = 2.23 V	$V_{CC} = 3.0 V_{c} = 10^{\circ} C_{c}$
·····	- CCA	,

		-3 Sp	beed ¹	-2 S	peed	-1 S	peed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V PCI		0.7		0.8		0.9		1.1		1.5	ns
t _{INYH}	Input Data Pad to Y High 5 V TTL		0.5		0.5		0.6		0.7		0.9	ns
t _{INYL}	Input Data Pad to Y Low 5 V TTL		0.7		0.8		0.9		1.1		1.5	ns
Input Modu	le Predicted Routing Delays ²											
t _{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t _{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t _{IRD3}	FO = 3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t _{IRD4}	FO = 4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t _{IRD8}	FO = 8 Routing Delay		1.2		1.4		1.5		0.8		2.5	ns
t _{IRD12}	FO = 12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns

Notes:

1. All –3 speed grades have been discontinued.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-23 • A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions V _{CC}	_A = 2.25 V, V _{CCl} = 3.0 V, T _J = 70°C)
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		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated ((Hardwired) Array Clock Netwo	rks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.3		1.5		2.2	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.6	ns
t _{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.5		2.1	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.4		1.7		2.3	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.7	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-29 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _c	_{CCI} = 2.25 V, T _J = 70°C)
----------------------------------	---------------------------------------------	-------------------------------------------------

		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated	(Hardwired) Array Clock Netwo	'ks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.9		3.4		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.4		2.7		3.2		4.4	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.6	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.9		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.0	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.9		1.0		1.2		1.4		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.4		1.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-38 • A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 V$, $V_{CCI} = 4.75 V$, $T_J = 70^{\circ}$ C)

		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t _{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t _{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t _{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t _{qcksw}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t _{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t _{qcksw}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: *All –3 speed grades have been discontinued.

Table 2-40 A54SX72A Timing Characteristics

(Worst-Case Commercial	Conditions $V_{CCA} = 2.25$	$V_{V_{CCI}} = 3.0$	$I_{1} = 70^{\circ}C$
(.,.,,

		-3 Speed ¹	–2 Spee	ed	–1 Spee	ed	Std. 9	Speed	–F S	peed	
Parameter	Description	Min. Max.	Min. M	ax.	Min. M	ax.	Min.	Max.	Min.	Max.	Units
3.3 V PCI O	utput Module Timing ²										
t _{DLH}	Data-to-Pad Low to High	2.3	2	.7	3	.0		3.6		5.0	ns
t _{DHL}	Data-to-Pad High to Low	2.5	2	.9	3	.2		3.8		5.3	ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4	1	.7	1	.9		2.2		3.1	ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2	.7	3	.0		3.6		5.0	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5	2	.8	3	.2		3.8		5.3	ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5	2	.9	3	.2		3.8		5.3	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0	015	0.0	015		0.015		0.025	ns/pF
3.3 V LVTTL	3.3 V LVTTL Output Module Timing ⁴										
t _{DLH}	Data-to-Pad Low to High	3.2	3	.7	4	.2		5.0		6.9	ns
t _{DHL}	Data-to-Pad High to Low	3.2	3	.7	4	.2		4.9		6.9	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	10.3	11	1.9	13	3.5		15.8		22.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2	2	.6	2	.9		3.4		4.8	ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8	18	3.9	2	1.3		25.4		34.9	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.2	3	.7	4	.2		5.0		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9	3	.3	3	.7		4.4		6.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.2	3	.7	4	.2		4.9		6.9	ns
d _{TLH} ³	Delta Low to High	0.025	0.	03	0.	03		0.04		0.045	ns/pF
d _{THL} ³	Delta High to Low	0.015	0.0)15	0.0	015		0.015		0.025	ns/pF
d _{THLS} ³	Delta High to Low—low slew	0.053	0.0)53	0.0	067		0.073		0.107	ns/pF

Notes:

1. All –3 speed grades have been discontinued.

2. Delays based on 10 pF loading and 25 Ω resistance.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

4. Delays based on 35 pF loading.



176-Pin TQFP



Figure 3-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA



Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.



256-Pin FBGA



Figure 3-7 • 256-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

Previous Version	Changes in Current Version (v5.3)	Page
v4.0	Table 2-12 was updated.	2-11
(continued)	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The ""Clock Resources" section" was updated	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23

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