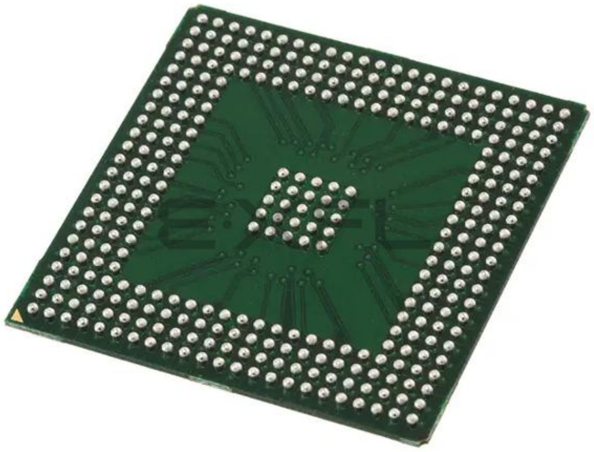
# Microchip Technology - A54SX32A-1BG329M Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2880 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 249 |
| Number of Gates | 48000 |
| Voltage - Supply | 2.25V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TC) |
| Package / Case | 329-BBGA |
| Supplier Device Package | 329-PBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-1bg329m |

## Temperature Grade Offering

| **Package** | **A54SX08A** | **A54SX16A** | **A54SX32A** | **A54SX72A** |
|---|---|---|---|---|
| PQ208 | C,I,A,M | C,I,A,M | C,I,A,M | C,I,A,M |
| TQ100 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| TQ176 | | | C,I,M | |
| BG329 | | | C,I,M | |
| FG144 | C,I,A,M | C,I,A,M | C,I,A,M | |
| FG256 | | C,I,A,M | C,I,A,M | C,I,A,M |
| FG484 | | | C,I,M | C,I,A,M |
| CQ208 | | | C,M,B | C,M,B |
| CQ256 | | | C,M,B | C,M,B |

***Notes:***

1. *C = Commercial*
2. *I = Industrial*
3. *A = Automotive*
4. *M = Military*
5. *B = MIL-STD-883 Class B*
6. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
7. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

## Speed Grade and Temperature Grade Matrix

| | **F** | **Std** | **–1** | **–2** | **–3** |
|---|---|---|---|---|---|
| Commercial | ✓ | ✓ | ✓ | ✓ | Discontinued |
| Industrial | | ✓ | ✓ | ✓ | Discontinued |
| Automotive | | ✓ | | | |
| Military | | ✓ | ✓ | | |
| MIL-STD-883B | | ✓ | ✓ | | |

***Notes:***

1. *For more information regarding automotive products, refer to the* SX-A Automotive Family FPGAs *datasheet.*
2. *For more information regarding Mil-Temp and ceramic packages, refer to the* HiRel SX-A Family FPGAs *datasheet.*

Contact your Actel Sales representative for more information on availability.

## Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Device*s and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

*Table 1-1* • **SX-A Clock Resources**

| | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---|---|---|---|---|
| Routed Clocks (CLKA, CLKB) | 2 | 2 | 2 | 2 |
| Hardwired Clocks (HCLK) | 1 | 1 | 1 | 1 |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0 | 0 | 0 | 4 |

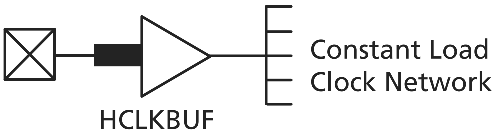


*Figure 1-7* • **SX-A HCLK Clock Buffer**

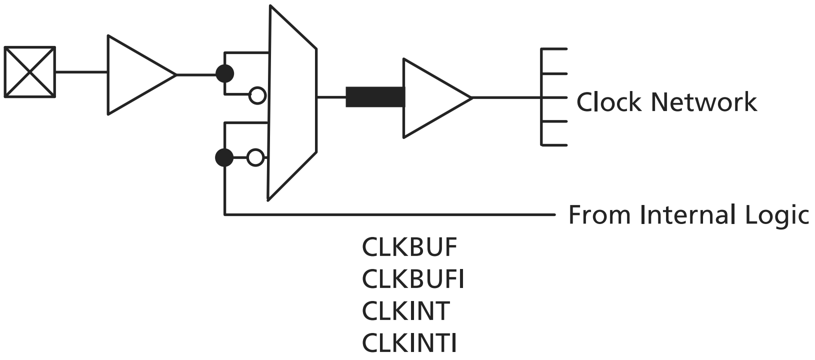


*Figure 1-8* • **SX-A Routed Clock Buffer**

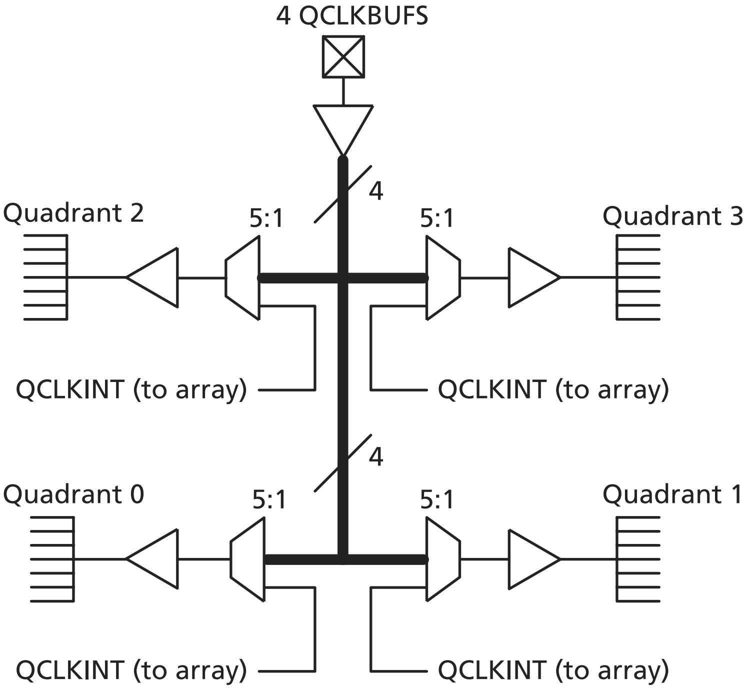


*Figure 1-9* • **SX-A QCLK Architecture**

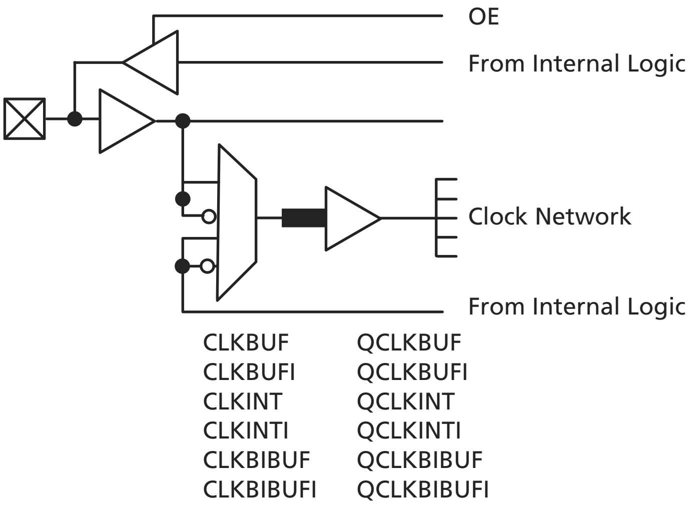


*Figure 1-10* • **A54SX72A Routed Clock and QCLK Buffer**

## Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

### Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

*Figure 1-12* • **Device Selection Wizard**

*Table 1-5* • **Reserve Pin Definitions**

| Pin | Function |
|---|---|
| Reserve JTAG | Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS) |
| Reserve JTAG Test Reset | Regular I/O or JTAG reset with an internal pull-up |
| Reserve Probe | Keeps pins from being used or regular I/O |

### Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to $V_{CCI}$ should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

*Table 1-6* • **Boundary-Scan Pin Configurations and Functions**

| Mode | Designer "Reserve JTAG" Selection | TAP Controller State |
|---|---|---|
| Dedicated (JTAG) | Checked | Any |
| Flexible (User I/O) | Unchecked | Test-Logic-Reset |
| Flexible (JTAG) | Unchecked | Any EXCEPT Test-Logic-Reset |

### TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

## Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

# Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

# Electrical Specifications

*Table 2-5* • **3.3 V LVTTL and 5 V TTL Electrical Specifications**

| **Symbol** | **Parameter** | | **Commercial** | | **Industrial** | | **Units** |
|---|---|---|---|---|---|---|---|
| | | | **Min.** | **Max.** | **Min.** | **Max.** | |
| $V_{OH}$ | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 0.9 $V_{CCI}$ | | 0.9 $V_{CCI}$ | | V |
| | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –8 mA) | 2.4 | | 2.4 | | V |
| $V_{OL}$ | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{CCI}$ = Minimum<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 12 mA) | | 0.4 | | 0.4 | V |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | 5.75 | 2.0 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

*Table 2-6* • **2.5 V LVCMOS2 Electrical Specifications**

| **Symbol** | **Parameter** | | **Commercial** | | **Industrial** | | **Units** |
|---|---|---|---|---|---|---|---|
| | | | **Min.** | **Max.** | **Min.** | **Max.** | |
| $V_{OH}$ | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –100 µA) | 2.1 | | 2.1 | | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = –1 mA) | 2.0 | | 2.0 | | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ =–-2 mA) | 1.7 | | 1.7 | | V |
| $V_{OL}$ | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 100 µA) | | 0.2 | | 0.2 | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1 mA) | | 0.4 | | 0.4 | V |
| | $V_{DD}$ = MIN,<br>$V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 2 mA) | | 0.7 | | 0.7 | V |
| $V_{IL}$ | Input Low Voltage, $V_{OUT} \leq V_{VOL(max)}$ | | -0.3 | 0.7 | -0.3 | 0.7 | V |
| $V_{IH}$ | Input High Voltage, $V_{OUT} \geq V_{VOH(min)}$ | | 1.7 | 5.75 | 1.7 | 5.75 | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current, $V_{IN} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_F$ | Input Transition Time $t_R$, $t_F$ | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| $I_{CC}$ | Standby Current | | | 10 | | 20 | mA |
| IV Curve* | Can be derived from the IBIS model on the web. | | | | | | |

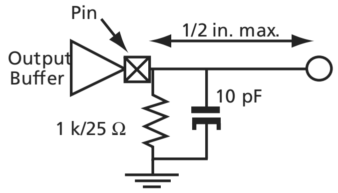
***Note:*** **The IBIS model can be found at http://www.actel.com/download/ibis/default.aspx.*

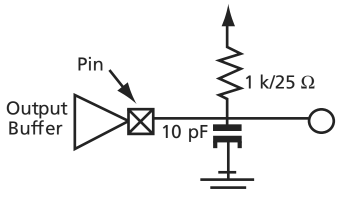
*Table 2-10* • **AC Specifications (3.3 V PCI Operation)**

| **Symbol** | **Parameter** | **Condition** | **Min.** | **Max.** | **Units** |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CCI}$ [1] | $-12V_{CCI}$ | – | mA |
| | | $0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}$ [1] | $(-17.1(V_{CCI} - V_{OUT}))$ | – | mA |
| | | $0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2] | – | EQ 2-3 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}$ [2] | – | $-32V_{CCI}$ | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{CCI} > V_{OUT} \geq 0.6V_{CCI}$ [1] | $16V_{CCI}$ | – | mA |
| | | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1] | $(26.7V_{OUT})$ | – | mA |
| | | $0.18V_{CCI} > V_{OUT} > 0$ [1, 2] | – | EQ 2-4 on page 2-7 | – |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}$ [2] | – | $38V_{CCI}$ | mA |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | – | mA |
| $I_{CH}$ | High Clamp Current | $V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$ | $25 + (V_{IN} - V_{CCI} - 1)/0.015$ | – | mA |
| $slew_R$ | Output Rise Slew Rate | $0.2V_{CCI}$ - $0.6V_{CCI}$ load [3] | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate | $0.6V_{CCI}$ - $0.2V_{CCI}$ load [3] | 1 | 4 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*





## Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

### Estimating Power Dissipation

The total power dissipation for the SX-A family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 2-5*

### DC Power Dissipation

The power due to standby current is typically a small component of the overall power. An estimation of DC power dissipation under typical conditions is given by:

$$P_{DC} = I_{Standby} * V_{CCA}$$

*EQ 2-6*

Note: For other combinations of temperature and voltage settings, refer to the *eX, SX-A and RT54SX-S Power Calculator*.

### AC Power Dissipation

The power dissipation of the SX-A family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{C\text{-cells}} + P_{R\text{-cells}} + P_{CLKA} + P_{CLKB} + P_{HCLK} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 2-7*

or:

$$\begin{aligned} P_{AC} = {} & V_{CCA}^2 * [(m * C_{EQCM} * fm)_{C\text{-cells}} + (m * C_{EQSM} * fm)_{R\text{-cells}} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} \\ & + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{CLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{CLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + \\ & (C_{EQHF} * f_{s1}))_{HCLK}] \end{aligned}$$

*EQ 2-8*

# Timing Characteristics

*Table 2-14* • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions, $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **C-Cell Propagation Delays[1]** | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module | | 0.9 | | 1.1 | | 1.2 | | 1.7 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | | | |
| $t_{DC}$ | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 0.8 | | 0.9 | | 1 | | 1.4 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 1.4 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{RD12}$ | FO = 12 Routing Delay | | 2 | | 2.2 | | 2.6 | | 3.6 | ns |
| **R-Cell Timing** | | | | | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.6 | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.4 | | 1.5 | | 1.8 | | 2.5 | | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | 0.3 | | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{MPW}$ | Clock Pulse Width | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | |
| $t_{INYH}$ | Input Data Pad to Y High 2.5 V LVCMOS | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 2.5 V LVCMOS | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V PCI | | 0.6 | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V PCI | | 0.7 | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{INYH}$ | Input Data Pad to Y High 3.3 V LVTTL | | 0.7 | | 0.7 | | 0.9 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad to Y Low 3.3 V LVTTL | | 1.0 | | 1.1 | | 1.3 | | 1.8 | ns |

***Notes:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

*Table 2-17* • **A54SX08A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| Parameter | Description | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.3 | | 1.5 | | 2.3 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.5 | | 0.8 | ns |
| $t_{HP}$ | Minimum Period | 3.2 | | 3.6 | | 4.2 | | 5.8 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 313 | | 278 | | 238 | | 172 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.6 | | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 1.0 | | 1.1 | | 1.5 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |

*Table 2-24* • **A54SX16A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ =4.75 V, $T_J$ = 70°C)**

| **Parameter** | **Description** | **–3 Speed*** | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **–F Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.0 | | 1.1 | | 1.2 | | 1.5 | | 2.2 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.3 | | 0.4 | | 0.4 | | 0.7 | ns |
| $t_{HP}$ | Minimum Period | 2.8 | | 3.4 | | 3.8 | | 4.4 | | 6.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 357 | | 294 | | 263 | | 227 | | 167 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.0 | | 1.2 | | 1.3 | | 1.6 | | 2.2 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.1 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.0 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-38* • **A54SX72A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed* | | –2 Speed | | –1 Speed | | Std. Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (Pad to R-cell Input) | | 1.6 | | 1.8 | | 2.1 | | 2.4 | | 3.8 | ns |
| $t_{HCKL}$ | Input High to Low (Pad to R-cell Input) | | 1.6 | | 1.9 | | 2.1 | | 2.5 | | 3.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.3 | ns |
| $t_{HP}$ | Minimum Period | 3.0 | | 3.4 | | 4.0 | | 4.6 | | 6.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 333 | | 294 | | 250 | | 217 | | 156 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.9 | ns |
| $t_{RCKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{RCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 2.5 | | 2.9 | | 3.2 | | 3.8 | | 5.3 | ns |
| $t_{RCKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 3.0 | | 3.4 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{RCKH}$ | Input Low to High (100% Load) (Pad to R-cell Input) | | 2.6 | | 3.0 | | 3.4 | | 3.9 | | 5.5 | ns |
| $t_{RCKL}$ | Input High to Low (100% Load) (Pad to R-cell Input) | | 3.2 | | 3.6 | | 4.1 | | 4.8 | | 6.8 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 1.5 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 1.9 | | 2.2 | | 2.5 | | 3.0 | | 4.1 | ns |
| **Quadrant Array Clock Networks** | | | | | | | | | | | | |
| $t_{QCKH}$ | Input Low to High (Light Load) (Pad to R-cell Input) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| $t_{QCHKL}$ | Input High to Low (Light Load) (Pad to R-cell Input) | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{QCKH}$ | Input Low to High (50% Load) (Pad to R-cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{QCHKL}$ | Input High to Low (50% Load) (Pad to R-cell Input) | | 1.4 | | 1.7 | | 1.9 | | 2.2 | | 3.1 | ns |

***Note:*** **All –3 speed grades have been discontinued.*

*Table 2-41* • **A54SX72A Timing Characteristics**
**(Worst-Case Commercial Conditions $V_{CCA}$ = 2.25 V, $V_{CCI}$ = 4.75 V, $T_J$ = 70°C)**

| **Parameter** | **Description** | **–3 Speed[1]** | | **–2 Speed** | | **–1 Speed** | | **Std. Speed** | | **–F Speed** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| **5 V PCI Output Module Timing[2]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.0 | | 3.5 | | 3.9 | | 4.6 | | 6.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.4 | | 3.9 | | 4.4 | | 5.1 | | 7.2 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.016 | | 0.016 | | 0.02 | | 0.022 | | 0.032 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.026 | | 0.03 | | 0.032 | | 0.04 | | 0.052 | ns/pF |
| **5 V TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low—low slew | | 7.4 | | 8.5 | | 9.7 | | 11.4 | | 15.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{ENZLS}$ | Enable-to-Pad, Z to L—low slew | | 7.4 | | 8.4 | | 9.5 | | 11.0 | | 15.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.4 | | 2.8 | | 3.1 | | 3.7 | | 5.1 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.6 | | 4.2 | | 4.7 | | 5.6 | | 7.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | ns |
| $d_{TLH}$[3] | Delta Low to High | | 0.014 | | 0.017 | | 0.017 | | 0.023 | | 0.031 | ns/pF |
| $d_{THL}$[3] | Delta High to Low | | 0.023 | | 0.029 | | 0.031 | | 0.037 | | 0.051 | ns/pF |
| $d_{THLS}$[3] | Delta High to Low—low slew | | 0.043 | | 0.046 | | 0.057 | | 0.066 | | 0.089 | ns/pF |

***Notes:***

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the $V_{CCI}$ value into the following equation:*
   *Slew Rate [V/ns] = (0.1*$V_{CCI}$ – 0.9*$V_{CCI}$)/ ($C_{load}$ * $d_{T[LH|HL|HLS]}$)*
   *where $C_{load}$ is the load capacitance driven by the I/O in pF*
   *$d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.*
4. *Delays based on 35 pF loading.*

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 1 | GND | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O | I/O |
| 4 | NC | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O | I/O |
| 6 | NC | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O | I/O |
| 10 | I/O | I/O | I/O | I/O |
| 11 | TMS | TMS | TMS | TMS |
| 12 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 13 | I/O | I/O | I/O | I/O |
| 14 | NC | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O | I/O |
| 17 | NC | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O | GND |
| 19 | I/O | I/O | I/O | $V_{CCA}$ |
| 20 | NC | I/O | I/O | I/O |
| 21 | I/O | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O | I/O |
| 23 | NC | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O | I/O |
| 25 | NC | NC | NC | I/O |
| 26 | GND | GND | GND | GND |
| 27 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 28 | GND | GND | GND | GND |
| 29 | I/O | I/O | I/O | I/O |
| 30 | TRST, I/O | TRST, I/O | TRST, I/O | TRST, I/O |
| 31 | NC | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O | I/O |
| 35 | NC | I/O | I/O | I/O |

| 208-Pin PQFP | | | | |
|---|---|---|---|---|
| **Pin Number** | **A54SX08A Function** | **A54SX16A Function** | **A54SX32A Function** | **A54SX72A Function** |
| 36 | I/O | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O | I/O |
| 39 | NC | I/O | I/O | I/O |
| 40 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 41 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 42 | I/O | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O | I/O |
| 44 | I/O | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O | I/O |
| 48 | NC | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O | I/O |
| 50 | NC | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O | I/O |
| 52 | GND | GND | GND | GND |
| 53 | I/O | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 61 | NC | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O | I/O |
| 64 | NC | I/O | I/O | I/O |
| 65 | I/O | I/O | NC | I/O |
| 66 | I/O | I/O | I/O | I/O |
| 67 | NC | I/O | I/O | I/O |
| 68 | I/O | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O | I/O |
| 70 | NC | I/O | I/O | I/O |

| 100-TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | I/O | I/O | I/O |
| 80 | I/O | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | CLKA | CLKA | CLKA |
| 88 | CLKB | CLKB | CLKB |
| 89 | NC | NC | NC |
| 90 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 91 | GND | GND | GND |
| 92 | PRA, I/O | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | I/O | I/O | I/O |
| 99 | I/O | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O | TCK, I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32A Function |
| V22 | I/O |
| V23 | I/O |
| W1 | I/O |
| W2 | I/O |
| W3 | I/O |
| W4 | I/O |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |
| W23 | NC |
| Y1 | NC |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | GND |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | I/O |
| Y12 | $V_{CCA}$ |
| Y13 | NC |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | GND |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |

# 256-Pin FBGA

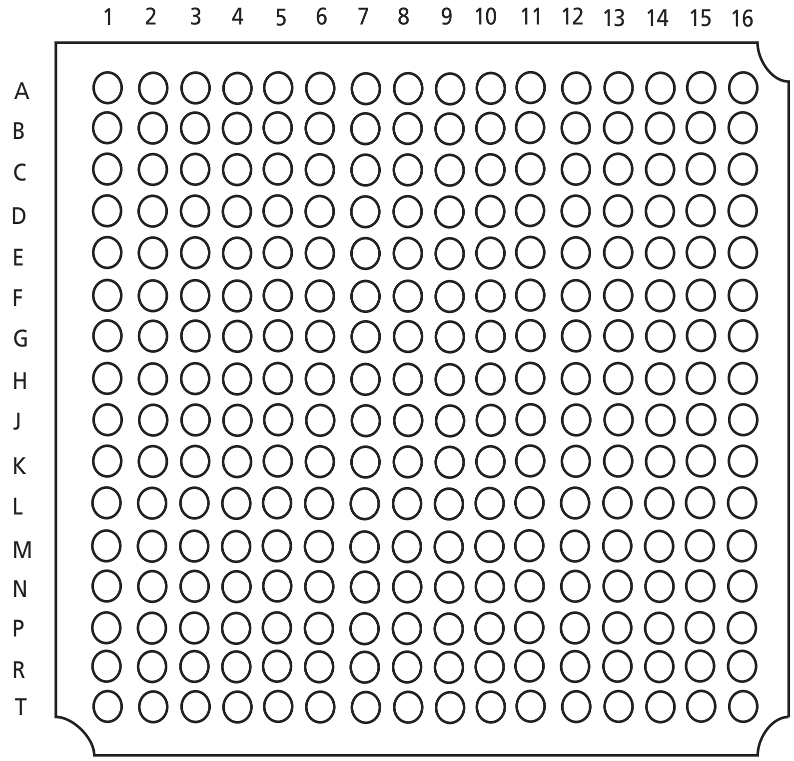


*Figure 3-7* • **256-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# 484-Pin FBGA

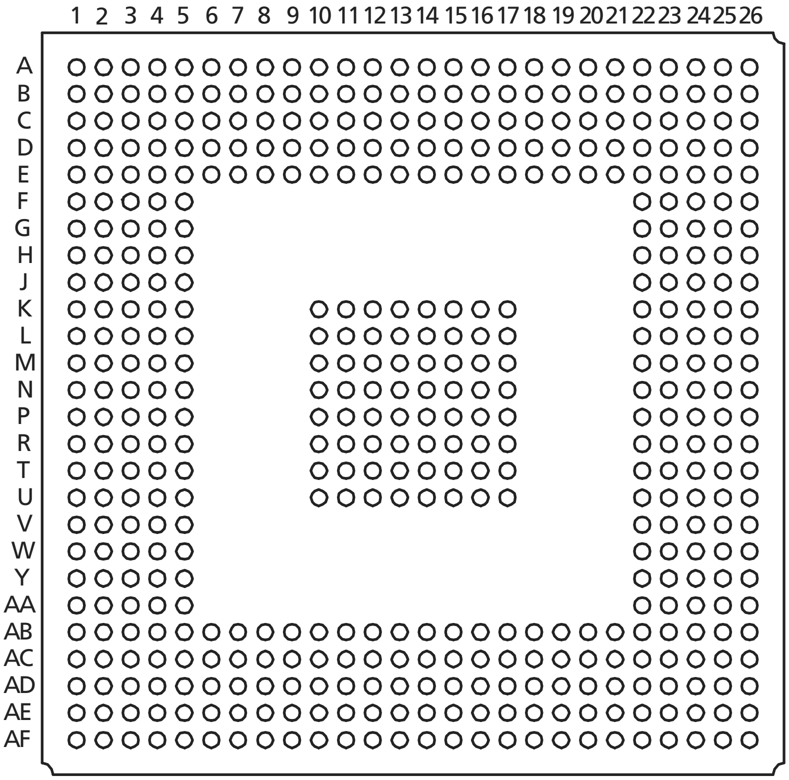


*Figure 3-8* • **484-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v5.3) | Page |
|---|---|---|
| v5.2<br>(June 2006) | –3 speed grades have been discontinued. | N/A |
| | The "SX-A Timing Model" was updated with –2 data. | 2-14 |
| v5.1<br>February 2005 | RoHS information was added to the "Ordering Information". | ii |
| | The "Programming" section was updated. | 1-13 |
| v5.0 | Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device. | i |
| | The "Thermal Characteristics" section was updated. | 2-11 |
| | The "176-Pin TQFP" was updated to add pins 81 to 90. | 3-11 |
| | The "484-Pin FBGA" was updated to add pins R4 to Y26 | 3-26 |
| v4.0 | The "Temperature Grade Offering" is new. | 1-iii |
| | The "Speed Grade and Temperature Grade Matrix" is new. | 1-iii |
| | "SX-A Family Architecture" was updated. | 1-1 |
| | "Clock Resources" was updated. | 1-5 |
| | "User Security" was updated. | 1-7 |
| | "Power-Up/Down and Hot Swapping" was updated. | 1-7 |
| | "Dedicated Mode" is new | 1-9 |
| | Table 1-5 is new. | 1-9 |
| | "JTAG Instructions" is new | 1-10 |
| | "Design Considerations" was updated. | 1-12 |
| | The "Programming" section is new. | 1-13 |
| | "Design Environment" was updated. | 1-13 |
| | "Pin Description" was updated. | 1-15 |
| | Table 2-1 was updated. | 2-1 |
| | Table 2-2 was updated. | 2-1 |
| | Table 2-3 is new. | 2-1 |
| | Table 2-4 is new. | 2-1 |
| | Table 2-5 was updated. | 2-2 |
| | Table 2-6 was updated. | 2-2 |
| | "Power Dissipation" is new. | 2-8 |
| | Table 2-11 was updated. | 2-9 |

# Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

## Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

## Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

## Unmarked (production)

This datasheet version contains information that is considered to be final.

## Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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