E·XFL



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	
Total RAM Bits	-
Number of I/O	174
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-1pq208

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Information



Notes:

1. For more information about the CQFP package options, refer to the HiRel SX-A datasheet.

2. All –3 speed grades have been discontinued.

Device Resources

		User I/Os (Including Clock Buffers)													
Device	208-Pin PQFP	100-Pin TQFP	144-Pin TQFP	176-Pin TQFP	329-Pin PBGA	144-Pin FBGA	256-Pin FBGA	484-Pin FBGA							
A54SX08A	130	81	113	-	-	111	-	-							
A54SX16A	175	81	113	-	-	111	180	-							
A54SX32A	174	81	113	147	249	111	203	249							
A54SX72A	171	-	-	-	-	_	203	360							

Notes: Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

Table of Contents

General Description

Introduction	1-1
SX-A Family Architecture	1-1
Other Architectural Features	1-7
Programming	1-13
Related Documents	1-14
Pin Description	1-15

Detailed Specifications

Operating Conditions	2-1
Typical SX-A Standby Current	2-1
Electrical Specifications	2-2
PCI Compliance for the SX-A Family	2-3
Thermal Characteristics 2	2-11
SX-A Timing Model 2	2-14
Sample Path Calculations 2	2-14
Output Buffer Delays 2	2-15
AC Test Loads	2-15
Input Buffer Delays 2	2-16
C-Cell Delays 2	2-16
Cell Timing Characteristics 2	2-16
Timing Characteristics 2	2-17
Temperature and Voltage Derating Factors 2	2-17
Timing Characteristics 2	2-18

Package Pin Assignments

208-Pin PQFP	 		 	•								 •	 •					 	3-	·1
100-Pin TQFP	 		 	•								 •	 	•				 	3-	-5
144-Pin TQFP	 		 	•								 •	 	•				 	3-	8
176-Pin TQFP	 		 	•								 •	 	•					3-1	1
329-Pin PBGA	 		 	•								 •	 	•					3-1	4
144-Pin FBGA	 		 	•								 •	 	•					3-1	8
256-Pin FBGA	 		 	•								 •	 	•					3-2	1
484-Pin FBGA	 		 																3-2	6

Datasheet Information

List of Changes	4-1
Datasheet Categories	4-3
International Traffic in Arms Regulations (ITAR) and Export Administration	
Regulations (EAR)	4-3

Logic Module Design

The SX-A family architecture is described as a "sea-ofmodules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-byregister basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000 different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.



Figure 1-2 • R-Cell



Figure 1-3 • C-Cell



Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as a user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, the user must reserve the JTAG pins in Actel's Designer software. Reserve the JTAG pins by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12).

The default for the software is Flexible mode; all boxes are unchecked. Table 1-5 lists the definitions of the options in the Device Selection Wizard.

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, uncheck the **Reserve JTAG** box in the Device Selection Wizard dialog in the Actel Designer software. In Flexible mode, TDI, TCK, and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST Test Access Port (TAP) controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. **An external 10 k pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it High by default.**

Table 1-6 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-6	٠	Boundary-Scan Pin Configurations an	d
		Functions	

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test- Logic-Reset

Figure 1-12 • Device Selection Wizard

Table 1-5 • Reserve Pin Definitions

Pin	Function					
Reserve JTAG	Keeps pins from being used and changes the behavior of JTAG pins (no pull-up on TMS)					
Reserve JTAG Test Reset	Regular I/O or JTAG reset with an internal pull-up					
Reserve Probe	Keeps pins from being used or regular I/O					

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or can be driven high.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70 Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70 Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.



Figure 1-13 • Probe Setup

Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V _{CCI}	DC Supply Voltage for I/Os	-0.3 to +6.0	V
V _{CCA}	DC Supply Voltage for Arrays	-0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
V _O	Output Voltage	–0.5 to + V _{CCI} + 0.5	V
T _{STG}	Storage Temperature	–65 to +150	°C

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
2.5 V Power Supply Range (V _{CCA} and V _{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V _{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V _{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with $V_{CCA} = 2.5 V$

Product	V _{CCI} = 2.5 V	V _{CCI} = 3.3 V	V _{CCI} = 5 V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

V _{CCA}	V _{CCI} *	Maximum Input Tolerance	Maximum Output Drive
2. 5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

Note: *3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.



PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V _{CCA}	Supply Voltage for Array		2.25	2.75	V
V _{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	5.75	V
V _{IL}	Input Low Voltage		-0.5	0.8	V
I _{IH}	Input High Leakage Current ¹	V _{IN} = 2.7	-	70	μΑ
IIL	Input Low Leakage Current ¹	V _{IN} = 0.5	-	-70	μΑ
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4	-	V
V _{OL}	Output Low Voltage ²	I _{OUT} = 3 mA, 6 mA	-	0.55	V
C _{IN}	Input Pin Capacitance ³		-	10	pF
C _{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.

2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.

3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Symbol	Parameter	Condition	Min.	Max.	Units
I _{OH(AC)}	Switching Current High	$0 < V_{OUT} \le 0.3 V_{CCI}^{1}$	–12V _{CCI}	-	mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ ¹	(-17.1(V _{CCI} - V _{OUT}))	_	mA
		0.7V _{CCI} < V _{OUT} < V _{CCI} ^{1, 2}	_	EQ 2-3 on page 2-7	-
	(Test Point)	$V_{OUT} = 0.7 V_{CC}^2$	-	-32V _{CCI}	mA
I _{OL(AC)}	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6 V_{CCI}^{1}$	16V _{CCI}	-	mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^{1}$	(26.7V _{OUT})	-	mA
		0.18V _{CCI} > V _{OUT} > 0 ^{1, 2}	_	EQ 2-4 on page 2-7	-
	(Test Point)	$V_{OUT} = 0.18 V_{CC}^2$	-	38V _{CCI}	mA
I _{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	–25 + (V _{IN} + 1)/0.015	-	mA
I _{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	25 + (V _{IN} – V _{CCI} – 1)/0.015	-	mA
slew _R	Output Rise Slew Rate	0.2V _{CCI} - 0.6V _{CCI} load ³	1	4	V/ns
slew _F	Output Fall Slew Rate	$0.6V_{CCI} - 0.2V_{CCI} \log^3$	1	4	V/ns

Table 2-10 • AC Specifications (3.3 V PCI Operation)

Notes:

1. Refer to the V/I curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.

- 2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
- 3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.





Where:

- C_{EQCM} = Equivalent capacitance of combinatorial modules (C-cells) in pF
- C_{EQSM} = Equivalent capacitance of sequential modules (R-Cells) in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of CLKA/B in pF
- C_{EQHV} = Variable capacitance of HCLK in pF
- C_{EQHF} = Fixed capacitance of HCLK in pF
 - C_{L =} Output lead capacitance in pF
 - f_m = Average logic module switching rate in MHz
 - $f_n =$ Average input buffer switching rate in MHz
 - f_p = Average output buffer switching rate in MHz
 - $f_{a1} =$ Average CLKA rate in MHz
 - $f_{\alpha 2}$ = Average CLKB rate in MHz
 - f_{s1} = Average HCLK rate in MHz
 - m = Number of logic modules switching at fm
 - n = Number of input buffers switching at fn
 - p = Number of output buffers switching at fp
 - q₁ = Number of clock loads on CLKA
 - q₂ = Number of clock loads on CLKB
 - $r_1 =$ Fixed capacitance due to CLKA
 - r₂ = Fixed capacitance due to CLKB
 - s1 = Number of clock loads on HCLK
 - x = Number of I/Os at logic low
 - y = Number of I/Os at logic high

Table 2-11 • CEQ Values for SX-A Devices

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Combinatorial modules (C _{EQCM})	1.70 pF	2.00 pF	2.00 pF	1.80 pF
Sequential modules (C _{EQCM})	1.50 pF	1.50 pF	1.30 pF	1.50 pF
Input buffers (C _{EQI})	1.30 pF	1.30 pF	1.30 pF	1.30 pF
Output buffers (C _{EQO})	7.40 pF	7.40 pF	7.40 pF	7.40 pF
Routed array clocks (C _{EQCR})	1.05 pF	1.05 pF	1.05 pF	1.05 pF
Dedicated array clocks – variable (C _{EQHV})	0.85 pF	0.85 pF	0.85 pF	0.85 pF
Dedicated array clocks – fixed (C_{EQHF})	30.00 pF	55.00 pF	110.00 pF	240.00 pF
Routed array clock A (r ₁)	35.00 pF	50.00 pF	90.00 pF	310.00 pF

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}$$
C/W is taken from Table 2-12 on page 2-11

 $T_A = 125$ °C is the maximum limit of ambient (from the datasheet)

Max. Allowed Power =
$$\frac{\text{Max Junction Temp - Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

$$T_{J} = 110^{\circ}C$$

 $T_{A} = 70^{\circ}C$

From the datasheet:

 $\theta_{JA} = 18.0^{\circ}C/W$ $\theta_{JC} = 3.2^{\circ}C/W$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{Max Junction Temp - Max. Ambient Temp}{P} = \frac{110^{\circ}C - 70^{\circ}C}{3.00 W} = 13.33^{\circ}C/W$$

EQ 2-13



Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. The timing characteristics listed in this datasheet represent sample timing numbers of the SX-A devices. Design-specific delay values may be determined by using Timer or performing simulation after successful place-and-route with the Designer software.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

 Table 2-13
 Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.25 V)

			Juncti	ion Temperatu	re (T _J)		
V _{CCA}	-55°C -40°C 0° 0.79 0.80 0.4 0.74 0.75 0.4 0.68 0.69 0.4		0°C	25°C	70°C	85°C	125°C
2.250 V	0.79	0.80	0.87	0.89	1.00	1.04	1.14
2.500 V	0.74	0.75	0.82	0.83	0.94	0.97	1.07
2.750 V	0.68	0.69	0.75	0.77	0.87	0.90	0.99

Timing Characteristics

Table 2-14 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

		-2 S	peed	-1 S	peed	Std. S	5peed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
C-Cell Propa	igation Delays ¹									
t _{PD}	Internal Array Module		0.9		1.1		1.2		1.7	ns
Predicted Ro	outing Delays ²									
t _{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t _{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.3		0.4		0.6	ns
t _{RD1}	FO = 1 Routing Delay		0.3		0.4		0.5		0.6	ns
t _{RD2}	FO = 2 Routing Delay		0.5		0.5		0.6		0.8	ns
t _{RD3}	FO = 3 Routing Delay		0.6		0.7		0.8		1.1	ns
t _{RD4}	FO = 4 Routing Delay		0.8		0.9		1		1.4	ns
t _{RD8}	FO = 8 Routing Delay		1.4		1.5		1.8		2.5	ns
t _{RD12}	FO = 12 Routing Delay		2		2.2		2.6		3.6	ns
R-Cell Timin	lg									
t _{RCO}	Sequential Clock-to-Q		0.7		0.8		0.9		1.3	ns
t _{CLR}	Asynchronous Clear-to-Q		0.6		0.6		0.8		1.0	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.7		0.7		0.9		1.2	ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.2		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.5		1.8		2.5		ns
t _{recasyn}	Asynchronous Recovery Time	0.4		0.4		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.3		0.4		0.6		ns
t _{MPW}	Clock Pulse Width	1.6		1.8		2.1		2.9		ns
Input Modu	le Propagation Delays									
t _{INYH}	Input Data Pad to Y High 2.5 V LVCMOS		0.8		0.9		1.0		1.4	ns
t _{INYL}	Input Data Pad to Y Low 2.5 V LVCMOS		1.0		1.2		1.4		1.9	ns
t _{INYH}	Input Data Pad to Y High 3.3 V PCI		0.6		0.6		0.7		1.0	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V PCI		0.7		0.8		0.9		1.3	ns
t _{INYH}	Input Data Pad to Y High 3.3 V LVTTL		0.7		0.7		0.9		1.2	ns
t _{INYL}	Input Data Pad to Y Low 3.3 V LVTTL		1.0		1.1		1.3		1.8	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-18 A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions	$V_{CCA} = 2.25 V, V_{CCI} = 2.3 V, T_{I} = 2$	70°C)
(- (CA =	,

		-2 S	peed	-1 S	peed	Std. S	5peed	–F S	peed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCMO	S Output Module Timing ^{1,2}									
t _{DLH}	Data-to-Pad Low to High		3.9		4.4		5.2		7.2	ns
t _{DHL}	Data-to-Pad High to Low		3.0		3.4		3.9		5.5	ns
t _{DHLS}	Data-to-Pad High to Low—low slew		13.3		15.1		17.7		24.8	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.9		4.4		5.2		7.2	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.0		3.4		3.9		5.5	ns
d _{TLH} ³	Delta Low to High		0.037		0.043		0.051		0.071	ns/pF
d _{THL} ³	Delta High to Low		0.017		0.023		0.023		0.037	ns/pF
d _{THLS} ³	Delta High to Low—low slew		0.06		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

2. The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = (0.1* V_{CCI} – 0.9* V_{CCI} / (C_{load} * $d_{T[LH|HL|HLS]}$) where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

Table 2-31 A54SX32A Timing Characteristics

(Worst-Case Commercial Condition	s V _{CCA} = 2.25 V, V _{CCI} :	= 4.75 V, T _J = 70°C)
----------------------------------	---	----------------------------------

		-3 Sp	beed*	-2 S	peed	-1 S	peed	Std.	Speed	-F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated ((Hardwired) Array Clock Netwo	rks										
t _{HCKH}	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t _{HCKL}	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t _{HPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{HPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t _{HP}	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f _{HMAX}	Maximum Frequency		357		313		278		238		172	MHz
Routed Arr	ay Clock Networks											
t _{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t _{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t _{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t _{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t _{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t _{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t _{RPWH}	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t _{RPWL}	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t _{RCKSW}	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: *All –3 speed grades have been discontinued.

Table 2-39 A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions $V_{CCA} = 2.25 \text{ V}$, $V_{CCI} = 2.3 \text{ V}$, $T_J = 70^{\circ}\text{C}$)

		-3 Speed	-2	Speed	-1 Speed	Std. 9	Speed	–F Sp	beed	
Parameter	Description	Min. Ma	. Mir	. Max.	Min. Max	Min.	Max.	Min.	Max.	Units
2.5 V LVCM	OS Output Module Timing ^{2, 3}									
t _{DLH}	Data-to-Pad Low to High	3.9		4.5	5.1		6.0		8.4	ns
t _{DHL}	Data-to-Pad High to Low	3.1		3.6	4.1		4.8		6.7	ns
t _{DHLS}	Data-to-Pad High to Low—low slew	12.	,	14.6	16.5		19.4		27.2	ns
t _{ENZL}	Enable-to-Pad, Z to L	2.4		2.8	3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.	3	13.7	15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H	3.9		4.5	5.1		6.0		8.4	ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.1		2.5	2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z	3.1		3.6	4.1		4.8		6.7	ns
d_{TLH}^{4}	Delta Low to High	0.03	1	0.037	0.043		0.051		0.071	ns/pF
${\sf d_{THL}}^4$	Delta High to Low	0.01	7	0.017	0.023		0.023		0.037	ns/pF
d_{THLS}^4	Delta High to Low—low slew	0.05	7	0.06	0.071		0.086		0.117	ns/pF

Note:

1. All –3 speed grades have been discontinued.

2. Delays based on 35 pF loading.

3. The equivalent IO Attribute settings for 2.5 V LVCMOS is 2.5 V LVTTL in the software.

4. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation: Slew Rate [V/ns] = $(0.1 * V_{CCI} - 0.9 * V_{CCI})/(C_{load} * d_{T[LH|HL|HLS]})$ where C_{load} is the load capacitance driven by the I/O in pF

 $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.

144-Pin TQFP



Figure 3-3 • 144-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

329-Pin PBGA

		12	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Α	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{0}$
В	C	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
С	(00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D		$\frac{1}{2}$	0	0	0	0	Ο	Ο	0	Ο	Ο	0	0	Ο	0	Ο	Ο	0	Ο	0	0	0	0
E) 0	0	0																0	Ö	0	0
г G		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $																				\bigcirc
Н		$\frac{1}{2}$	$\overline{0}$	0																$\hat{0}$	0	$\hat{0}$	$\tilde{0}$
J	Ċ	50	Õ	õ																ŏ	ŏ	õ	õ
к	C	00	0	0						Ο	0	Ο	0	0						Ο	Ο	Ο	0
L	C	00	0	0						0	0	0	0	0						0	Ο	Ο	0
M		$\sum_{i=1}^{i}$	0	0						Õ	Õ	Õ	Õ	Õ						Õ	Õ	Õ	0
N P		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $	0								0								0	0	\bigcirc	\mathbf{O}
R		$\frac{1}{2}$	$\overline{0}$	õ						0	0	0	0	0						0	õ	õ	0
т	C	00	Õ	Õ																Õ	õ	Õ	Õ
U	C	00	0	Ο																0	0	0	0
V	C	00	0	0																0	0	0	0
W		$\frac{1}{2}$	0	0	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	0	Õ	0	0
Y A A) 0	\mathbf{O}	0	0	0	0	0	0	0	0	0 O	O	O	0	0	0	0	0	0	0	0	0
AB		$\frac{1}{2}$	$\left \begin{array}{c} 0 \\ 0 \end{array} \right $								0	0		0									0
AC	$\left(\right)$	$\frac{1}{2}$	$\overline{0}$	0	0	0	õ	0	0	0	õ	õ	õ	õ	0	0	0	0	õ	0	õ	õ	õ
).		Ũ	-	Ŭ	-	-	-	Ŭ	Ŭ	Ŭ	Ŭ	-	-	Ŭ	-	-	-	-	Ŭ	Ŭ	Ŭ	- (

Figure 3-5 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.



329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
A1	GND	AA15	I/O	AC6	I/O	B20	I/O
A2	GND	AA16	I/O	AC7	I/O	B21	I/O
A3	V _{CCI}	AA17	I/O	AC8	I/O	B22	GND
A4	NC	AA18	I/O	AC9	V _{CCI}	B23	V _{CCI}
A5	I/O	AA19	I/O	AC10	I/O	C1	NC
A6	I/O	AA20	TDO, I/O	AC11	I/O	C2	TDI, I/O
A7	V _{CCI}	AA21	V _{CCI}	AC12	I/O	C3	GND
A8	NC	AA22	I/O	AC13	I/O	C4	I/O
A9	I/O	AA23	V _{CCI}	AC14	I/O	C5	I/O
A10	I/O	AB1	I/O	AC15	NC	C6	I/O
A11	I/O	AB2	GND	AC16	I/O	С7	I/O
A12	I/O	AB3	I/O	AC17	I/O	C8	I/O
A13	CLKB	AB4	I/O	AC18	I/O	С9	I/O
A14	I/O	AB5	I/O	AC19	I/O	C10	I/O
A15	I/O	AB6	I/O	AC20	I/O	C11	I/O
A16	I/O	AB7	I/O	AC21	NC	C12	I/O
A17	I/O	AB8	I/O	AC22	V _{CCI}	C13	I/O
A18	I/O	AB9	I/O	AC23	GND	C14	I/O
A19	I/O	AB10	I/O	B1	V _{CCI}	C15	I/O
A20	I/O	AB11	PRB, I/O	B2	GND	C16	I/O
A21	NC	AB12	I/O	B3	I/O	C17	I/O
A22	V _{CCI}	AB13	HCLK	B4	I/O	C18	I/O
A23	GND	AB14	I/O	B5	I/O	C19	I/O
AA1	V _{CCI}	AB15	I/O	B6	I/O	C20	I/O
AA2	I/O	AB16	I/O	В7	I/O	C21	V _{CCI}
AA3	GND	AB17	I/O	B8	I/O	C22	GND
AA4	I/O	AB18	I/O	B9	I/O	C23	NC
AA5	I/O	AB19	I/O	B10	I/O	D1	I/O
AA6	I/O	AB20	I/O	B11	I/O	D2	I/O
AA7	I/O	AB21	I/O	B12	PRA, I/O	D3	I/O
AA8	I/O	AB22	GND	B13	CLKA	D4	TCK, I/O
AA9	I/O	AB23	I/O	B14	I/O	D5	I/O
AA10	I/O	AC1	GND	B15	I/O	D6	I/O
AA11	I/O	AC2	V _{CCI}	B16	I/O	D7	I/O
AA12	I/O	AC3	NC	B17	I/O	D8	I/O
AA13	I/O	AC4	I/O	B18	I/O	D9	I/O
AA14	I/O	AC5	I/O	B19	I/O	D10	I/O

144-Pin FBGA



Figure 3-6 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.