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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                                                     |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                                            |
| Number of LABs/CLBs            | 2880                                                                                                                                                                |
| Number of Logic Elements/Cells | -                                                                                                                                                                   |
| Total RAM Bits                 | -                                                                                                                                                                   |
| Number of I/O                  | 174                                                                                                                                                                 |
| Number of Gates                | 48000                                                                                                                                                               |
| Voltage - Supply               | 2.25V ~ 5.25V                                                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                                                       |
| Operating Temperature          | -55°C ~ 125°C (TC)                                                                                                                                                  |
| Package / Case                 | 208-BFQFP                                                                                                                                                           |
| Supplier Device Package        | 208-PQFP (28x28)                                                                                                                                                    |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-1pq208m">https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-1pq208m</a> |

## Temperature Grade Offering

| Package | A54SX08A | A54SX16A | A54SX32A | A54SX72A |
|---------|----------|----------|----------|----------|
| PQ208   | C,I,A,M  | C,I,A,M  | C,I,A,M  | C,I,A,M  |
| TQ100   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| TQ144   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| TQ176   |          |          | C,I,M    |          |
| BG329   |          |          | C,I,M    |          |
| FG144   | C,I,A,M  | C,I,A,M  | C,I,A,M  |          |
| FG256   |          | C,I,A,M  | C,I,A,M  | C,I,A,M  |
| FG484   |          |          | C,I,M    | C,I,A,M  |
| CQ208   |          |          | C,M,B    | C,M,B    |
| CQ256   |          |          | C,M,B    | C,M,B    |

**Notes:**

1. C = Commercial
2. I = Industrial
3. A = Automotive
4. M = Military
5. B = MIL-STD-883 Class B
6. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
7. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

## Speed Grade and Temperature Grade Matrix

|              | F | Std | -1 | -2 | -3           |
|--------------|---|-----|----|----|--------------|
| Commercial   | ✓ | ✓   | ✓  | ✓  | Discontinued |
| Industrial   |   | ✓   | ✓  | ✓  | Discontinued |
| Automotive   |   | ✓   |    |    |              |
| Military     |   | ✓   | ✓  |    |              |
| MIL-STD-883B |   | ✓   | ✓  |    |              |

**Notes:**

1. For more information regarding automotive products, refer to the SX-A Automotive Family FPGAs datasheet.
2. For more information regarding Mil-Temp and ceramic packages, refer to the HiRel SX-A Family FPGAs datasheet.

Contact your Actel Sales representative for more information on availability.

# General Description

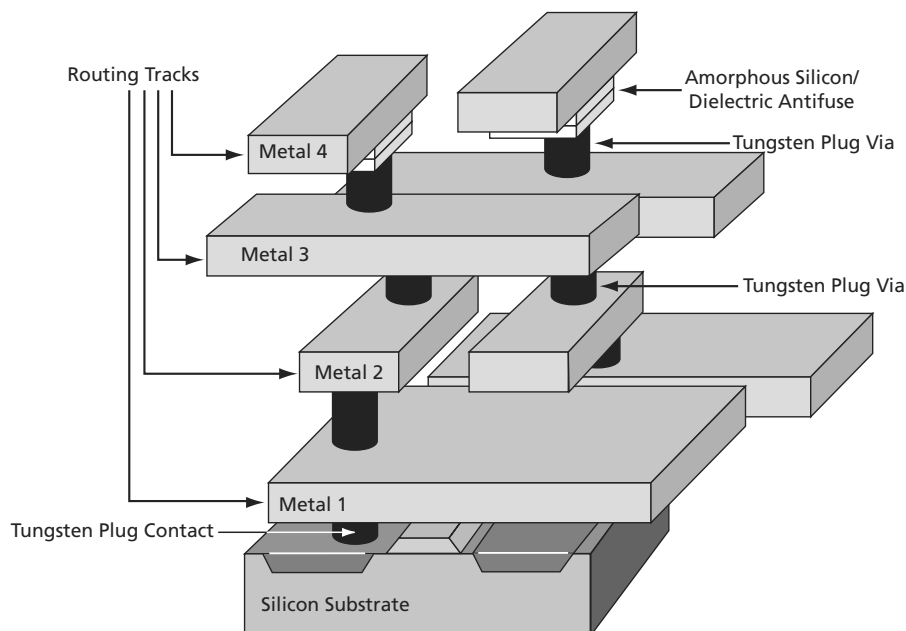
## Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22  $\mu\text{m}$  / 0.25  $\mu\text{m}$  CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

## SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



**Note:** The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

## Design Environment

The SX-A family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmarGen core generator, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

## Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor is compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor also provides extensive hardware self-testing capability.

The procedure for programming an SX-A device using Silicon Sculptor is as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For detailed information on programming, read the following documents *Programming Antifuse Devices* and *Silicon Sculptor User's Guide*.

## PCI Compliance for the SX-A Family

The SX-A family supports 3.3 V and 5 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-7 • DC Specifications (5 V PCI Operation)

| Symbol           | Parameter                               | Condition                     | Min. | Max. | Units |
|------------------|-----------------------------------------|-------------------------------|------|------|-------|
| V <sub>CCA</sub> | Supply Voltage for Array                |                               | 2.25 | 2.75 | V     |
| V <sub>CCI</sub> | Supply Voltage for I/Os                 |                               | 4.75 | 5.25 | V     |
| V <sub>IH</sub>  | Input High Voltage                      |                               | 2.0  | 5.75 | V     |
| V <sub>IL</sub>  | Input Low Voltage                       |                               | –0.5 | 0.8  | V     |
| I <sub>IH</sub>  | Input High Leakage Current <sup>1</sup> | V <sub>IN</sub> = 2.7         | –    | 70   | μA    |
| I <sub>IL</sub>  | Input Low Leakage Current <sup>1</sup>  | V <sub>IN</sub> = 0.5         | –    | –70  | μA    |
| V <sub>OH</sub>  | Output High Voltage                     | I <sub>OUT</sub> = –2 mA      | 2.4  | –    | V     |
| V <sub>OL</sub>  | Output Low Voltage <sup>2</sup>         | I <sub>OUT</sub> = 3 mA, 6 mA | –    | 0.55 | V     |
| C <sub>IN</sub>  | Input Pin Capacitance <sup>3</sup>      |                               | –    | 10   | pF    |
| C <sub>CLK</sub> | CLK Pin Capacitance                     |                               | 5    | 12   | pF    |

### Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

**Table 2-8 • AC Specifications (5 V PCI Operation)**

| Symbol       | Parameter              | Condition                                 | Min.                            | Max.               | Units |
|--------------|------------------------|-------------------------------------------|---------------------------------|--------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4$ <sup>1</sup>       | -44                             | –                  | mA    |
|              |                        | $1.4 \leq V_{OUT} < 2.4$ <sup>1, 2</sup>  | $(-44 + (V_{OUT} - 1.4)/0.024)$ | –                  | mA    |
|              |                        | $3.1 < V_{OUT} < V_{CCI}$ <sup>1, 3</sup> | –                               | EQ 2-1 on page 2-5 | –     |
|              | (Test Point)           | $V_{OUT} = 3.1$ <sup>3</sup>              | –                               | -142               | mA    |
| $I_{OL(AC)}$ | Switching Current Low  | $V_{OUT} \geq 2.2$ <sup>1</sup>           | 95                              | –                  | mA    |
|              |                        | $2.2 > V_{OUT} > 0.55$ <sup>1</sup>       | $(V_{OUT}/0.023)$               | –                  | mA    |
|              |                        | $0.71 > V_{OUT} > 0$ <sup>1, 3</sup>      | –                               | EQ 2-2 on page 2-5 | –     |
|              | (Test Point)           | $V_{OUT} = 0.71$ <sup>3</sup>             | –                               | 206                | mA    |
| $I_{CL}$     | Low Clamp Current      | $-5 < V_{IN} \leq -1$                     | $-25 + (V_{IN} + 1)/0.015$      | –                  | mA    |
| $slew_R$     | Output Rise Slew Rate  | 0.4 V to 2.4 V load <sup>4</sup>          | 1                               | 5                  | V/ns  |
| $slew_F$     | Output Fall Slew Rate  | 2.4 V to 0.4 V load <sup>4</sup>          | 1                               | 5                  | V/ns  |

**Notes:**

1. Refer to the V/I curves in Figure 2-1 on page 2-5. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 2-1 on page 2-5. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

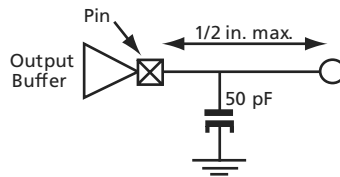


Figure 2-1 shows the 5 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

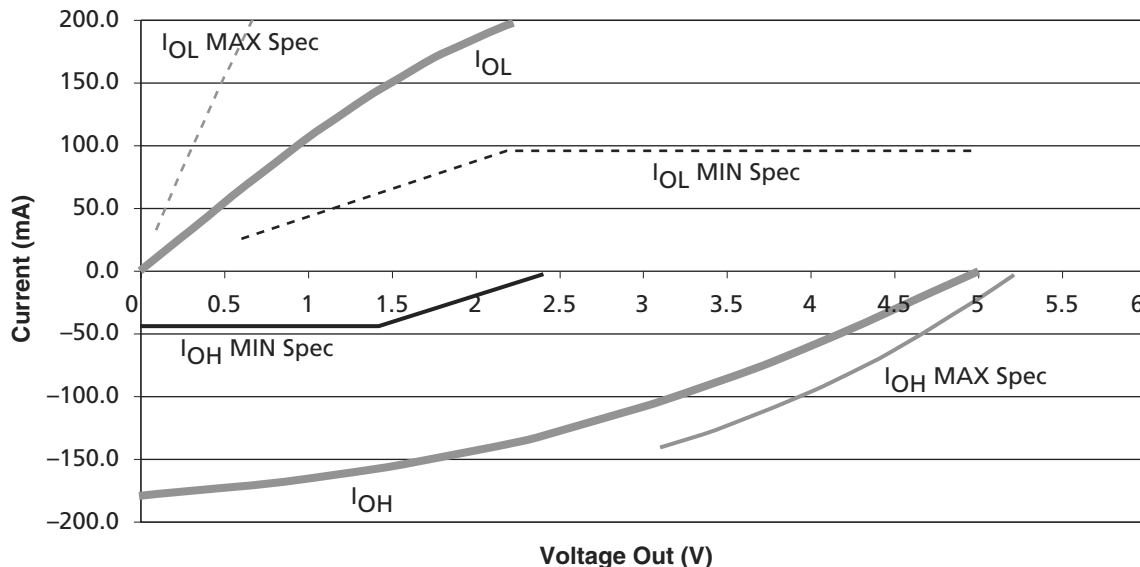


Figure 2-1 • 5 V PCI V/I Curve for SX-A Family

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for  $V_{CCI} > V_{OUT} > 3.1V$

EQ 2-1

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for  $0V < V_{OUT} < 0.71V$

EQ 2-2

Table 2-9 • DC Specifications (3.3 V PCI Operation)

| Symbol    | Parameter                          | Condition               | Min.         | Max.            | Units   |
|-----------|------------------------------------|-------------------------|--------------|-----------------|---------|
| $V_{CCA}$ | Supply Voltage for Array           |                         | 2.25         | 2.75            | V       |
| $V_{CCI}$ | Supply Voltage for I/Os            |                         | 3.0          | 3.6             | V       |
| $V_{IH}$  | Input High Voltage                 |                         | $0.5V_{CCI}$ | $V_{CCI} + 0.5$ | V       |
| $V_{IL}$  | Input Low Voltage                  |                         | -0.5         | $0.3V_{CCI}$    | V       |
| $I_{IPU}$ | Input Pull-up Voltage <sup>1</sup> |                         | $0.7V_{CCI}$ | –               | V       |
| $I_{IL}$  | Input Leakage Current <sup>2</sup> | $0 < V_{IN} < V_{CCI}$  | -10          | +10             | $\mu A$ |
| $V_{OH}$  | Output High Voltage                | $I_{OUT} = -500 \mu A$  | $0.9V_{CCI}$ | –               | V       |
| $V_{OL}$  | Output Low Voltage                 | $I_{OUT} = 1,500 \mu A$ |              | $0.1V_{CCI}$    | V       |
| $C_{IN}$  | Input Pin Capacitance <sup>3</sup> |                         | –            | 10              | pF      |
| $C_{CLK}$ | CLK Pin Capacitance                |                         | 5            | 12              | pF      |

**Notes:**

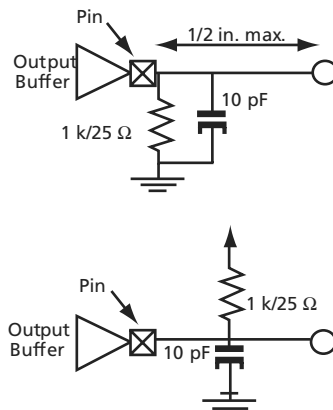
1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 2-10 • AC Specifications (3.3 V PCI Operation)

| Symbol       | Parameter              | Condition                                   | Min.                                | Max.               | Units |
|--------------|------------------------|---------------------------------------------|-------------------------------------|--------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CCI}^1$             | $-12V_{CCI}$                        | –                  | mA    |
|              |                        | $0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}^1$    | $(-17.1(V_{CCI} - V_{OUT}))$        | –                  | mA    |
|              |                        | $0.7V_{CCI} < V_{OUT} < V_{CCI}^{1,2}$      | –                                   | EQ 2-3 on page 2-7 | –     |
|              | (Test Point)           | $V_{OUT} = 0.7V_{CC}^2$                     | –                                   | $-32V_{CCI}$       | mA    |
| $I_{OL(AC)}$ | Switching Current Low  | $V_{CCI} > V_{OUT} \geq 0.6V_{CCI}^1$       | $16V_{CCI}$                         | –                  | mA    |
|              |                        | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^1$       | $(26.7V_{OUT})$                     | –                  | mA    |
|              |                        | $0.18V_{CCI} > V_{OUT} > 0^{1,2}$           | –                                   | EQ 2-4 on page 2-7 | –     |
|              | (Test Point)           | $V_{OUT} = 0.18V_{CC}^2$                    | –                                   | $38V_{CCI}$        | mA    |
| $I_{CL}$     | Low Clamp Current      | $-3 < V_{IN} \leq -1$                       | $-25 + (V_{IN} + 1)/0.015$          | –                  | mA    |
| $I_{CH}$     | High Clamp Current     | $V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$     | $25 + (V_{IN} - V_{CCI} - 1)/0.015$ | –                  | mA    |
| $slew_R$     | Output Rise Slew Rate  | $0.2V_{CCI} - 0.6V_{CCI}$ load <sup>3</sup> | 1                                   | 4                  | V/ns  |
| $slew_F$     | Output Fall Slew Rate  | $0.6V_{CCI} - 0.2V_{CCI}$ load <sup>3</sup> | 1                                   | 4                  | V/ns  |

**Notes:**

1. Refer to the *VII* curves in Figure 2-2 on page 2-7. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 2-2 on page 2-7. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.



To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

$$\theta_{CS} = 0.37^{\circ}\text{C/W}$$

= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$$\theta_{SA} = \text{thermal resistance of the heat sink in } ^{\circ}\text{C/W}$$

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33^{\circ}\text{C/W} - 3.20^{\circ}\text{C/W} - 0.37^{\circ}\text{C/W}$$

$$\theta_{SA} = 9.76^{\circ}\text{C/W}$$

A heat sink with a thermal resistance of  $9.76^{\circ}\text{C/W}$  or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Table 2-15 • **A54SX08A Timing Characteristics**  
**(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.25\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

| Parameter                                  | Description                                          | –2 Speed |      | –1 Speed |      | Std. Speed |      | –F Speed |      | Units |
|--------------------------------------------|------------------------------------------------------|----------|------|----------|------|------------|------|----------|------|-------|
|                                            |                                                      | Min.     | Max. | Min.     | Max. | Min.       | Max. | Min.     | Max. |       |
| Dedicated (Hardwired) Array Clock Networks |                                                      |          |      |          |      |            |      |          |      |       |
| t <sub>HCKH</sub>                          | Input Low to High (Pad to R-cell Input)              | 1.4      |      | 1.6      |      | 1.8        |      | 2.6      |      | ns    |
| t <sub>HCKL</sub>                          | Input High to Low (Pad to R-cell Input)              | 1.3      |      | 1.5      |      | 1.7        |      | 2.4      |      | ns    |
| t <sub>HPWH</sub>                          | Minimum Pulse Width High                             | 1.6      |      | 1.8      |      | 2.1        |      | 2.9      |      | ns    |
| t <sub>HPWL</sub>                          | Minimum Pulse Width Low                              | 1.6      |      | 1.8      |      | 2.1        |      | 2.9      |      | ns    |
| t <sub>HCKSW</sub>                         | Maximum Skew                                         | 0.4      |      | 0.4      |      | 0.5        |      | 0.7      |      | ns    |
| t <sub>HP</sub>                            | Minimum Period                                       | 3.2      |      | 3.6      |      | 4.2        |      | 5.8      |      | ns    |
| f <sub>HMAX</sub>                          | Maximum Frequency                                    | 313      |      | 278      |      | 238        |      | 172      |      | MHz   |
| Routed Array Clock Networks                |                                                      |          |      |          |      |            |      |          |      |       |
| t <sub>RCKH</sub>                          | Input Low to High (Light Load) (Pad to R-cell Input) | 1.0      |      | 1.1      |      | 1.3        |      | 1.8      |      | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (Light Load) (Pad to R-cell Input) | 1.1      |      | 1.2      |      | 1.4        |      | 2.0      |      | ns    |
| t <sub>RCKH</sub>                          | Input Low to High (50% Load) (Pad to R-cell Input)   | 1.0      |      | 1.1      |      | 1.3        |      | 1.8      |      | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (50% Load) (Pad to R-cell Input)   | 1.1      |      | 1.2      |      | 1.4        |      | 2.0      |      | ns    |
| t <sub>RCKH</sub>                          | Input Low to High (100% Load) (Pad to R-cell Input)  | 1.1      |      | 1.2      |      | 1.4        |      | 2.0      |      | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (100% Load) (Pad to R-cell Input)  | 1.3      |      | 1.5      |      | 1.7        |      | 2.4      |      | ns    |
| t <sub>RPWH</sub>                          | Minimum Pulse Width High                             | 1.6      |      | 1.8      |      | 2.1        |      | 2.9      |      | ns    |
| t <sub>RPWL</sub>                          | Minimum Pulse Width Low                              | 1.6      |      | 1.8      |      | 2.1        |      | 2.9      |      | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (Light Load)                            | 0.7      |      | 0.8      |      | 0.9        |      | 1.3      |      | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (50% Load)                              | 0.7      |      | 0.8      |      | 0.9        |      | 1.3      |      | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (100% Load)                             | 0.9      |      | 1.0      |      | 1.2        |      | 1.7      |      | ns    |

Table 2-18 • A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.3\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter                                        | Description                      | –2 Speed |       | –1 Speed |       | Std. Speed |       | –F Speed |       | Units |
|--------------------------------------------------|----------------------------------|----------|-------|----------|-------|------------|-------|----------|-------|-------|
|                                                  |                                  | Min.     | Max.  | Min.     | Max.  | Min.       | Max.  | Min.     | Max.  |       |
| 2.5 V LVCMOS Output Module Timing <sup>1,2</sup> |                                  |          |       |          |       |            |       |          |       |       |
| t <sub>DLH</sub>                                 | Data-to-Pad Low to High          |          | 3.9   |          | 4.4   |            | 5.2   |          | 7.2   | ns    |
| t <sub>DHL</sub>                                 | Data-to-Pad High to Low          |          | 3.0   |          | 3.4   |            | 3.9   |          | 5.5   | ns    |
| t <sub>DHLS</sub>                                | Data-to-Pad High to Low—low slew |          | 13.3  |          | 15.1  |            | 17.7  |          | 24.8  | ns    |
| t <sub>ENZL</sub>                                | Enable-to-Pad, Z to L            |          | 2.8   |          | 3.2   |            | 3.7   |          | 5.2   | ns    |
| t <sub>ENZLS</sub>                               | Data-to-Pad, Z to L—low slew     |          | 13.7  |          | 15.5  |            | 18.2  |          | 25.5  | ns    |
| t <sub>ENZH</sub>                                | Enable-to-Pad, Z to H            |          | 3.9   |          | 4.4   |            | 5.2   |          | 7.2   | ns    |
| t <sub>ENLZ</sub>                                | Enable-to-Pad, L to Z            |          | 2.5   |          | 2.8   |            | 3.3   |          | 4.7   | ns    |
| t <sub>ENHZ</sub>                                | Enable-to-Pad, H to Z            |          | 3.0   |          | 3.4   |            | 3.9   |          | 5.5   | ns    |
| d <sub>TLH</sub> <sup>3</sup>                    | Delta Low to High                |          | 0.037 |          | 0.043 |            | 0.051 |          | 0.071 | ns/pF |
| d <sub>THL</sub> <sup>3</sup>                    | Delta High to Low                |          | 0.017 |          | 0.023 |            | 0.023 |          | 0.037 | ns/pF |
| d <sub>THLS</sub> <sup>3</sup>                   | Delta High to Low—low slew       |          | 0.06  |          | 0.071 |            | 0.086 |          | 0.117 | ns/pF |

**Note:**

- Delays based on 35 pF loading.
- The equivalent I/O Attribute Editor settings for 2.5 V LVCMOS is 2.5 V LVTTTL in the software.
- To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HL|HL|HLS]})$$
where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[HL|HL|HLS]}$  is the worst case delta value from the datasheet in ns/pF.

**Table 2-34 • A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

| Parameter                                 | Description                      | –3 Speed <sup>1</sup> |      | –2 Speed |      | –1 Speed |      | Std. Speed |      | –F Speed |      | Units |
|-------------------------------------------|----------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
|                                           |                                  | Min.                  | Max. | Min.     | Max. | Min.     | Max. | Min.       | Max. | Min.     | Max. |       |
| 5 V PCI Output Module Timing <sup>2</sup> |                                  |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>DLH</sub>                          | Data-to-Pad Low to High          | 2.1                   |      | 2.4      |      | 2.8      |      | 3.2        |      | 4.5      |      | ns    |
| t <sub>DHL</sub>                          | Data-to-Pad High to Low          | 2.8                   |      | 3.2      |      | 3.6      |      | 4.2        |      | 5.9      |      | ns    |
| t <sub>ENZL</sub>                         | Enable-to-Pad, Z to L            | 1.3                   |      | 1.5      |      | 1.7      |      | 2.0        |      | 2.8      |      | ns    |
| t <sub>ENZH</sub>                         | Enable-to-Pad, Z to H            | 2.1                   |      | 2.4      |      | 2.8      |      | 3.2        |      | 4.5      |      | ns    |
| t <sub>ENLZ</sub>                         | Enable-to-Pad, L to Z            | 3.0                   |      | 3.5      |      | 3.9      |      | 4.6        |      | 6.4      |      | ns    |
| t <sub>ENHZ</sub>                         | Enable-to-Pad, H to Z            | 2.8                   |      | 3.2      |      | 3.6      |      | 4.2        |      | 5.9      |      | ns    |
| d <sub>TLH</sub> <sup>3</sup>             | Delta Low to High                | 0.016                 |      | 0.016    |      | 0.02     |      | 0.022      |      | 0.032    |      | ns/pF |
| d <sub>THL</sub> <sup>3</sup>             | Delta High to Low                | 0.026                 |      | 0.03     |      | 0.032    |      | 0.04       |      | 0.052    |      | ns/pF |
| 5 V TTL Output Module Timing <sup>4</sup> |                                  |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>DLH</sub>                          | Data-to-Pad Low to High          | 1.9                   |      | 2.2      |      | 2.5      |      | 2.9        |      | 4.1      |      | ns    |
| t <sub>DHL</sub>                          | Data-to-Pad High to Low          | 2.5                   |      | 2.9      |      | 3.3      |      | 3.9        |      | 5.4      |      | ns    |
| t <sub>DHLS</sub>                         | Data-to-Pad High to Low—low slew | 6.6                   |      | 7.6      |      | 8.6      |      | 10.1       |      | 14.2     |      | ns    |
| t <sub>ENZL</sub>                         | Enable-to-Pad, Z to L            | 2.1                   |      | 2.4      |      | 2.7      |      | 3.2        |      | 4.5      |      | ns    |
| t <sub>ENZLS</sub>                        | Enable-to-Pad, Z to L—low slew   | 7.4                   |      | 8.4      |      | 9.5      |      | 11.0       |      | 15.4     |      | ns    |
| t <sub>ENZH</sub>                         | Enable-to-Pad, Z to H            | 1.9                   |      | 2.2      |      | 2.5      |      | 2.9        |      | 4.1      |      | ns    |
| t <sub>ENLZ</sub>                         | Enable-to-Pad, L to Z            | 3.6                   |      | 4.2      |      | 4.7      |      | 5.6        |      | 7.8      |      | ns    |
| t <sub>ENHZ</sub>                         | Enable-to-Pad, H to Z            | 2.5                   |      | 2.9      |      | 3.3      |      | 3.9        |      | 5.4      |      | ns    |
| d <sub>TLH</sub> <sup>3</sup>             | Delta Low to High                | 0.014                 |      | 0.017    |      | 0.017    |      | 0.023      |      | 0.031    |      | ns/pF |
| d <sub>THL</sub> <sup>3</sup>             | Delta High to Low                | 0.023                 |      | 0.029    |      | 0.031    |      | 0.037      |      | 0.051    |      | ns/pF |
| d <sub>THLS</sub> <sup>3</sup>            | Delta High to Low—low slew       | 0.043                 |      | 0.046    |      | 0.057    |      | 0.066      |      | 0.089    |      | ns/pF |

**Notes:**

1. All –3 speed grades have been discontinued.
2. Delays based on 50 pF loading.
3. To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the  $V_{CCI}$  value into the following equation:  

$$\text{Slew Rate [V/ns]} = (0.1 * V_{CCI} - 0.9 * V_{CCI}) / (C_{load} * d_{T[HLH|HLS]})$$
 where  $C_{load}$  is the load capacitance driven by the I/O in pF  
 $d_{T[HLH|HLS]}$  is the worst case delta value from the datasheet in ns/pF.
4. Delays based on 35 pF loading.

**Table 2-35 • A54SX72A Timing Characteristics**
**(Worst-Case Commercial Conditions,  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

| Parameter                              | Description                           | -3 Speed <sup>1</sup> |      | -2 Speed |      | -1 Speed |      | Std. Speed |      | -F Speed |      | Units |
|----------------------------------------|---------------------------------------|-----------------------|------|----------|------|----------|------|------------|------|----------|------|-------|
|                                        |                                       | Min.                  | Max. | Min.     | Max. | Min.     | Max. | Min.       | Max. | Min.     | Max. |       |
| C-Cell Propagation Delays <sup>2</sup> |                                       |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>PD</sub>                        | Internal Array Module                 | 1.0                   |      | 1.1      |      | 1.3      |      | 1.5        |      | 2.0      |      | ns    |
| Predicted Routing Delays <sup>3</sup>  |                                       |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>DC</sub>                        | FO = 1 Routing Delay, Direct Connect  | 0.1                   |      | 0.1      |      | 0.1      |      | 0.1        |      | 0.1      |      | ns    |
| t <sub>FC</sub>                        | FO = 1 Routing Delay, Fast Connect    | 0.3                   |      | 0.3      |      | 0.3      |      | 0.4        |      | 0.6      |      | ns    |
| t <sub>RD1</sub>                       | FO = 1 Routing Delay                  | 0.3                   |      | 0.3      |      | 0.4      |      | 0.5        |      | 0.7      |      | ns    |
| t <sub>RD2</sub>                       | FO = 2 Routing Delay                  | 0.4                   |      | 0.5      |      | 0.6      |      | 0.7        |      | 1        |      | ns    |
| t <sub>RD3</sub>                       | FO = 3 Routing Delay                  | 0.5                   |      | 0.7      |      | 0.8      |      | 0.9        |      | 1.3      |      | ns    |
| t <sub>RD4</sub>                       | FO = 4 Routing Delay                  | 0.7                   |      | 0.9      |      | 1        |      | 1.1        |      | 1.5      |      | ns    |
| t <sub>RD8</sub>                       | FO = 8 Routing Delay                  | 1.2                   |      | 1.5      |      | 1.7      |      | 2.1        |      | 2.9      |      | ns    |
| t <sub>RD12</sub>                      | FO = 12 Routing Delay                 | 1.7                   |      | 2.2      |      | 2.5      |      | 3          |      | 4.2      |      | ns    |
| R-Cell Timing                          |                                       |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>RCO</sub>                       | Sequential Clock-to-Q                 | 0.7                   |      | 0.8      |      | 0.9      |      | 1.1        |      | 1.5      |      | ns    |
| t <sub>CLR</sub>                       | Asynchronous Clear-to-Q               | 0.6                   |      | 0.7      |      | 0.7      |      | 0.9        |      | 1.2      |      | ns    |
| t <sub>PRESET</sub>                    | Asynchronous Preset-to-Q              | 0.7                   |      | 0.8      |      | 0.8      |      | 1.0        |      | 1.4      |      | ns    |
| t <sub>SUD</sub>                       | Flip-Flop Data Input Set-Up           | 0.7                   |      | 0.8      |      | 0.9      |      | 1.0        |      | 1.4      |      | ns    |
| t <sub>HD</sub>                        | Flip-Flop Data Input Hold             | 0.0                   |      | 0.0      |      | 0.0      |      | 0.0        |      | 0.0      |      | ns    |
| t <sub>WASYN</sub>                     | Asynchronous Pulse Width              | 1.3                   |      | 1.5      |      | 1.7      |      | 2.0        |      | 2.8      |      | ns    |
| t <sub>RECASYN</sub>                   | Asynchronous Recovery Time            | 0.3                   |      | 0.4      |      | 0.4      |      | 0.5        |      | 0.7      |      | ns    |
| t <sub>HASYN</sub>                     | Asynchronous Hold Time                | 0.3                   |      | 0.3      |      | 0.3      |      | 0.4        |      | 0.6      |      | ns    |
| t <sub>MPW</sub>                       | Clock Minimum Pulse Width             | 1.5                   |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| Input Module Propagation Delays        |                                       |                       |      |          |      |          |      |            |      |          |      |       |
| t <sub>INYH</sub>                      | Input Data Pad to Y High 2.5 V LVCMOS | 0.6                   |      | 0.7      |      | 0.8      |      | 0.9        |      | 1.3      |      | ns    |
| t <sub>INYL</sub>                      | Input Data Pad to Y Low 2.5 V LVCMOS  | 0.8                   |      | 1.0      |      | 1.1      |      | 1.3        |      | 1.7      |      | ns    |
| t <sub>INYH</sub>                      | Input Data Pad to Y High 3.3 V PCI    | 0.6                   |      | 0.7      |      | 0.7      |      | 0.9        |      | 1.2      |      | ns    |
| t <sub>INYL</sub>                      | Input Data Pad to Y Low 3.3 V PCI     | 0.7                   |      | 0.8      |      | 0.9      |      | 1.0        |      | 1.4      |      | ns    |
| t <sub>INYH</sub>                      | Input Data Pad to Y High 3.3 V LVTTTL | 0.7                   |      | 0.7      |      | 0.8      |      | 1.0        |      | 1.4      |      | ns    |
| t <sub>INYL</sub>                      | Input Data Pad to Y Low 3.3 V LVTTTL  | 1.0                   |      | 1.2      |      | 1.3      |      | 1.5        |      | 2.1      |      | ns    |

**Notes:**

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-36 • A54SX72A Timing Characteristics (Continued)  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.25\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter   | Description                                            | –3 Speed* |      | –2 Speed |      | –1 Speed |      | Std. Speed |      | –F Speed |      | Units |
|-------------|--------------------------------------------------------|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
|             |                                                        | Min.      | Max. | Min.     | Max. | Min.     | Max. | Min.       | Max. | Min.     | Max. |       |
| $t_{QCKH}$  | Input Low to High (100% Load)<br>(Pad to R-cell Input) |           | 3.0  |          | 3.4  |          | 3.9  |            | 4.6  |          | 6.4  | ns    |
| $t_{QCHKL}$ | Input High to Low (100% Load)<br>(Pad to R-cell Input) |           | 2.9  |          | 3.4  |          | 3.8  |            | 4.5  |          | 6.3  | ns    |
| $t_{QPWH}$  | Minimum Pulse Width High                               | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| $t_{QPWL}$  | Minimum Pulse Width Low                                | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| $t_{QCKSW}$ | Maximum Skew (Light Load)                              |           | 0.2  |          | 0.3  |          | 0.3  |            | 0.3  |          | 0.5  | ns    |
| $t_{QCKSW}$ | Maximum Skew (50% Load)                                |           | 0.4  |          | 0.5  |          | 0.5  |            | 0.6  |          | 0.9  | ns    |
| $t_{QCKSW}$ | Maximum Skew (100% Load)                               |           | 0.4  |          | 0.5  |          | 0.5  |            | 0.6  |          | 0.9  | ns    |

**Note:** \*All –3 speed grades have been discontinued.

Table 2-38 • **A54SX72A Timing Characteristics**  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

| Parameter                                  | Description                                          | –3 Speed* |      | –2 Speed |      | –1 Speed |      | Std. Speed |      | –F Speed |      | Units |
|--------------------------------------------|------------------------------------------------------|-----------|------|----------|------|----------|------|------------|------|----------|------|-------|
|                                            |                                                      | Min.      | Max. | Min.     | Max. | Min.     | Max. | Min.       | Max. | Min.     | Max. |       |
| Dedicated (Hardwired) Array Clock Networks |                                                      |           |      |          |      |          |      |            |      |          |      |       |
| t <sub>HCKH</sub>                          | Input Low to High (Pad to R-cell Input)              |           | 1.6  |          | 1.8  |          | 2.1  |            | 2.4  |          | 3.8  | ns    |
| t <sub>HCKL</sub>                          | Input High to Low (Pad to R-cell Input)              |           | 1.6  |          | 1.9  |          | 2.1  |            | 2.5  |          | 3.8  | ns    |
| t <sub>HPWH</sub>                          | Minimum Pulse Width High                             | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| t <sub>HPWL</sub>                          | Minimum Pulse Width Low                              | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| t <sub>HCKSW</sub>                         | Maximum Skew                                         |           | 1.4  |          | 1.6  |          | 1.8  |            | 2.1  |          | 3.3  | ns    |
| t <sub>HP</sub>                            | Minimum Period                                       | 3.0       |      | 3.4      |      | 4.0      |      | 4.6        |      | 6.4      |      | ns    |
| f <sub>HMAX</sub>                          | Maximum Frequency                                    |           | 333  |          | 294  |          | 250  |            | 217  |          | 156  | MHz   |
| Routed Array Clock Networks                |                                                      |           |      |          |      |          |      |            |      |          |      |       |
| t <sub>RCKH</sub>                          | Input Low to High (Light Load) (Pad to R-cell Input) |           | 2.3  |          | 2.6  |          | 3.0  |            | 3.5  |          | 4.9  | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (Light Load) (Pad to R-cell Input) |           | 2.8  |          | 3.2  |          | 3.6  |            | 4.3  |          | 6.0  | ns    |
| t <sub>RCKH</sub>                          | Input Low to High (50% Load) (Pad to R-cell Input)   |           | 2.5  |          | 2.9  |          | 3.2  |            | 3.8  |          | 5.3  | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (50% Load) (Pad to R-cell Input)   |           | 3.0  |          | 3.4  |          | 3.9  |            | 4.6  |          | 6.4  | ns    |
| t <sub>RCKH</sub>                          | Input Low to High (100% Load) (Pad to R-cell Input)  |           | 2.6  |          | 3.0  |          | 3.4  |            | 3.9  |          | 5.5  | ns    |
| t <sub>RCKL</sub>                          | Input High to Low (100% Load) (Pad to R-cell Input)  |           | 3.2  |          | 3.6  |          | 4.1  |            | 4.8  |          | 6.8  | ns    |
| t <sub>RPWH</sub>                          | Minimum Pulse Width High                             | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| t <sub>RPWL</sub>                          | Minimum Pulse Width Low                              | 1.5       |      | 1.7      |      | 2.0      |      | 2.3        |      | 3.2      |      | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (Light Load)                            |           | 1.9  |          | 2.2  |          | 2.5  |            | 3.0  |          | 4.1  | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (50% Load)                              |           | 1.9  |          | 2.2  |          | 2.5  |            | 3.0  |          | 4.1  | ns    |
| t <sub>RCKSW</sub>                         | Maximum Skew (100% Load)                             |           | 1.9  |          | 2.2  |          | 2.5  |            | 3.0  |          | 4.1  | ns    |
| Quadrant Array Clock Networks              |                                                      |           |      |          |      |          |      |            |      |          |      |       |
| t <sub>QCKH</sub>                          | Input Low to High (Light Load) (Pad to R-cell Input) |           | 1.2  |          | 1.4  |          | 1.6  |            | 1.8  |          | 2.6  | ns    |
| t <sub>QCHKL</sub>                         | Input High to Low (Light Load) (Pad to R-cell Input) |           | 1.3  |          | 1.4  |          | 1.6  |            | 1.9  |          | 2.7  | ns    |
| t <sub>QCKH</sub>                          | Input Low to High (50% Load) (Pad to R-cell Input)   |           | 1.4  |          | 1.6  |          | 1.8  |            | 2.1  |          | 3.0  | ns    |
| t <sub>QCHKL</sub>                         | Input High to Low (50% Load) (Pad to R-cell Input)   |           | 1.4  |          | 1.7  |          | 1.9  |            | 2.2  |          | 3.1  | ns    |

**Note:** \*All –3 speed grades have been discontinued.

**208-Pin PQFP**

| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
|------------|-------------------|-------------------|-------------------|-------------------|
| 141        | NC                | I/O               | I/O               | I/O               |
| 142        | I/O               | I/O               | I/O               | I/O               |
| 143        | NC                | I/O               | I/O               | I/O               |
| 144        | I/O               | I/O               | I/O               | I/O               |
| 145        | V <sub>CCA</sub>  | V <sub>CCA</sub>  | V <sub>CCA</sub>  | V <sub>CCA</sub>  |
| 146        | GND               | GND               | GND               | GND               |
| 147        | I/O               | I/O               | I/O               | I/O               |
| 148        | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| 149        | I/O               | I/O               | I/O               | I/O               |
| 150        | I/O               | I/O               | I/O               | I/O               |
| 151        | I/O               | I/O               | I/O               | I/O               |
| 152        | I/O               | I/O               | I/O               | I/O               |
| 153        | I/O               | I/O               | I/O               | I/O               |
| 154        | I/O               | I/O               | I/O               | I/O               |
| 155        | NC                | I/O               | I/O               | I/O               |
| 156        | NC                | I/O               | I/O               | I/O               |
| 157        | GND               | GND               | GND               | GND               |
| 158        | I/O               | I/O               | I/O               | I/O               |
| 159        | I/O               | I/O               | I/O               | I/O               |
| 160        | I/O               | I/O               | I/O               | I/O               |
| 161        | I/O               | I/O               | I/O               | I/O               |
| 162        | I/O               | I/O               | I/O               | I/O               |
| 163        | I/O               | I/O               | I/O               | I/O               |
| 164        | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| 165        | I/O               | I/O               | I/O               | I/O               |
| 166        | I/O               | I/O               | I/O               | I/O               |
| 167        | NC                | I/O               | I/O               | I/O               |
| 168        | I/O               | I/O               | I/O               | I/O               |
| 169        | I/O               | I/O               | I/O               | I/O               |
| 170        | NC                | I/O               | I/O               | I/O               |
| 171        | I/O               | I/O               | I/O               | I/O               |
| 172        | I/O               | I/O               | I/O               | I/O               |
| 173        | NC                | I/O               | I/O               | I/O               |
| 174        | I/O               | I/O               | I/O               | I/O               |
| 175        | I/O               | I/O               | I/O               | I/O               |

**208-Pin PQFP**

| Pin Number | A54SX08A Function | A54SX16A Function | A54SX32A Function | A54SX72A Function |
|------------|-------------------|-------------------|-------------------|-------------------|
| 176        | NC                | I/O               | I/O               | I/O               |
| 177        | I/O               | I/O               | I/O               | I/O               |
| 178        | I/O               | I/O               | I/O               | QCLKD             |
| 179        | I/O               | I/O               | I/O               | I/O               |
| 180        | CLKA              | CLKA              | CLKA              | CLKA              |
| 181        | CLKB              | CLKB              | CLKB              | CLKB              |
| 182        | NC                | NC                | NC                | NC                |
| 183        | GND               | GND               | GND               | GND               |
| 184        | V <sub>CCA</sub>  | V <sub>CCA</sub>  | V <sub>CCA</sub>  | V <sub>CCA</sub>  |
| 185        | GND               | GND               | GND               | GND               |
| 186        | PRA, I/O          | PRA, I/O          | PRA, I/O          | PRA, I/O          |
| 187        | I/O               | I/O               | I/O               | V <sub>CCI</sub>  |
| 188        | I/O               | I/O               | I/O               | I/O               |
| 189        | NC                | I/O               | I/O               | I/O               |
| 190        | I/O               | I/O               | I/O               | QCLKC             |
| 191        | I/O               | I/O               | I/O               | I/O               |
| 192        | NC                | I/O               | I/O               | I/O               |
| 193        | I/O               | I/O               | I/O               | I/O               |
| 194        | I/O               | I/O               | I/O               | I/O               |
| 195        | NC                | I/O               | I/O               | I/O               |
| 196        | I/O               | I/O               | I/O               | I/O               |
| 197        | I/O               | I/O               | I/O               | I/O               |
| 198        | NC                | I/O               | I/O               | I/O               |
| 199        | I/O               | I/O               | I/O               | I/O               |
| 200        | I/O               | I/O               | I/O               | I/O               |
| 201        | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| 202        | NC                | I/O               | I/O               | I/O               |
| 203        | NC                | I/O               | I/O               | I/O               |
| 204        | I/O               | I/O               | I/O               | I/O               |
| 205        | NC                | I/O               | I/O               | I/O               |
| 206        | I/O               | I/O               | I/O               | I/O               |
| 207        | I/O               | I/O               | I/O               | I/O               |
| 208        | TCK, I/O          | TCK, I/O          | TCK, I/O          | TCK, I/O          |

| 100-TQFP   |                      |                      |                      |
|------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX08A<br>Function | A54SX16A<br>Function | A54SX32A<br>Function |
| 1          | GND                  | GND                  | GND                  |
| 2          | TDI, I/O             | TDI, I/O             | TDI, I/O             |
| 3          | I/O                  | I/O                  | I/O                  |
| 4          | I/O                  | I/O                  | I/O                  |
| 5          | I/O                  | I/O                  | I/O                  |
| 6          | I/O                  | I/O                  | I/O                  |
| 7          | TMS                  | TMS                  | TMS                  |
| 8          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| 9          | GND                  | GND                  | GND                  |
| 10         | I/O                  | I/O                  | I/O                  |
| 11         | I/O                  | I/O                  | I/O                  |
| 12         | I/O                  | I/O                  | I/O                  |
| 13         | I/O                  | I/O                  | I/O                  |
| 14         | I/O                  | I/O                  | I/O                  |
| 15         | I/O                  | I/O                  | I/O                  |
| 16         | TRST, I/O            | TRST, I/O            | TRST, I/O            |
| 17         | I/O                  | I/O                  | I/O                  |
| 18         | I/O                  | I/O                  | I/O                  |
| 19         | I/O                  | I/O                  | I/O                  |
| 20         | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| 21         | I/O                  | I/O                  | I/O                  |
| 22         | I/O                  | I/O                  | I/O                  |
| 23         | I/O                  | I/O                  | I/O                  |
| 24         | I/O                  | I/O                  | I/O                  |
| 25         | I/O                  | I/O                  | I/O                  |
| 26         | I/O                  | I/O                  | I/O                  |
| 27         | I/O                  | I/O                  | I/O                  |
| 28         | I/O                  | I/O                  | I/O                  |
| 29         | I/O                  | I/O                  | I/O                  |
| 30         | I/O                  | I/O                  | I/O                  |
| 31         | I/O                  | I/O                  | I/O                  |
| 32         | I/O                  | I/O                  | I/O                  |
| 33         | I/O                  | I/O                  | I/O                  |
| 34         | PRB, I/O             | PRB, I/O             | PRB, I/O             |
| 35         | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |

| 100-TQFP   |                      |                      |                      |
|------------|----------------------|----------------------|----------------------|
| Pin Number | A54SX08A<br>Function | A54SX16A<br>Function | A54SX32A<br>Function |
| 36         | GND                  | GND                  | GND                  |
| 37         | NC                   | NC                   | NC                   |
| 38         | I/O                  | I/O                  | I/O                  |
| 39         | HCLK                 | HCLK                 | HCLK                 |
| 40         | I/O                  | I/O                  | I/O                  |
| 41         | I/O                  | I/O                  | I/O                  |
| 42         | I/O                  | I/O                  | I/O                  |
| 43         | I/O                  | I/O                  | I/O                  |
| 44         | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| 45         | I/O                  | I/O                  | I/O                  |
| 46         | I/O                  | I/O                  | I/O                  |
| 47         | I/O                  | I/O                  | I/O                  |
| 48         | I/O                  | I/O                  | I/O                  |
| 49         | TDO, I/O             | TDO, I/O             | TDO, I/O             |
| 50         | I/O                  | I/O                  | I/O                  |
| 51         | GND                  | GND                  | GND                  |
| 52         | I/O                  | I/O                  | I/O                  |
| 53         | I/O                  | I/O                  | I/O                  |
| 54         | I/O                  | I/O                  | I/O                  |
| 55         | I/O                  | I/O                  | I/O                  |
| 56         | I/O                  | I/O                  | I/O                  |
| 57         | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |
| 58         | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| 59         | I/O                  | I/O                  | I/O                  |
| 60         | I/O                  | I/O                  | I/O                  |
| 61         | I/O                  | I/O                  | I/O                  |
| 62         | I/O                  | I/O                  | I/O                  |
| 63         | I/O                  | I/O                  | I/O                  |
| 64         | I/O                  | I/O                  | I/O                  |
| 65         | I/O                  | I/O                  | I/O                  |
| 66         | I/O                  | I/O                  | I/O                  |
| 67         | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |
| 68         | GND                  | GND                  | GND                  |
| 69         | GND                  | GND                  | GND                  |
| 70         | I/O                  | I/O                  | I/O                  |

## 144-Pin TQFP

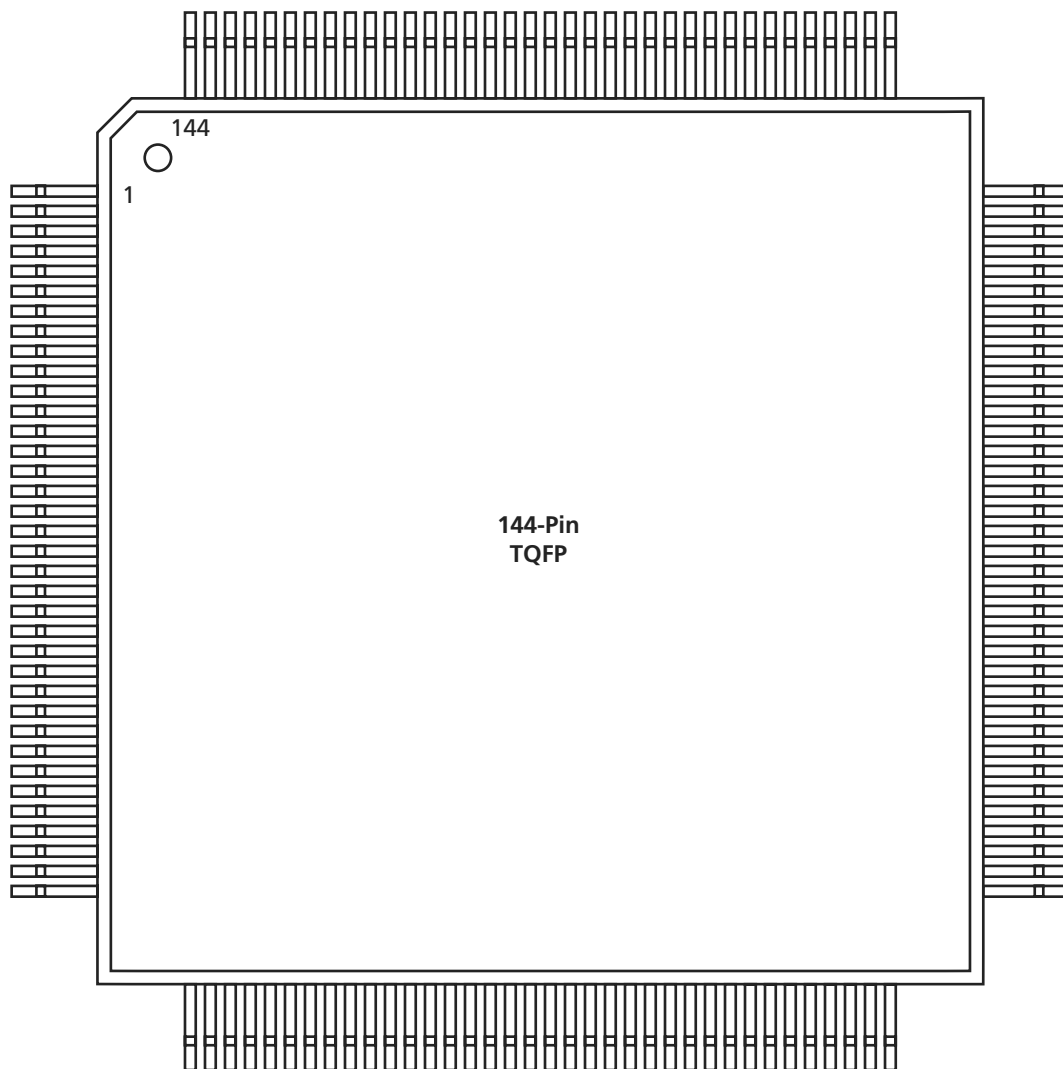


Figure 3-3 • 144-Pin TQFP (Top View)

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 256-Pin FBGA |                      |                      |                      |
|--------------|----------------------|----------------------|----------------------|
| Pin Number   | A545X16A<br>Function | A545X32A<br>Function | A545X72A<br>Function |
| E11          | I/O                  | I/O                  | I/O                  |
| E12          | I/O                  | I/O                  | I/O                  |
| E13          | NC                   | I/O                  | I/O                  |
| E14          | I/O                  | I/O                  | I/O                  |
| E15          | I/O                  | I/O                  | I/O                  |
| E16          | I/O                  | I/O                  | I/O                  |
| F1           | I/O                  | I/O                  | I/O                  |
| F2           | I/O                  | I/O                  | I/O                  |
| F3           | I/O                  | I/O                  | I/O                  |
| F4           | TMS                  | TMS                  | TMS                  |
| F5           | I/O                  | I/O                  | I/O                  |
| F6           | I/O                  | I/O                  | I/O                  |
| F7           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| F8           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| F9           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| F10          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| F11          | I/O                  | I/O                  | I/O                  |
| F12          | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |
| F13          | I/O                  | I/O                  | I/O                  |
| F14          | I/O                  | I/O                  | I/O                  |
| F15          | I/O                  | I/O                  | I/O                  |
| F16          | I/O                  | I/O                  | I/O                  |
| G1           | NC                   | I/O                  | I/O                  |
| G2           | I/O                  | I/O                  | I/O                  |
| G3           | NC                   | I/O                  | I/O                  |
| G4           | I/O                  | I/O                  | I/O                  |
| G5           | I/O                  | I/O                  | I/O                  |
| G6           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| G7           | GND                  | GND                  | GND                  |
| G8           | GND                  | GND                  | GND                  |
| G9           | GND                  | GND                  | GND                  |
| G10          | GND                  | GND                  | GND                  |
| G11          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| G12          | I/O                  | I/O                  | I/O                  |
| G13          | GND                  | GND                  | GND                  |
| G14          | NC                   | I/O                  | I/O                  |
| G15          | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |

| 256-Pin FBGA |                      |                      |                      |
|--------------|----------------------|----------------------|----------------------|
| Pin Number   | A545X16A<br>Function | A545X32A<br>Function | A545X72A<br>Function |
| G16          | I/O                  | I/O                  | I/O                  |
| H1           | I/O                  | I/O                  | I/O                  |
| H2           | I/O                  | I/O                  | I/O                  |
| H3           | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |
| H4           | TRST, I/O            | TRST, I/O            | TRST, I/O            |
| H5           | I/O                  | I/O                  | I/O                  |
| H6           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| H7           | GND                  | GND                  | GND                  |
| H8           | GND                  | GND                  | GND                  |
| H9           | GND                  | GND                  | GND                  |
| H10          | GND                  | GND                  | GND                  |
| H11          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| H12          | I/O                  | I/O                  | I/O                  |
| H13          | I/O                  | I/O                  | I/O                  |
| H14          | I/O                  | I/O                  | I/O                  |
| H15          | I/O                  | I/O                  | I/O                  |
| H16          | NC                   | I/O                  | I/O                  |
| J1           | NC                   | I/O                  | I/O                  |
| J2           | NC                   | I/O                  | I/O                  |
| J3           | NC                   | I/O                  | I/O                  |
| J4           | I/O                  | I/O                  | I/O                  |
| J5           | I/O                  | I/O                  | I/O                  |
| J6           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| J7           | GND                  | GND                  | GND                  |
| J8           | GND                  | GND                  | GND                  |
| J9           | GND                  | GND                  | GND                  |
| J10          | GND                  | GND                  | GND                  |
| J11          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| J12          | I/O                  | I/O                  | I/O                  |
| J13          | I/O                  | I/O                  | I/O                  |
| J14          | I/O                  | I/O                  | I/O                  |
| J15          | I/O                  | I/O                  | I/O                  |
| J16          | I/O                  | I/O                  | I/O                  |
| K1           | I/O                  | I/O                  | I/O                  |
| K2           | I/O                  | I/O                  | I/O                  |
| K3           | NC                   | I/O                  | I/O                  |
| K4           | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |

| 256-Pin FBGA |                      |                      |                      |
|--------------|----------------------|----------------------|----------------------|
| Pin Number   | A54SX16A<br>Function | A54SX32A<br>Function | A54SX72A<br>Function |
| K5           | I/O                  | I/O                  | I/O                  |
| K6           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| K7           | GND                  | GND                  | GND                  |
| K8           | GND                  | GND                  | GND                  |
| K9           | GND                  | GND                  | GND                  |
| K10          | GND                  | GND                  | GND                  |
| K11          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| K12          | I/O                  | I/O                  | I/O                  |
| K13          | I/O                  | I/O                  | I/O                  |
| K14          | I/O                  | I/O                  | I/O                  |
| K15          | NC                   | I/O                  | I/O                  |
| K16          | I/O                  | I/O                  | I/O                  |
| L1           | I/O                  | I/O                  | I/O                  |
| L2           | I/O                  | I/O                  | I/O                  |
| L3           | I/O                  | I/O                  | I/O                  |
| L4           | I/O                  | I/O                  | I/O                  |
| L5           | I/O                  | I/O                  | I/O                  |
| L6           | I/O                  | I/O                  | I/O                  |
| L7           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| L8           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| L9           | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| L10          | V <sub>CCI</sub>     | V <sub>CCI</sub>     | V <sub>CCI</sub>     |
| L11          | I/O                  | I/O                  | I/O                  |
| L12          | I/O                  | I/O                  | I/O                  |
| L13          | I/O                  | I/O                  | I/O                  |
| L14          | I/O                  | I/O                  | I/O                  |
| L15          | I/O                  | I/O                  | I/O                  |
| L16          | NC                   | I/O                  | I/O                  |
| M1           | I/O                  | I/O                  | I/O                  |
| M2           | I/O                  | I/O                  | I/O                  |
| M3           | I/O                  | I/O                  | I/O                  |
| M4           | I/O                  | I/O                  | I/O                  |
| M5           | I/O                  | I/O                  | I/O                  |
| M6           | I/O                  | I/O                  | I/O                  |
| M7           | I/O                  | I/O                  | QCLKA                |
| M8           | PRB, I/O             | PRB, I/O             | PRB, I/O             |
| M9           | I/O                  | I/O                  | I/O                  |

| 256-Pin FBGA |                      |                      |                      |
|--------------|----------------------|----------------------|----------------------|
| Pin Number   | A54SX16A<br>Function | A54SX32A<br>Function | A54SX72A<br>Function |
| M10          | I/O                  | I/O                  | I/O                  |
| M11          | I/O                  | I/O                  | I/O                  |
| M12          | NC                   | I/O                  | I/O                  |
| M13          | I/O                  | I/O                  | I/O                  |
| M14          | NC                   | I/O                  | I/O                  |
| M15          | I/O                  | I/O                  | I/O                  |
| M16          | I/O                  | I/O                  | I/O                  |
| N1           | I/O                  | I/O                  | I/O                  |
| N2           | I/O                  | I/O                  | I/O                  |
| N3           | I/O                  | I/O                  | I/O                  |
| N4           | I/O                  | I/O                  | I/O                  |
| N5           | I/O                  | I/O                  | I/O                  |
| N6           | I/O                  | I/O                  | I/O                  |
| N7           | I/O                  | I/O                  | I/O                  |
| N8           | I/O                  | I/O                  | I/O                  |
| N9           | I/O                  | I/O                  | I/O                  |
| N10          | I/O                  | I/O                  | I/O                  |
| N11          | I/O                  | I/O                  | I/O                  |
| N12          | I/O                  | I/O                  | I/O                  |
| N13          | I/O                  | I/O                  | I/O                  |
| N14          | I/O                  | I/O                  | I/O                  |
| N15          | I/O                  | I/O                  | I/O                  |
| N16          | I/O                  | I/O                  | I/O                  |
| P1           | I/O                  | I/O                  | I/O                  |
| P2           | GND                  | GND                  | GND                  |
| P3           | I/O                  | I/O                  | I/O                  |
| P4           | I/O                  | I/O                  | I/O                  |
| P5           | NC                   | I/O                  | I/O                  |
| P6           | I/O                  | I/O                  | I/O                  |
| P7           | I/O                  | I/O                  | I/O                  |
| P8           | I/O                  | I/O                  | I/O                  |
| P9           | I/O                  | I/O                  | I/O                  |
| P10          | NC                   | I/O                  | I/O                  |
| P11          | I/O                  | I/O                  | I/O                  |
| P12          | I/O                  | I/O                  | I/O                  |
| P13          | V <sub>CCA</sub>     | V <sub>CCA</sub>     | V <sub>CCA</sub>     |
| P14          | I/O                  | I/O                  | I/O                  |

| 484-Pin FBGA |                   |                   |
|--------------|-------------------|-------------------|
| Pin Number   | A54SX32A Function | A54SX72A Function |
| AD18         | I/O               | I/O               |
| AD19         | I/O               | I/O               |
| AD20         | I/O               | I/O               |
| AD21         | I/O               | I/O               |
| AD22         | I/O               | I/O               |
| AD23         | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| AD24         | NC*               | I/O               |
| AD25         | NC*               | I/O               |
| AD26         | NC*               | I/O               |
| AE1          | NC*               | NC                |
| AE2          | I/O               | I/O               |
| AE3          | NC*               | I/O               |
| AE4          | NC*               | I/O               |
| AE5          | NC*               | I/O               |
| AE6          | NC*               | I/O               |
| AE7          | I/O               | I/O               |
| AE8          | I/O               | I/O               |
| AE9          | I/O               | I/O               |
| AE10         | I/O               | I/O               |
| AE11         | NC*               | I/O               |
| AE12         | I/O               | I/O               |
| AE13         | I/O               | I/O               |
| AE14         | I/O               | I/O               |
| AE15         | NC*               | I/O               |
| AE16         | NC*               | I/O               |
| AE17         | I/O               | I/O               |
| AE18         | I/O               | I/O               |
| AE19         | I/O               | I/O               |
| AE20         | I/O               | I/O               |
| AE21         | NC*               | I/O               |
| AE22         | NC*               | I/O               |
| AE23         | NC*               | I/O               |
| AE24         | NC*               | I/O               |
| AE25         | NC*               | NC                |
| AE26         | NC*               | NC                |

| 484-Pin FBGA |                   |                   |
|--------------|-------------------|-------------------|
| Pin Number   | A54SX32A Function | A54SX72A Function |
| AF1          | NC*               | NC                |
| AF2          | NC*               | NC                |
| AF3          | NC                | I/O               |
| AF4          | NC*               | I/O               |
| AF5          | NC*               | I/O               |
| AF6          | NC*               | I/O               |
| AF7          | I/O               | I/O               |
| AF8          | I/O               | I/O               |
| AF9          | I/O               | I/O               |
| AF10         | I/O               | I/O               |
| AF11         | NC*               | I/O               |
| AF12         | NC*               | NC                |
| AF13         | HCLK              | HCLK              |
| AF14         | I/O               | QCLKB             |
| AF15         | NC*               | I/O               |
| AF16         | NC*               | I/O               |
| AF17         | I/O               | I/O               |
| AF18         | I/O               | I/O               |
| AF19         | I/O               | I/O               |
| AF20         | NC*               | I/O               |
| AF21         | NC*               | I/O               |
| AF22         | NC*               | I/O               |
| AF23         | NC*               | I/O               |
| AF24         | NC*               | I/O               |
| AF25         | NC*               | NC                |
| AF26         | NC*               | NC                |
| B1           | NC*               | NC                |
| B2           | NC*               | NC                |
| B3           | NC*               | I/O               |
| B4           | NC*               | I/O               |
| B5           | NC*               | I/O               |
| B6           | I/O               | I/O               |
| B7           | I/O               | I/O               |
| B8           | I/O               | I/O               |
| B9           | I/O               | I/O               |

| 484-Pin FBGA |                   |                   |
|--------------|-------------------|-------------------|
| Pin Number   | A54SX32A Function | A54SX72A Function |
| B10          | I/O               | I/O               |
| B11          | NC*               | I/O               |
| B12          | NC*               | I/O               |
| B13          | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| B14          | CLKA              | CLKA              |
| B15          | NC*               | I/O               |
| B16          | NC*               | I/O               |
| B17          | I/O               | I/O               |
| B18          | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| B19          | I/O               | I/O               |
| B20          | I/O               | I/O               |
| B21          | NC*               | I/O               |
| B22          | NC*               | I/O               |
| B23          | NC*               | I/O               |
| B24          | NC*               | I/O               |
| B25          | I/O               | I/O               |
| B26          | NC*               | NC                |
| C1           | NC*               | I/O               |
| C2           | NC*               | I/O               |
| C3           | NC*               | I/O               |
| C4           | NC*               | I/O               |
| C5           | I/O               | I/O               |
| C6           | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| C7           | I/O               | I/O               |
| C8           | I/O               | I/O               |
| C9           | V <sub>CCI</sub>  | V <sub>CCI</sub>  |
| C10          | I/O               | I/O               |
| C11          | I/O               | I/O               |
| C12          | I/O               | I/O               |
| C13          | PRA, I/O          | PRA, I/O          |
| C14          | I/O               | I/O               |
| C15          | I/O               | QCLKD             |
| C16          | I/O               | I/O               |
| C17          | I/O               | I/O               |
| C18          | I/O               | I/O               |

**Note:** \*These pins must be left floating on the A54SX32A device.