Microsemi Corporation - A54SX32A-1TQG176 Datasheet

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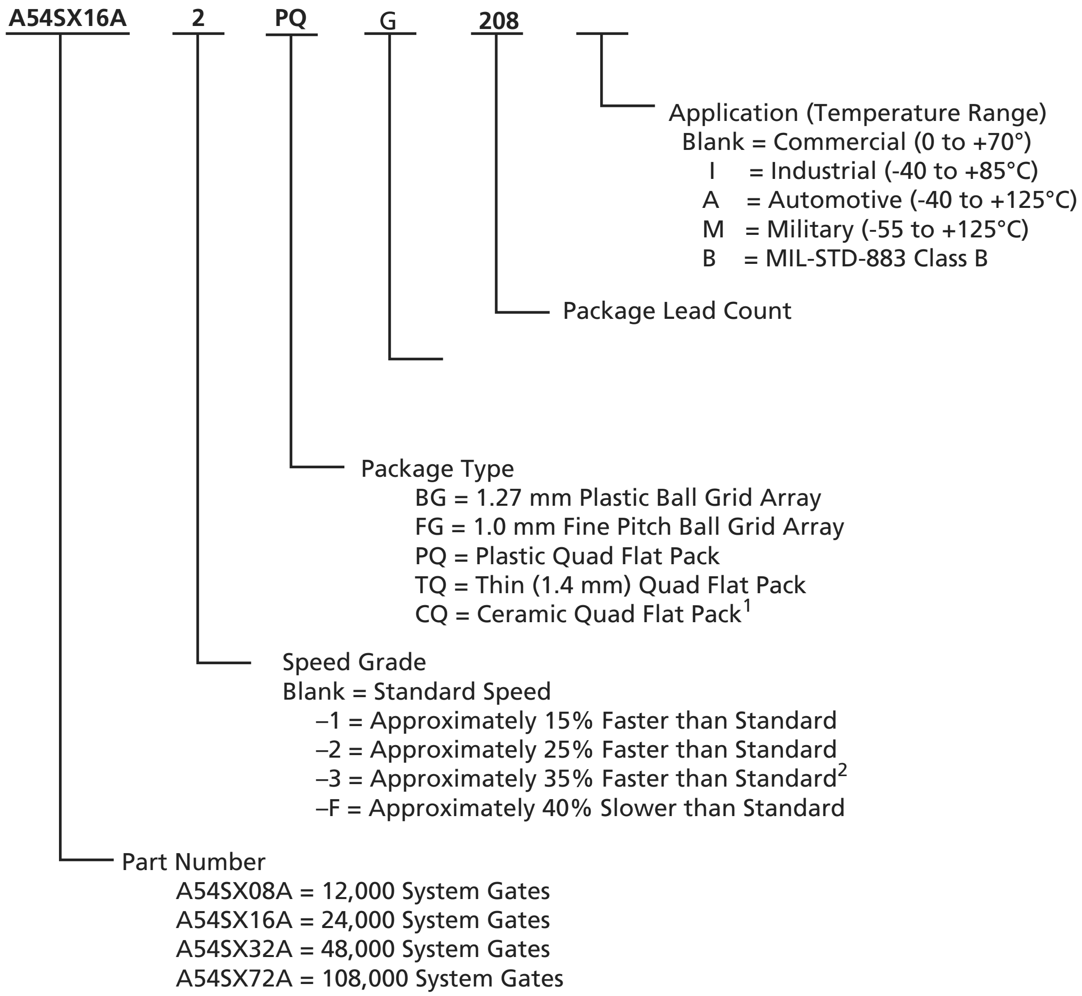
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	147
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx32a-1tqg176

Ordering Information



Application (Temperature Range)
Blank = Commercial (0 to +70°)
I = Industrial (-40 to +85°C)
A = Automotive (-40 to +125°C)
M = Military (-55 to +125°C)
B = MIL-STD-883 Class B

Package Lead Count

Package Type
BG = 1.27 mm Plastic Ball Grid Array
FG = 1.0 mm Fine Pitch Ball Grid Array
PQ = Plastic Quad Flat Pack
TQ = Thin (1.4 mm) Quad Flat Pack
CQ = Ceramic Quad Flat Pack[1]

Speed Grade
Blank = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard[2]
–F = Approximately 40% Slower than Standard

Part Number
A54SX08A = 12,000 System Gates
A54SX16A = 24,000 System Gates
A54SX32A = 48,000 System Gates
A54SX72A = 108,000 System Gates

Notes:

1. *For more information about the CQFP package options, refer to the* HiRel SX-A datasheet.
2. *All –3 speed grades have been discontinued.*

Device Resources

	User I/Os (Including Clock Buffers)							
Device	**208-Pin PQFP**	**100-Pin TQFP**	**144-Pin TQFP**	**176-Pin TQFP**	**329-Pin PBGA**	**144-Pin FBGA**	**256-Pin FBGA**	**484-Pin FBGA**
A54SX08A	130	81	113	–	–	111	–	–
A54SX16A	175	81	113	–	–	111	180	–
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	–	–	–	–	–	203	360

Notes: *Package Definitions: PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array*

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General Description

Detailed Specifications

Package Pin Assignments

Datasheet Information

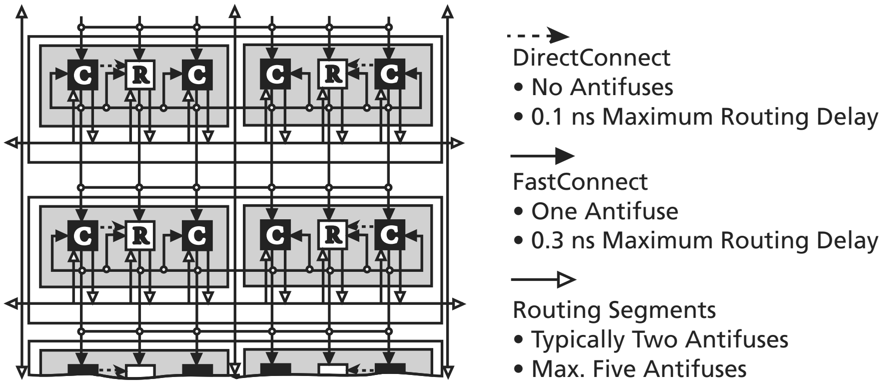

Figure 1-5 • **DirectConnect and FastConnect for Type 1 SuperClusters**

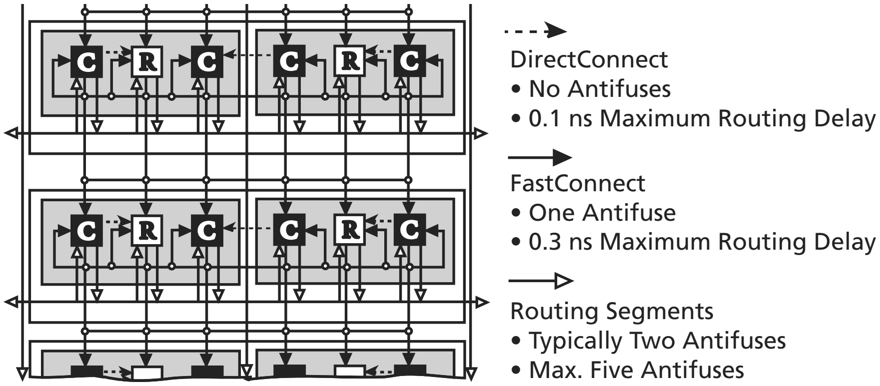

Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

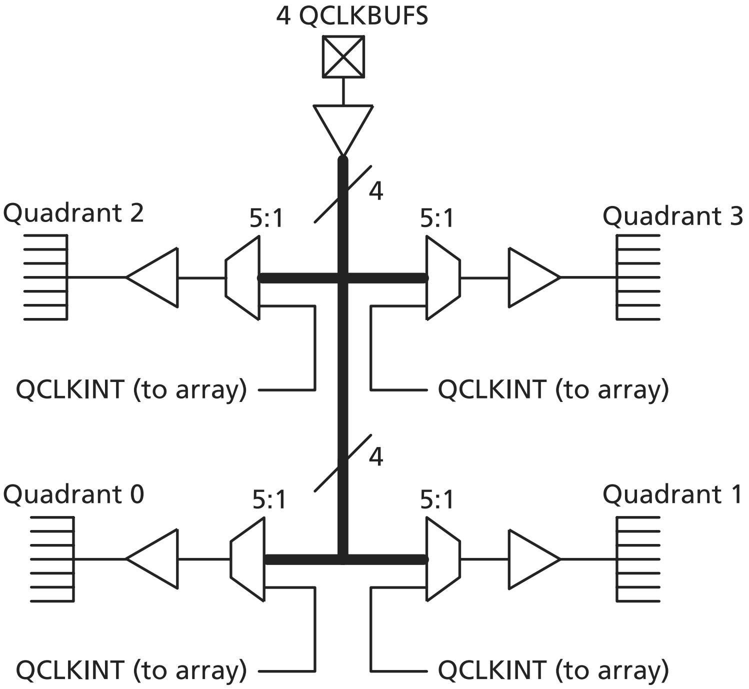

Figure 1-9 • **SX-A QCLK Architecture**

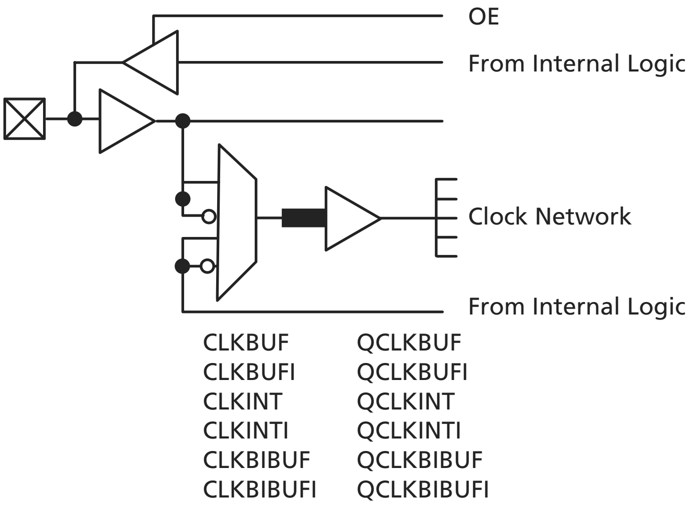

Figure 1-10 • **A54SX72A Routed Clock and QCLK Buffer**

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II diagnostic hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST High. If the TRST pin is held Low, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

When selecting the **Reserve Probe Pin** box as shown in Figure 1-12 on page 1-9, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This **Reserve** option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the **Reserve Probe Pin** option, Designer Layout will override the **Reserve Probe Pin** option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the JTAG and probe circuitry. Table 1-9 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Table 1-9 • **Device Configuration Options for Probe Capability (TRST Pin Reserved)**

JTAG Mode	**TRST[1]**	**Security Fuse Programmed**	**PRA, PRB[2]**	**TDI, TCK, TDO[2]**
Dedicated	Low	No	User I/O[3]	JTAG Disabled
	High	No	Probe Circuit Outputs	JTAG I/O
Flexible	Low	No	User I/O[3]	User I/O[3]
	High	No	Probe Circuit Outputs	JTAG I/O
		Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If the TRST pin is not reserved, the device behaves according to TRST = High as described in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

Pin Description

CLKA/B, I/O **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be tied Low or High (NOT left floating) on the board to avoid unwanted power consumption.

For A54SX72A, these pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only. When not used, these pins must be tied Low or High (NOT left floating).

QCLKA/B/C/D, I/O **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only used for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. When not used, these pins must be tied Low or High on the board (NOT left floating).

These pins can also be configured as user I/Os. When employed as user I/Os, these pins offer built-in programmable pull-up or pull-down resistors active during power-up only.

GND **Ground**

Low supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI, or 5 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When not used, HCLK must be tied Low or High on the board (NOT left floating). When used, this pin should be held Low or High during power-up to avoid unwanted static power consumption.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, LVCMOS2, 3.3 V PCI or 5 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC **No Connection**

This pin is not connected to circuitry within the device and can be driven to any voltage or be left floating with no effect on the operation of the device.

PRA/B, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In Flexible mode, TCK becomes active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In Flexible mode, TDI is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the “logic reset” state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (refer to Table 1-6 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the checksum command is run. It will return to user /IO when checksum is complete.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-6 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the logic reset state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The logic reset state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** is not selected in Designer.

V_{CCI} **Supply Voltage**

Supply voltage for I/Os. See Table 2-2 on page 2-1. All V_{CCI} power pins in the device should be connected.

V_{CCA} **Supply Voltage**

Supply voltage for array. See Table 2-2 on page 2-1. All V_{CCA} power pins in the device should be connected.

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules
Inputs Switching (n) = Number inputs/4
Outputs Switching (p) = Number of outputs/4
CLKA Loads (q1) = 20% of R-cells
CLKB Loads (q2) = 20% of R-cells
Load Capacitance (CL) = 35 pF
Average Logic Module Switching Rate (fm) = f/10
Average Input Switching Rate (fn) =f/5
Average Output Switching Rate (fp) = f/10
Average CLKA Rate (fq1) = f/2
Average CLKB Rate (fq2) = f/2
Average HCLK Rate (fs1) = f
HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

To determine the heat sink's thermal performance, use the following equation:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 2-14

where:

θ_{CS} = 0.37°C/W
= thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
θ_{SA} = thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 2-15

$$\theta_{SA} = 13.33°C/W - 3.20°C/W - 0.37°C/W$$

$$\theta_{SA} = 9.76°C/W$$

A heat sink with a thermal resistance of 9.76°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with the presence of airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device, using the provided thermal resistance data.

Note: The values may vary depending on the application.

Input Buffer Delays

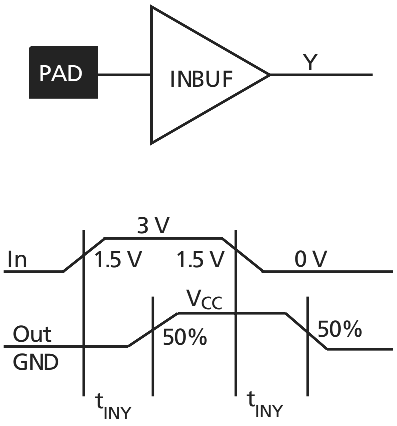

Figure 2-6 • **Input Buffer Delays**

C-Cell Delays

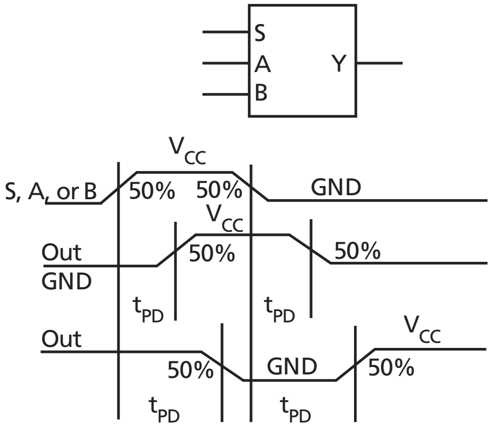

Figure 2-7 • **C-Cell Delays**

Cell Timing Characteristics

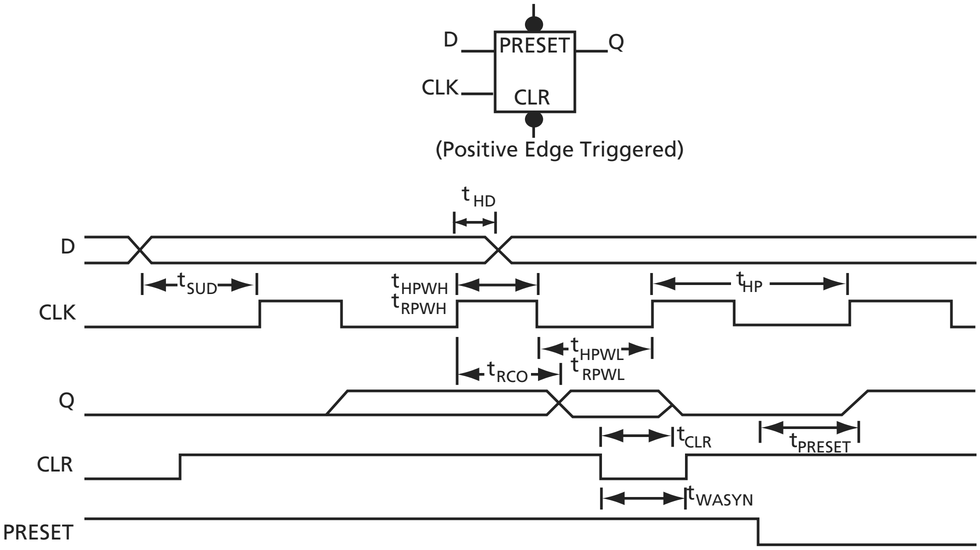

Figure 2-8 • **Flip-Flops**

Table 2-15 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.4		1.6		1.8		2.6	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.7	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.0		1.1		1.3		1.8	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.2		1.4		2.0	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.4	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.7		0.8		0.9		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-20 • **A54SX08A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

		–2 Speed		–1 Speed		Std. Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5 V PCI Output Module Timing[1]										
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.6		4.2		5.9	ns
d_{TLH}[2]	Delta Low to High		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[2]	Delta High to Low		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.2		4.5	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.6		4.2		5.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		7.6		8.6		10.1		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.2		4.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.6		4.2		5.9	ns
d_{TLH}	Delta Low to High		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta High to Low		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta High to Low—low slew		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1 * V_{CCI} – 0.9 * V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
3. *Delays based on 35 pF loading.*

Table 2-27 • **A54SX16A Timing Characteristics**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.5		2.8		3.3		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.6		4.2		5.9	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.2		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad High to Low		2.8		3.2		3.6		4.2		5.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		6.7		7.7		8.7		10.2		14.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.9		2.2		2.5		2.9		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.3		3.9		5.4	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1 \cdot V_{CCI} - 0.9 \cdot V_{CCI}) / (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-38 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)

		–3 Speed*		**–2 Speed**		**–1 Speed**		**Std. Speed**		**–F Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: **All –3 speed grades have been discontinued.*

176-Pin TQFP	
Pin Number	**A54SX32A Function**
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	TMS
11	V_{CCI}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	V_{CCA}
23	GND
24	I/O
25	TRST, I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	V_{CCI}
33	V_{CCA}
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	GND
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	V_{CCI}
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	PRB, I/O
65	GND
66	V_{CCA}
67	NC
68	I/O
69	HCLK
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V_{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	TDO, I/O
88	I/O
89	GND
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V_{CCA}
99	V_{CCI}
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	GND
109	V_{CCA}
110	GND
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	V_{CCA}
123	GND
124	V_{CCI}
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	GND
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	V_{CCI}
141	I/O
142	I/O
143	I/O
144	I/O

329-Pin PBGA	
Pin Number	**A54SX32A Function**
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V_{CCI}	V_{CCI}	V_{CCI}
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	V_{CCI}	V_{CCI}	V_{CCI}
F10	V_{CCI}	V_{CCI}	V_{CCI}
F11	I/O	I/O	I/O
F12	VCCA	VCCA	VCCA
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V_{CCI}	V_{CCI}	V_{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V_{CCI}	V_{CCI}	V_{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V_{CCA}	V_{CCA}	V_{CCA}

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V_{CCA}	V_{CCA}	V_{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V_{CCI}	V_{CCI}	V_{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V_{CCI}	V_{CCI}	V_{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V_{CCI}	V_{CCI}	V_{CCI}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V_{CCI}	V_{CCI}	V_{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V_{CCA}	V_{CCA}	V_{CCA}

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC*	NC
K25	NC*	I/O
K26	NC*	I/O
L1	NC*	I/O
L2	NC*	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC*	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC*	I/O
M26	NC*	I/O
N1	I/O	I/O
N2	V_{CCI}	V_{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V_{CCA}	V_{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC*	NC
P1	NC*	I/O
P2	NC*	I/O
P3	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
P4	I/O	I/O
P5	V_{CCA}	V_{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V_{CCI}	V_{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC*	I/O
R2	NC*	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O
R23	I/O	I/O
R24	I/O	I/O
R25	NC*	I/O
R26	NC*	I/O
T1	NC*	I/O
T2	NC*	I/O

Note: **These pins must be left floating on the A54SX32A device.*

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9

Previous Version	Changes in Current Version (v5.3)	Page
v4.0 (continued)	Table 2-12 was updated.	2-11
	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The “"Clock Resources" section“was updated	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23

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