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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	147
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a54sx32a-1tqg176m">https://www.e-xfl.com/product-detail/microsemi/a54sx32a-1tqg176m</a>

# General Description

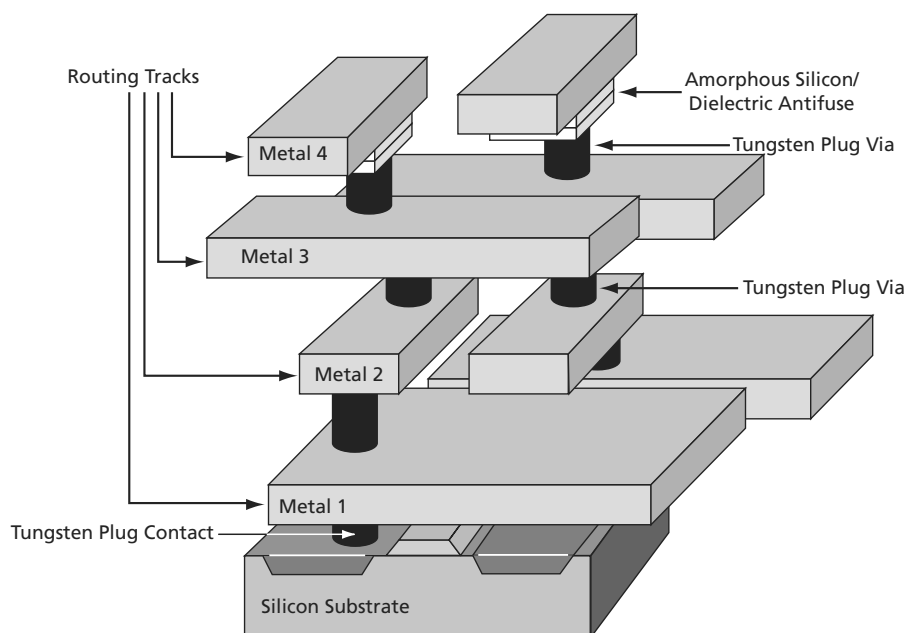
## Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22  $\mu\text{m}$  / 0.25  $\mu\text{m}$  CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

## SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



**Note:** The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.

Figure 1-1 • SX-A Family Interconnect Elements

## Logic Module Design

The SX-A family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX-A family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable, using the S0 and S1 lines control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3). Inclusion of the DB input and its associated inverter function allows up to 4,000

different combinatorial functions to be implemented in a single module. An example of the flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays.

## Module Organization

All C-cell and R-cell logic modules are arranged into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are grouped together into SuperClusters (Figure 1-4 on page 1-3). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

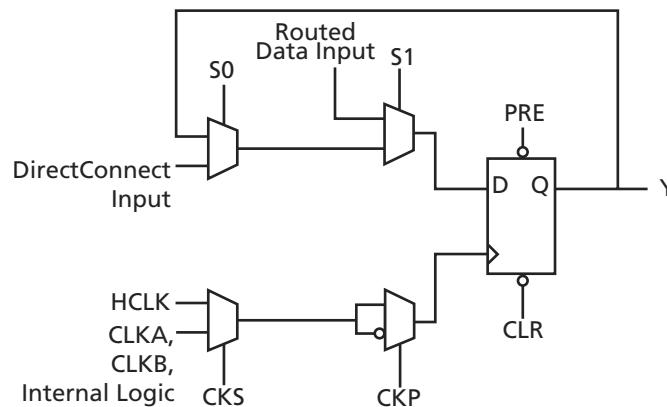


Figure 1-2 • R-Cell

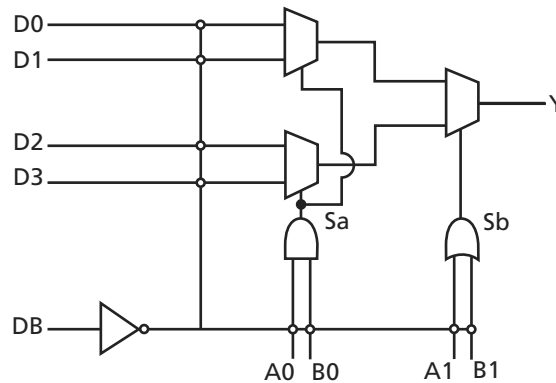


Figure 1-3 • C-Cell

## Routing Resources

The routing and interconnect resources of SX-A devices are in the top two metal layers above the logic modules (Figure 1-1 on page 1-1), providing optimal use of silicon, thus enabling the entire floor of the device to be spanned with an uninterrupted grid of logic modules. Interconnection between these logic modules is achieved using the Actel patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuits and, when programmed, form a permanent low-impedance connection.

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance, which is often required in applications such as fast counters, state machines, and data path logic. The interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-Cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable

interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

The general system of routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, most connections typically require three or fewer antifuses, resulting in fast and predictable performance.

The unique local and general routing structure featured in SX-A devices allows 100% pin-locking with full logic utilization, enables concurrent printed circuit board (PCB) development, reduces design time, and allows designers to achieve performance goals with minimum effort.

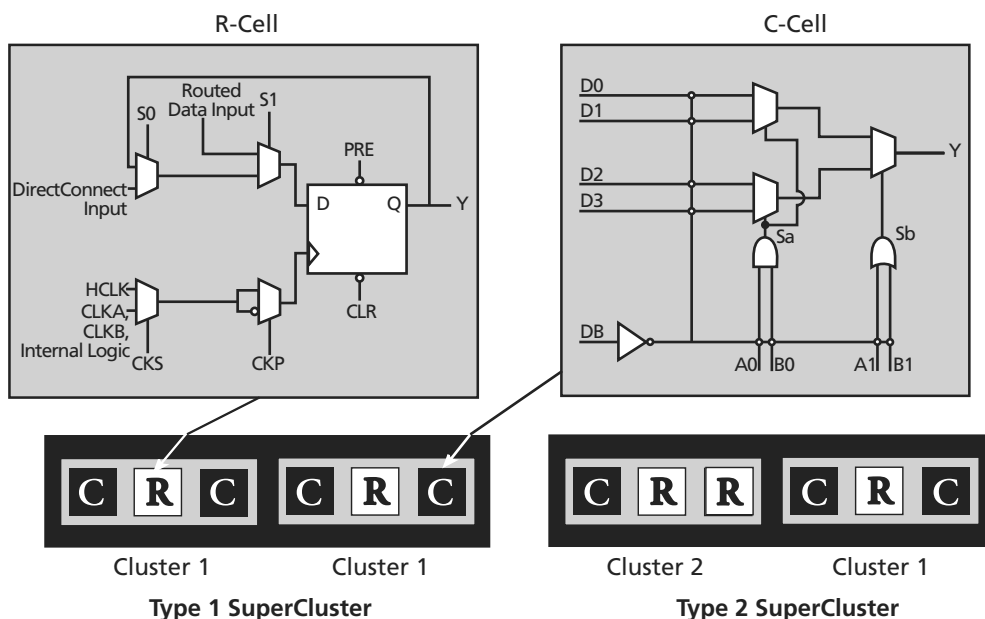


Figure 1-4 • Cluster Organization

## Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant load HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA

and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an entire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices and Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15.

Table 1-1 • **SX-A Clock Resources**

	<b>A54SX08A</b>	<b>A54SX16A</b>	<b>A54SX32A</b>	<b>A54SX72A</b>
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

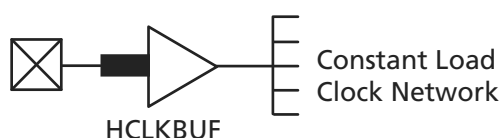


Figure 1-7 • **SX-A HCLK Clock Buffer**

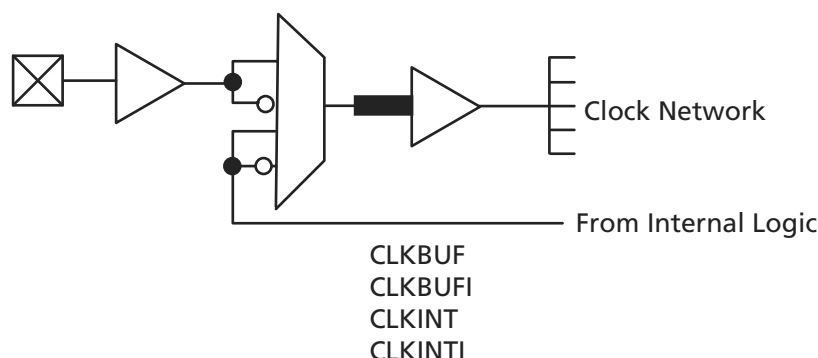


Figure 1-8 • **SX-A Routed Clock Buffer**

## SX-A Probe Circuit Control Pins

SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use, integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the

PRA/PRB pins for observation. Figure 1-13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

In order to preserve device probing capabilities, users should avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, the security fuse must not be programmed to preserve probing capabilities. Actel recommends that you use a 70  $\Omega$  series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70  $\Omega$  series termination is used to prevent data transmission corruption during probing and reading back the checksum.

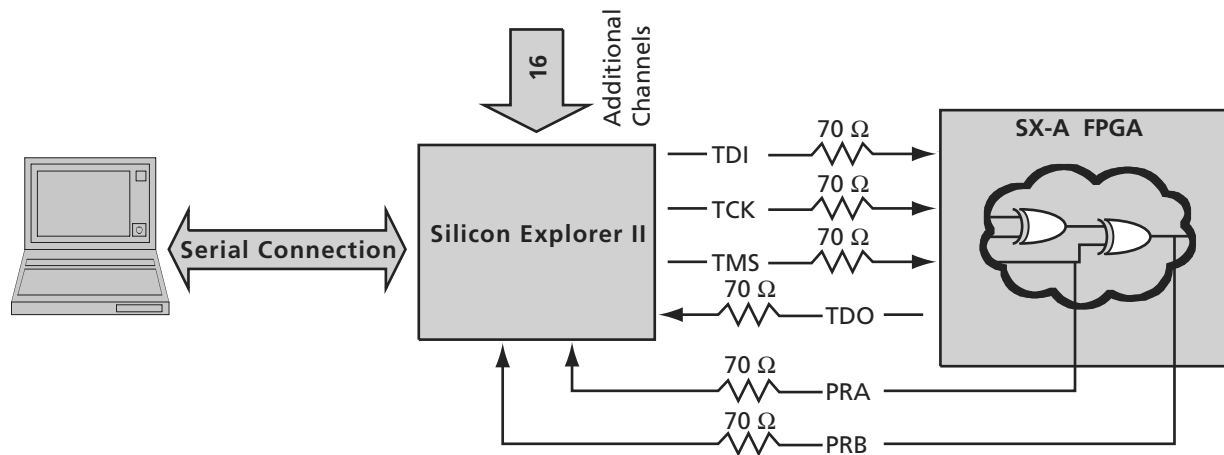


Figure 1-13 • Probe Setup

# Detailed Specifications

## Operating Conditions

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
$V_{CCI}$	DC Supply Voltage for I/Os	−0.3 to +6.0	V
$V_{CCA}$	DC Supply Voltage for Arrays	−0.3 to +3.0	V
$V_I$	Input Voltage	−0.5 to +5.75	V
$V_O$	Output Voltage	−0.5 to + $V_{CCI}$ + 0.5	V
$T_{STG}$	Storage Temperature	−65 to +150	°C

**Note:** \*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".

Table 2-2 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	−40 to +85	°C
2.5 V Power Supply Range ( $V_{CCA}$ and $V_{CCI}$ )	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range ( $V_{CCI}$ )	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range ( $V_{CCI}$ )	4.75 to 5.25	4.75 to 5.25	V

## Typical SX-A Standby Current

Table 2-3 • Typical Standby Current for SX-A at 25°C with  $V_{CCA} = 2.5$  V

Product	$V_{CCI} = 2.5$ V	$V_{CCI} = 3.3$ V	$V_{CCI} = 5$ V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • Supply Voltages

$V_{CCA}$	$V_{CCI}^*$	Maximum Input Tolerance	Maximum Output Drive
2.5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

**Note:** \*3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.

## Electrical Specifications

Table 2-5 • 3.3 V LVTTTL and 5 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = −1 mA)	0.9 V <sub>CCI</sub>		0.9 V <sub>CCI</sub>		V
	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = −8 mA)	2.4		2.4		V
V <sub>OL</sub>	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 1 mA)	0.4		0.4		V
	V <sub>CCI</sub> = Minimum V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 12 mA)	0.4		0.4		V
V <sub>IL</sub>	Input Low Voltage		0.8		0.8		V
V <sub>IH</sub>	Input High Voltage		2.0	5.75	2.0	5.75	V
I <sub>IL</sub> /I <sub>IH</sub>	Input Leakage Current, V <sub>IN</sub> = V <sub>CCI</sub> or GND		−10	10	−10	10	μA
I <sub>OZ</sub>	Tristate Output Leakage Current		−10	10	−10	10	μA
t <sub>R</sub> , t <sub>F</sub>	Input Transition Time t <sub>R</sub> , t <sub>F</sub>		10		10		ns
C <sub>IO</sub>	I/O Capacitance		10		10		pF
I <sub>CC</sub>	Standby Current		10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.						

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.

Table 2-6 • 2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -100 μA)	2.1		2.1		V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -1 mA)	2.0		2.0		V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OH</sub> = -2 mA)	1.7		1.7		V
V <sub>OL</sub>	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 100 μA)		0.2		0.2	V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 1 mA)		0.4		0.4	V
	V <sub>DD</sub> = MIN, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	(I <sub>OL</sub> = 2 mA)		0.7		0.7	V
V <sub>IL</sub>	Input Low Voltage, V <sub>OUT</sub> ≤ V <sub>VOL(max)</sub>		-0.3	0.7	-0.3	0.7	V
V <sub>IH</sub>	Input High Voltage, V <sub>OUT</sub> ≥ V <sub>VOH(min)</sub>		1.7	5.75	1.7	5.75	V
I <sub>IL</sub> /I <sub>IH</sub>	Input Leakage Current, V <sub>IN</sub> = V <sub>CCI</sub> or GND		-10	10	-10	10	μA
I <sub>OZ</sub>	Tristate Output Leakage Current, V <sub>OUT</sub> = V <sub>CCI</sub> or GND		-10	10	-10	10	μA
t <sub>R</sub> , t <sub>F</sub>	Input Transition Time t <sub>R</sub> , t <sub>F</sub>			10		10	ns
C <sub>IO</sub>	I/O Capacitance			10		10	pF
I <sub>CC</sub>	Standby Current			10		20	mA
IV Curve*	Can be derived from the IBIS model on the web.						

**Note:** \*The IBIS model can be found at <http://www.actel.com/download/libis/default.aspx>.



## Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

$$\theta_{JA} = 17.1^{\circ}\text{C/W} \text{ is taken from Table 2-12 on page 2-11}$$

$$T_A = 125^{\circ}\text{C} \text{ is the maximum limit of ambient (from the datasheet)}$$

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{17.1^{\circ}\text{C/W}} = 1.46 \text{ W}$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

## Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

## Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data  $T_J$  and  $T_A$  are given as follows:

$$T_J = 110^{\circ}\text{C}$$

$$T_A = 70^{\circ}\text{C}$$

From the datasheet:

$$\theta_{JA} = 18.0^{\circ}\text{C/W}$$

$$\theta_{JC} = 3.2^{\circ}\text{C/W}$$

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{18.0^{\circ}\text{C/W}} = 2.22 \text{ W}$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{3.00 \text{ W}} = 13.33^{\circ}\text{C/W}$$

EQ 2-13

Table 2-15 • **A54SX08A Timing Characteristics**  
(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 2.25\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )

Parameter	Description	-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)	1.4		1.6		1.8		2.6		ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)	1.3		1.5		1.7		2.4		ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t <sub>HCKSW</sub>	Maximum Skew	0.4		0.4		0.5		0.7		ns
t <sub>HP</sub>	Minimum Period	3.2		3.6		4.2		5.8		ns
f <sub>HMAX</sub>	Maximum Frequency	313		278		238		172		MHz
Routed Array Clock Networks										
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)	1.0		1.1		1.3		1.8		ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)	1.0		1.1		1.3		1.8		ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)	1.1		1.2		1.4		2.0		ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)	1.3		1.5		1.7		2.4		ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)	0.7		0.8		0.9		1.3		ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)	0.7		0.8		0.9		1.3		ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)	0.9		1.0		1.2		1.7		ns

**Table 2-28 • A54SX32A Timing Characteristics**
**(Worst-Case Commercial Conditions,  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 3.0\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	-3 Speed <sup>1</sup>		-2 Speed		-1 Speed		Std. Speed		-F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays <sup>2</sup>												
t <sub>PD</sub>	Internal Array Module	0.8		0.9		1.1		1.2		1.7		ns
Predicted Routing Delays <sup>3</sup>												
t <sub>DC</sub>	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t <sub>FC</sub>	FO = 1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t <sub>RD1</sub>	FO = 1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t <sub>RD2</sub>	FO = 2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t <sub>RD3</sub>	FO = 3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t <sub>RD4</sub>	FO = 4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t <sub>RD8</sub>	FO = 8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RD12</sub>	FO = 12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t <sub>RCO</sub>	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.5		0.6		0.6		0.8		1.0		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.6		0.7		0.7		0.9		1.2		ns
t <sub>SUD</sub>	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		0.9		1.2		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.2		1.4		1.5		1.8		2.5		ns
t <sub>RECASYN</sub>	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t <sub>HASYN</sub>	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
t <sub>MPW</sub>	Clock Pulse Width	1.4		1.6		1.8		2.1		2.9		ns
Input Module Propagation Delays												
t <sub>INYH</sub>	Input Data Pad to Y High 2.5 V LVCMOS	0.6		0.7		0.8		0.9		1.2		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 2.5 V LVCMOS	1.2		1.3		1.5		1.8		2.5		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V PCI	0.5		0.6		0.6		0.7		1.0		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V PCI	0.6		0.7		0.8		0.9		1.3		ns
t <sub>INYH</sub>	Input Data Pad to Y High 3.3 V LVTTTL	0.8		0.9		1.0		1.2		1.6		ns
t <sub>INYL</sub>	Input Data Pad to Y Low 3.3 V LVTTTL	1.4		1.6		1.8		2.2		3.0		ns

**Notes:**

1. All -3 speed grades have been discontinued.
2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{RCO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
3. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

Table 2-31 • **A54SX32A Timing Characteristics**  
**(Worst-Case Commercial Conditions  $V_{CCA} = 2.25\text{ V}$ ,  $V_{CCI} = 4.75\text{ V}$ ,  $T_J = 70^\circ\text{C}$ )**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t <sub>HCKH</sub>	Input Low to High (Pad to R-cell Input)		1.7		1.9		2.2		2.6		4.0	ns
t <sub>HCKL</sub>	Input High to Low (Pad to R-cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>HCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		1.3	ns
t <sub>HP</sub>	Minimum Period	2.8		3.2		3.6		4.2		5.8		ns
f <sub>HMAX</sub>	Maximum Frequency		357		313		278		238		172	MHz
Routed Array Clock Networks												
t <sub>RCKH</sub>	Input Low to High (Light Load) (Pad to R-cell Input)		2.2		2.5		2.8		3.3		4.7	ns
t <sub>RCKL</sub>	Input High to Low (Light Load) (Pad to R-cell Input)		2.1		2.5		2.8		3.3		4.5	ns
t <sub>RCKH</sub>	Input Low to High (50% Load) (Pad to R-cell Input)		2.4		2.7		3.1		3.6		5.1	ns
t <sub>RCKL</sub>	Input High to Low (50% Load) (Pad to R-cell Input)		2.2		2.6		2.9		3.4		4.7	ns
t <sub>RCKH</sub>	Input Low to High (100% Load) (Pad to R-cell Input)		2.5		2.8		3.2		3.8		5.3	ns
t <sub>RCKL</sub>	Input High to Low (100% Load) (Pad to R-cell Input)		2.4		2.8		3.1		3.7		5.2	ns
t <sub>RPWH</sub>	Minimum Pulse Width High	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RPWL</sub>	Minimum Pulse Width Low	1.4		1.6		1.8		2.1		2.9		ns
t <sub>RCKSW</sub>	Maximum Skew (Light Load)		1.0		1.1		1.3		1.5		2.1	ns
t <sub>RCKSW</sub>	Maximum Skew (50% Load)		1.0		1.1		1.3		1.5		2.1	ns
t <sub>RCKSW</sub>	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

**Note:** \*All –3 speed grades have been discontinued.

## 100-Pin TQFP

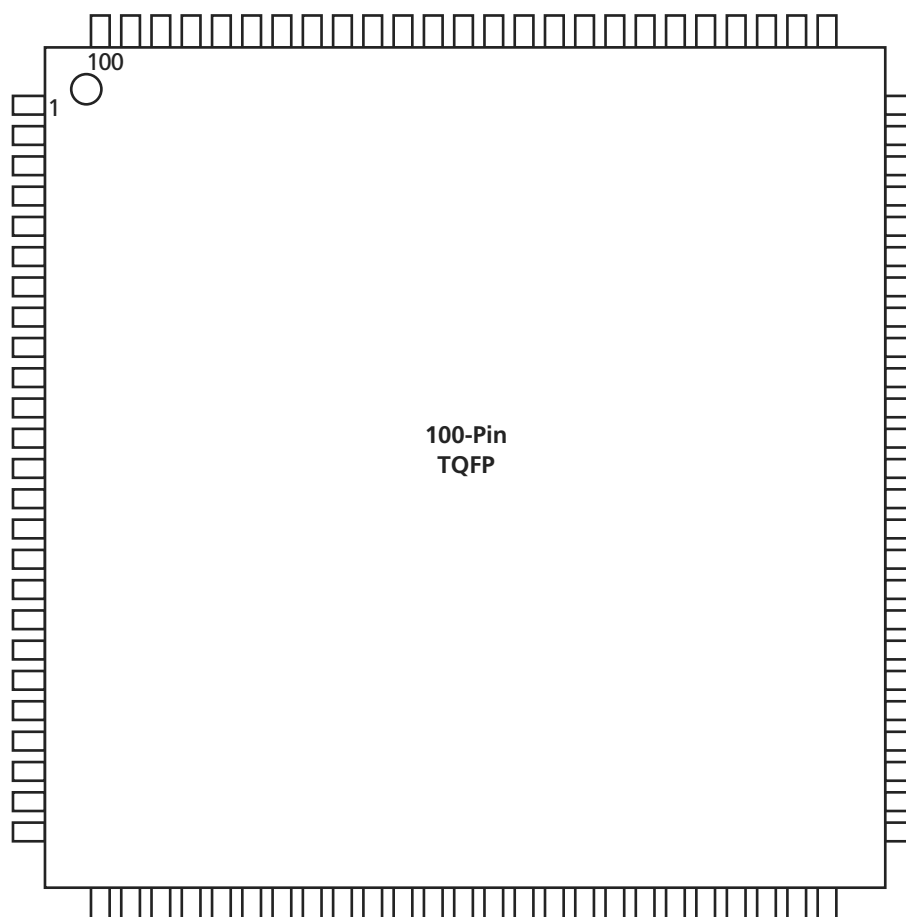


Figure 3-2 • 100-Pin TQFP

### Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
30	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V <sub>CCA</sub>	V <sub>CCA</sub>	V <sub>CCA</sub>
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V <sub>CCI</sub>	V <sub>CCI</sub>	V <sub>CCI</sub>
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
A1	GND	AA15	I/O	AC6	I/O	B20	I/O
A2	GND	AA16	I/O	AC7	I/O	B21	I/O
A3	V <sub>CCI</sub>	AA17	I/O	AC8	I/O	B22	GND
A4	NC	AA18	I/O	AC9	V <sub>CCI</sub>	B23	V <sub>CCI</sub>
A5	I/O	AA19	I/O	AC10	I/O	C1	NC
A6	I/O	AA20	TDO, I/O	AC11	I/O	C2	TDI, I/O
A7	V <sub>CCI</sub>	AA21	V <sub>CCI</sub>	AC12	I/O	C3	GND
A8	NC	AA22	I/O	AC13	I/O	C4	I/O
A9	I/O	AA23	V <sub>CCI</sub>	AC14	I/O	C5	I/O
A10	I/O	AB1	I/O	AC15	NC	C6	I/O
A11	I/O	AB2	GND	AC16	I/O	C7	I/O
A12	I/O	AB3	I/O	AC17	I/O	C8	I/O
A13	CLKB	AB4	I/O	AC18	I/O	C9	I/O
A14	I/O	AB5	I/O	AC19	I/O	C10	I/O
A15	I/O	AB6	I/O	AC20	I/O	C11	I/O
A16	I/O	AB7	I/O	AC21	NC	C12	I/O
A17	I/O	AB8	I/O	AC22	V <sub>CCI</sub>	C13	I/O
A18	I/O	AB9	I/O	AC23	GND	C14	I/O
A19	I/O	AB10	I/O	B1	V <sub>CCI</sub>	C15	I/O
A20	I/O	AB11	PRB, I/O	B2	GND	C16	I/O
A21	NC	AB12	I/O	B3	I/O	C17	I/O
A22	V <sub>CCI</sub>	AB13	HCLK	B4	I/O	C18	I/O
A23	GND	AB14	I/O	B5	I/O	C19	I/O
AA1	V <sub>CCI</sub>	AB15	I/O	B6	I/O	C20	I/O
AA2	I/O	AB16	I/O	B7	I/O	C21	V <sub>CCI</sub>
AA3	GND	AB17	I/O	B8	I/O	C22	GND
AA4	I/O	AB18	I/O	B9	I/O	C23	NC
AA5	I/O	AB19	I/O	B10	I/O	D1	I/O
AA6	I/O	AB20	I/O	B11	I/O	D2	I/O
AA7	I/O	AB21	I/O	B12	PRA, I/O	D3	I/O
AA8	I/O	AB22	GND	B13	CLKA	D4	TCK, I/O
AA9	I/O	AB23	I/O	B14	I/O	D5	I/O
AA10	I/O	AC1	GND	B15	I/O	D6	I/O
AA11	I/O	AC2	V <sub>CCI</sub>	B16	I/O	D7	I/O
AA12	I/O	AC3	NC	B17	I/O	D8	I/O
AA13	I/O	AC4	I/O	B18	I/O	D9	I/O
AA14	I/O	AC5	I/O	B19	I/O	D10	I/O



329-Pin PBGA	
Pin Number	A545X32A Function
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V <sub>CCA</sub>
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC
A2	NC*	NC
A3	NC*	I/O
A4	NC*	I/O
A5	NC*	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC*	I/O
A12	NC*	I/O
A13	I/O	I/O
A14	NC*	NC
A15	NC*	I/O
A16	NC*	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC*	I/O
A22	NC*	I/O
A23	NC*	I/O
A24	NC*	I/O
A25	NC*	NC
A26	NC*	NC
AA1	NC*	I/O
AA2	NC*	I/O
AA3	V <sub>CCA</sub>	V <sub>CCA</sub>
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AA26	NC*	I/O
AB1	NC*	NC
AB2	V <sub>CCI</sub>	V <sub>CCI</sub>
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC*	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V <sub>CCA</sub>	V <sub>CCA</sub>
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC*	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC*	I/O
AB26	NC*	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC*	I/O
AC5	V <sub>CCI</sub>	V <sub>CCI</sub>
AC6	I/O	I/O
AC7	V <sub>CCI</sub>	V <sub>CCI</sub>
AC8	I/O	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V <sub>CCI</sub>	V <sub>CCI</sub>
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC*	I/O
AC24	I/O	I/O
AC25	NC*	I/O
AC26	NC*	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V <sub>CCI</sub>	V <sub>CCI</sub>
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V <sub>CCI</sub>	V <sub>CCI</sub>
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V <sub>CCI</sub>	V <sub>CCI</sub>

**Note:** \*These pins must be left floating on the A54SX32A device.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC *	I/O
T26	NC *	I/O
U1	I/O	I/O
U2	V <sub>CCI</sub>	V <sub>CCI</sub>
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V <sub>CCI</sub>	V <sub>CCI</sub>
U26	I/O	I/O
V1	NC *	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
V2	NC *	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V <sub>CCA</sub>	V <sub>CCA</sub>
V23	I/O	I/O
V24	I/O	I/O
V25	NC *	I/O
V26	NC *	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V <sub>CCA</sub>	V <sub>CCA</sub>
W24	I/O	I/O
W25	NC *	I/O
W26	NC *	I/O
Y1	NC *	I/O
Y2	NC *	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC *	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V <sub>CCI</sub>	V <sub>CCI</sub>
Y25	I/O	I/O
Y26	I/O	I/O

**Note:** \*These pins must be left floating on the A54SX32A device.

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9

Previous Version	Changes in Current Version (v5.3)	Page
v4.0 (continued)	Table 2-12 was updated.	2-11
	The was updated.	2-14
	The "Sample Path Calculations" were updated.	2-14
	Table 2-13 was updated.	2-17
	Table 2-13 was updated.	2-17
	All timing tables were updated.	2-18 to 2-52
v3.0	The "Actel Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft" section was updated.	1-i
	The "Ordering Information" section was updated.	1-ii
	The "Temperature Grade Offering" section was updated.	1-iii
	The Figure 1-1 • SX-A Family Interconnect Elements was updated.	1-1
	The "Clock Resources" section was updated.	1-5
	The Table 1-1 • SX-A Clock Resources is new.	1-5
	The "User Security" section is new.	1-7
	The "I/O Modules" section was updated.	1-7
	The Table 1-2 • I/O Features was updated.	1-8
	The Table 1-3 • I/O Characteristics for All I/O Configurations is new.	1-8
	The Table 1-4 • Power-Up Time at which I/Os Become Active is new.	1-8
	The Figure 1-12 • Device Selection Wizard is new.	1-9
	The "Boundary-Scan Pin Configurations and Functions" section is new.	1-9
	The Table 1-9 • Device Configuration Options for Probe Capability (TRST Pin Reserved) is new.	1-11
	The "SX-A Probe Circuit Control Pins" section was updated.	1-12
	The "Design Considerations" section was updated.	1-12
	The Figure 1-13 • Probe Setup was updated.	1-12
	The Design Environment was updated.	1-13
	The Figure 1-13 • Design Flow is new.	1-11
	The "Absolute Maximum Ratings*" section was updated.	1-12
	The "Recommended Operating Conditions" section was updated.	1-12
	The "Electrical Specifications" section was updated.	1-12
	The "2.5V LVCMOS2 Electrical Specifications" section was updated.	1-13
	The "SX-A Timing Model" and "Sample Path Calculations" equations were updated.	1-23
	The "Pin Description" section was updated.	1-15
v2.0.1	The "Design Environment" section has been updated.	1-13
	The "I/O Modules" section, and Table 1-2 • I/O Features have been updated.	1-8
	The "SX-A Timing Model" section and the "Timing Characteristics" section have new timing numbers.	1-23