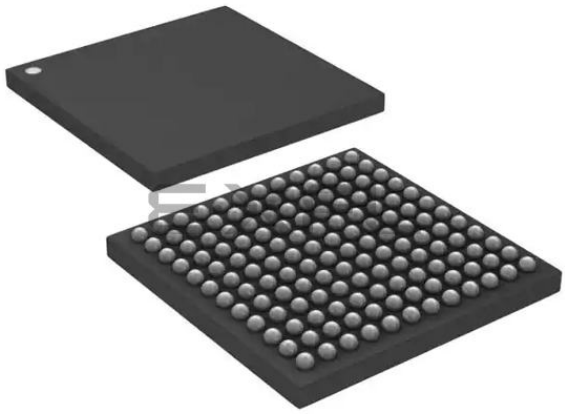


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx32a-2fg144

General Description

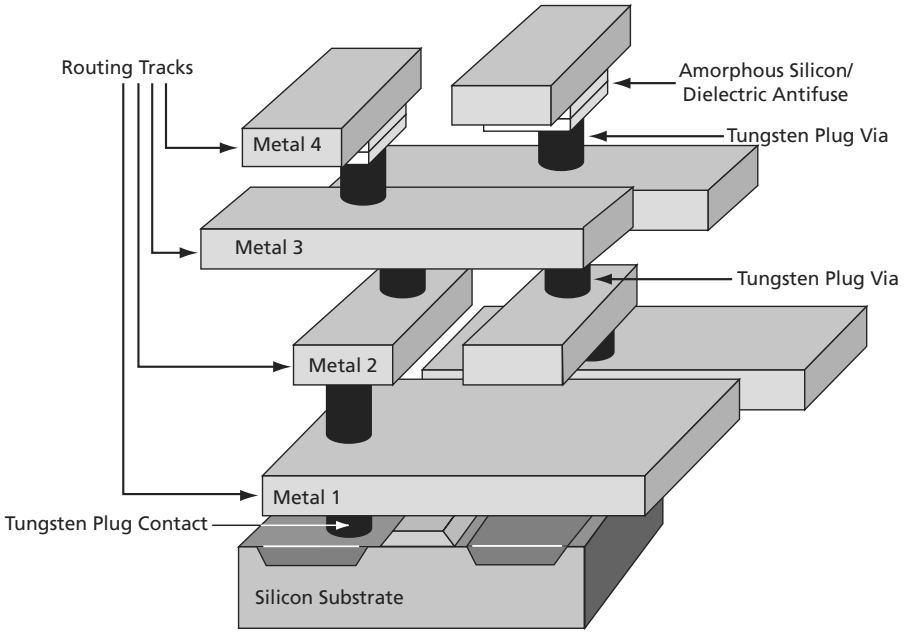
Introduction

The Actel SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. Fabricated on 0.22 µm / 0.25 µm CMOS antifuse technology and with the support of 2.5 V, 3.3 V and 5 V I/Os, the SX-A is a versatile platform to integrate designs while significantly reducing time-to-market.

SX-A Family Architecture

The SX-A family's device architecture provides a unique approach to module organization and chip routing that satisfies performance requirements and delivers the most optimal register/logic mix for a wide variety of applications.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements (Figure 1-1). The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.



Note: *The A54SX72A device has four layers of metal with the antifuse between Metal 3 and Metal 4. The A54SX08A, A54SX16A, and A54SX32A devices have three layers of metal with the antifuse between Metal 2 and Metal 3.*

Figure 1-1 • **SX-A Family Interconnect Elements**

Detailed Specifications

Operating Conditions

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage for I/Os	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage for Arrays	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.75	V
V_O	Output Voltage	–0.5 to + V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions".*

Table 2-2 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range	0 to +70	–40 to +85	°C
2.5 V Power Supply Range (V_{CCA} and V_{CCI})	2.25 to 2.75	2.25 to 2.75	V
3.3 V Power Supply Range (V_{CCI})	3.0 to 3.6	3.0 to 3.6	V
5 V Power Supply Range (V_{CCI})	4.75 to 5.25	4.75 to 5.25	V

Typical SX-A Standby Current

Table 2-3 • **Typical Standby Current for SX-A at 25°C with V_{CCA} = 2.5 V**

Product	V_{CCI} = 2.5 V	V_{CCI} = 3.3 V	V_{CCI} = 5 V
A54SX08A	0.8 mA	1.0 mA	2.9 mA
A54SX16A	0.8 mA	1.0 mA	2.9 mA
A54SX32A	0.9 mA	1.0 mA	3.0 mA
A54SX72A	3.6 mA	3.8 mA	4.5 mA

Table 2-4 • **Supply Voltages**

V_{CCA}	V_{CCI}*	Maximum Input Tolerance	Maximum Output Drive
2. 5 V	2.5 V	5.75 V	2.7 V
2.5 V	3.3 V	5.75 V	3.6 V
2.5 V	5 V	5.75 V	5.25 V

Note: **3.3 V PCI is not 5 V tolerant due to the clamp diode, but instead is 3.3 V tolerant.*

Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules

Inputs Switching (n) = Number inputs/4

Outputs Switching (p) = Number of outputs/4

CLKA Loads (q1) = 20% of R-cells

CLKB Loads (q2) = 20% of R-cells

Load Capacitance (CL) = 35 pF

Average Logic Module Switching Rate (fm) = f/10

Average Input Switching Rate (fn) =f/5

Average Output Switching Rate (fp) = f/10

Average CLKA Rate (fq1) = f/2

Average CLKB Rate (fq2) = f/2

Average HCLK Rate (fs1) = f

HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JESD-51 series but has little relevance in actual performance of the product in real application. It should be employed with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation to estimate the absolute maximum power dissipation allowed (worst case) for a 329-pin PBGA package at still air is as follows. i.e.:

θ_{JA} = 17.1°C/W is taken from Table 2-12 on page 2-11

T_A = 125°C is the maximum limit of ambient (from the datasheet)

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{150°C - 125°C}{17.1°C/W} = 1.46\ W$$

EQ 2-11

The device's power consumption must be lower than the calculated maximum power dissipation by the package.

The power consumption of a device can be calculated using the Actel power calculator. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration. If the power consumption is higher than the calculated maximum power dissipation of the package, then a heat sink is required.

Calculation for Heat Sink

For example, in a design implemented in a FG484 package, the power consumption value using the power calculator is 3.00 W. The user-dependent data T_J and T_A are given as follows:

T_J = 110°C

T_A = 70°C

From the datasheet:

θ_{JA} = 18.0°C/W

θ_{JC} = 3.2 °C/W

$$P = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{JA}} = \frac{110°C - 70°C}{18.0°C/W} = 2.22\ W$$

EQ 2-12

The 2.22 W power is less than then required 3.00 W; therefore, the design requires a heat sink or the airflow where the device is mounted should be increased. The design's junction-to-air thermal resistance requirement can be estimated by:

$$\theta_{JA} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{P} = \frac{110°C - 70°C}{3.00\ W} = 13.33°C/W$$

EQ 2-13

Table 2-17 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks										
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.3		1.5		2.3	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.2		1.4		2.0	ns
t_{HPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{HCKSW}	Maximum Skew		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	3.2		3.6		4.2		5.8		ns
f_{HMAX}	Maximum Frequency		313		278		238		172	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		0.9		1.0		1.2		1.7	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.5		1.7		2.0		2.7	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.1		1.3		1.5		2.1	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.6		1.8		2.1		2.9	ns
t_{RPWH}	Minimum Pulse Width High	1.6		1.8		2.1		2.9		ns
t_{RPWL}	Minimum Pulse Width Low	1.6		1.8		2.1		2.9		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		1.0		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9		1.0		1.2		1.7	ns

Table 2-19 • **A54SX08A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[1]										
t_{DLH}	Data-to-Pad Low to High		2.2		2.4		2.9		4.0	ns
t_{DHL}	Data-to-Pad High to Low		2.3		2.6		3.1		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.4		2.9		4.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.3		2.6		3.1		4.3	ns
d_{TLH}[2]	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[2]	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[3]										
t_{DLH}	Data-to-Pad Low to High		3.0		3.4		4.0		5.6	ns
t_{DHL}	Data-to-Pad High to Low		3.0		3.3		3.9		5.5	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		10.4		11.8		13.8		19.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3		3.4		4		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3		3.3		3.9		5.5	ns
d_{TLH}[2]	Delta Low to High		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[2]	Delta High to Low		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[2]	Delta High to Low—low slew		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25 Ω resistance.*
2. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
3. *Delays based on 35 pF loading.*

Table 2-22 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.2		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.7	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-23 • **A54SX16A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input Low to High (Pad to R-cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input High to Low (Pad to R-cell Input)		1.0		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.4		0.4		0.6	ns
t_{HP}	Minimum Period	2.8		3.4		3.8		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		357		294		263		227		167	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (Light Load) (Pad to R-cell Input)		1.0		1.2		1.3		1.5		2.1	ns
t_{RCKL}	Input High to Low (Light Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (50% Load) (Pad to R-cell Input)		1.1		1.3		1.4		1.7		2.3	ns
t_{RCKL}	Input High to Low (50% Load) (Pad to R-cell Input)		1.1		1.3		1.5		1.7		2.4	ns
t_{RCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.7	ns
t_{RCKL}	Input High to Low (100% Load) (Pad to R-cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RPWH}	Minimum Pulse Width High	1.4		1.7		1.9		2.2		3.0		ns
t_{RPWL}	Minimum Pulse Width Low	1.4		1.7		1.9		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9		1.0		1.2		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.0		1.1		1.3		1.5		2.1	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-35 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INYH}	Input Data Pad to Y High 5 V PCI		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad to Y Low 5 V PCI		0.8		0.9		1.0		1.2		1.6	ns
t_{INYH}	Input Data Pad to Y High 5 V TTL		0.7		0.8		0.9		1.0		1.4	ns
t_{INYL}	Input Data Pad to Y Low 5 V TTL		0.9		1.1		1.2		1.4		1.9	ns
Input Module Predicted Routing Delays[3]												
t_{IRD1}	FO = 1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO = 2 Routing Delay		0.4		0.5		0.6		0.7		1	ns
t_{IRD3}	FO = 3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO = 4 Routing Delay		0.7		0.9		1		1.1		1.5	ns
t_{IRD8}	FO = 8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		1.7		2.2		2.5		3		4.2	ns

Notes:

1. *All –3 speed grades have been discontinued.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Table 2-36 • **A54SX72A Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 2.25 V, T_J = 70°C)

Parameter	Description	–3 Speed*		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{QCKH}	Input Low to High (100% Load) (Pad to R-cell Input)		3.0		3.4		3.9		4.6		6.4	ns
t_{QCHKL}	Input High to Low (100% Load) (Pad to R-cell Input)		2.9		3.4		3.8		4.5		6.3	ns
t_{QPWH}	Minimum Pulse Width High	1.5		1.7		2.0		2.3		3.2		ns
t_{QPWL}	Minimum Pulse Width Low	1.5		1.7		2.0		2.3		3.2		ns
t_{QCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.3		0.5	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5		0.5		0.6		0.9	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.4		0.5		0.5		0.6		0.9	ns

Note: **All –3 speed grades have been discontinued.*

Table 2-40 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.3		2.7		3.0		3.6		5.0	ns
t_{DHL}	Data-to-Pad High to Low		2.5		2.9		3.2		3.8		5.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.0		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.9		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3 V LVTTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		3.2		3.7		4.2		5.0		6.9	ns
t_{DHL}	Data-to-Pad High to Low		3.2		3.7		4.2		4.9		6.9	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		10.3		11.9		13.5		15.8		22.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.2		3.7		4.2		5.0		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.2		3.7		4.2		4.9		6.9	ns
d_{TLH}[3]	Delta Low to High		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta High to Low		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 10 pF loading and 25 Ω resistance.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

Table 2-41 • **A54SX72A Timing Characteristics (Worst-Case Commercial Conditions V_{CCA} = 2.25 V, V_{CCI} = 4.75 V, T_J = 70°C)**

Parameter	Description	–3 Speed[1]		–2 Speed		–1 Speed		Std. Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5 V PCI Output Module Timing[2]												
t_{DLH}	Data-to-Pad Low to High		2.7		3.1		3.5		4.1		5.7	ns
t_{DHL}	Data-to-Pad High to Low		3.4		3.9		4.4		5.1		7.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.1		3.5		4.1		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		3.9		4.4		5.1		7.2	ns
d_{TLH}[3]	Delta Low to High		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta High to Low		0.026		0.03		0.032		0.04		0.052	ns/pF
5 V TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad Low to High		2.4		2.8		3.1		3.7		5.1	ns
t_{DHL}	Data-to-Pad High to Low		3.1		3.5		4.0		4.7		6.6	ns
t_{DHLS}	Data-to-Pad High to Low—low slew		7.4		8.5		9.7		11.4		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.8		3.1		3.7		5.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.1		3.5		4.0		4.7		6.6	ns
d_{TLH}[3]	Delta Low to High		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}[3]	Delta High to Low		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}[3]	Delta High to Low—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *All –3 speed grades have been discontinued.*
2. *Delays based on 50 pF loading.*
3. *To obtain the slew rate, substitute the appropriate Delta value, load capacitance, and the V_{CCI} value into the following equation:*
   Slew Rate [V/ns] = $(0.1*V_{CCI} – 0.9*V_{CCI})/ (C_{load} * d_{T[LH|HL|HLS]})$
   where C_{load} is the load capacitance driven by the I/O in pF
   $d_{T[LH|HL|HLS]}$ is the worst case delta value from the datasheet in ns/pF.
4. *Delays based on 35 pF loading.*

208-Pin PQFP				
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB,I/O
77	GND	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V_{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND

208-Pin PQFP				
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V_{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O

144-Pin FBGA

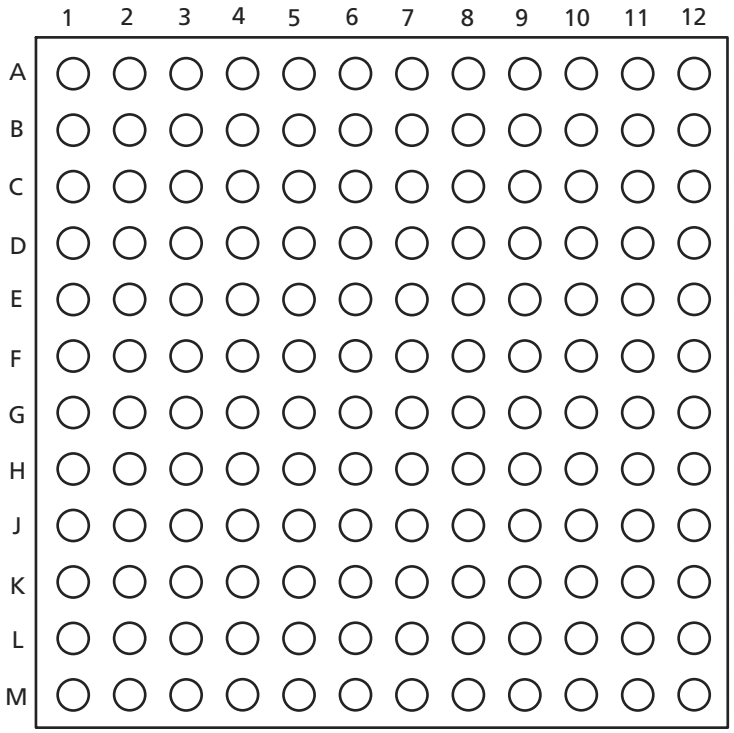


Figure 3-6 • **144-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

256-Pin FBGA

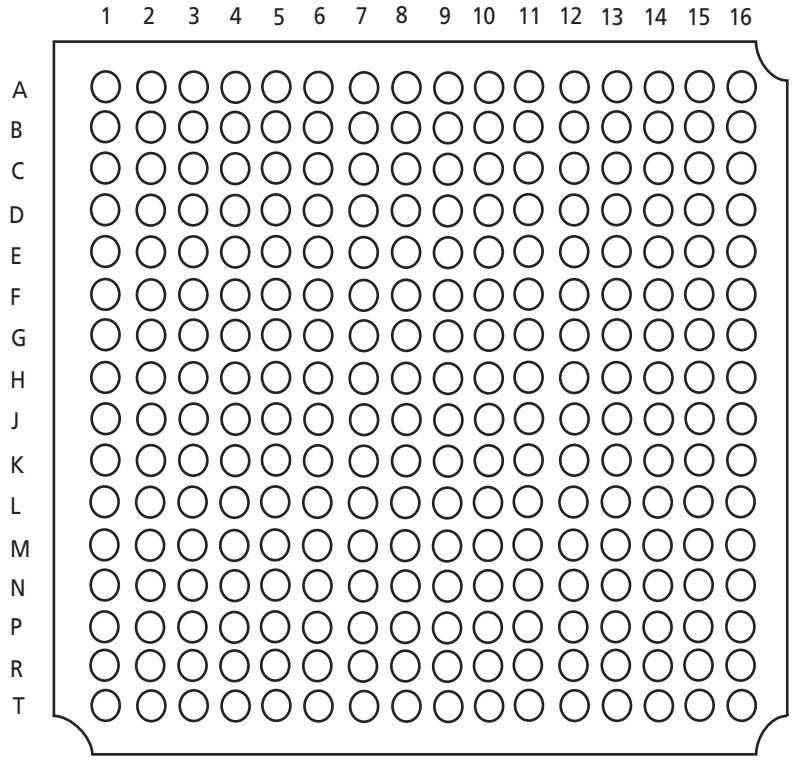


Figure 3-7 • **256-Pin FBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.actel.com/products/rescenter/package/index.html.

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
C19	I/O	I/O
C20	V_{CCI}	V_{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC*	I/O
C26	NC*	I/O
D1	NC*	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V_{CCI}	V_{CCI}
D5	NC*	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V_{CCI}	V_{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC*	I/O
D26	NC*	I/O
E1	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
E2	NC*	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V_{CCA}	V_{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V_{CCI}	V_{CCI}
E26	GND	GND
F1	V_{CCI}	V_{CCI}
F2	NC*	I/O
F3	NC*	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC*	I/O

484-Pin FBGA		
Pin Number	A54SX32A Function	A54SX72A Function
G1	NC*	I/O
G2	NC*	I/O
G3	NC*	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V_{CCA}	V_{CCA}
G24	I/O	I/O
G25	NC*	I/O
G26	NC*	I/O
H1	NC*	I/O
H2	NC*	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC*	I/O
H26	NC*	I/O
J1	NC*	I/O
J2	NC*	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V_{CCI}	V_{CCI}
J26	NC*	I/O
K1	I/O	I/O
K2	V_{CCI}	V_{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V_{CCA}	V_{CCA}

Note: **These pins must be left floating on the A54SX32A device.*

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC*	I/O
T26	NC*	I/O
U1	I/O	I/O
U2	V_{CCI}	V_{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V_{CCI}	V_{CCI}
U26	I/O	I/O
V1	NC*	I/O

484-Pin FBGA		
Pin Number	**A54SX32A Function**	**A54SX72A Function**
V2	NC*	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V_{CCA}	V_{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC*	I/O
V26	NC*	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V_{CCA}	V_{CCA}
W24	I/O	I/O
W25	NC*	I/O
W26	NC*	I/O
Y1	NC*	I/O
Y2	NC*	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC*	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V_{CCI}	V_{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: **These pins must be left floating on the A54SX32A device.*

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v5.3)	Page
v5.2 (June 2006)	–3 speed grades have been discontinued.	N/A
	The "SX-A Timing Model" was updated with –2 data.	2-14
v5.1 February 2005	RoHS information was added to the "Ordering Information".	ii
	The "Programming" section was updated.	1-13
v5.0	Revised Table 1 and the timing data to reflect the phase out of the –3 speed grade for the A54SX08A device.	i
	The "Thermal Characteristics" section was updated.	2-11
	The "176-Pin TQFP" was updated to add pins 81 to 90.	3-11
	The "484-Pin FBGA" was updated to add pins R4 to Y26	3-26
v4.0	The "Temperature Grade Offering" is new.	1-iii
	The "Speed Grade and Temperature Grade Matrix" is new.	1-iii
	"SX-A Family Architecture" was updated.	1-1
	"Clock Resources" was updated.	1-5
	"User Security" was updated.	1-7
	"Power-Up/Down and Hot Swapping" was updated.	1-7
	"Dedicated Mode" is new	1-9
	Table 1-5 is new.	1-9
	"JTAG Instructions" is new	1-10
	"Design Considerations" was updated.	1-12
	The "Programming" section is new.	1-13
	"Design Environment" was updated.	1-13
	"Pin Description" was updated.	1-15
	Table 2-1 was updated.	2-1
	Table 2-2 was updated.	2-1
	Table 2-3 is new.	2-1
	Table 2-4 is new.	2-1
	Table 2-5 was updated.	2-2
	Table 2-6 was updated.	2-2
	"Power Dissipation" is new.	2-8
	Table 2-11 was updated.	2-9

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.