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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	2880
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	249
Number of Gates	48000
Voltage - Supply	2.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (27X27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx32a-2fg484

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# Other Architectural Features

# Technology

The Actel SX-A family is im plemented on a high-voltage, twin-well CMOS process using 0.22 P/ 0.25 P design rules. The metal-to-metal antifuse is comprised of a combination of amor phous silicon and di electric material with barrier metals and has a programmed ('on' state) resistance of 25 : with capacitance of 1.0 fF for low signal impedance.

### Performance

The unique architectural feat ures of the SX-A family enable the devices to oper ate with internal clock frequencies of 350 MHz, causing very fast execution of even complex logic functions. The SX-A family is an optimal platform upon which to integrate the functionality previously cont ained in multiple complex programmable logic devices (CPLDs). In addition, designs that previously would have required a gate array to meet performance goals can be inte grated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

# **User Security**

Reverse engineering is virt ually impossible in SX-A devices because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. In addition, since SX-A is a nonvo latile, single-chip solution, there is no configuration bits tream to intercept at device power-up.

The Actel FuseLock advantag e ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located where they cannot be accessed or bypassed without destroying access to the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure (Figure 1-11).



Figure 1-11 • FuseLock

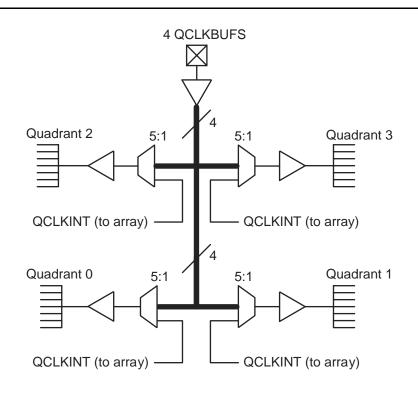
For more information, refer to Actel's Implementation of Security in Actel Antifuse FPGAs application note.

## I/O Modules

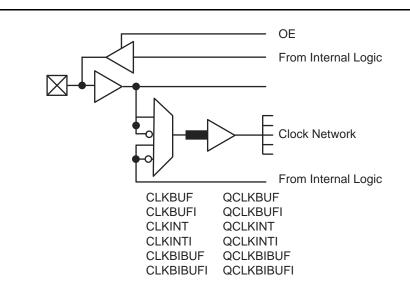
For a simplified I/O schematic, refer to Figure 1 in the application note, *Actel eX, SX-A, and RTSX-S I/Os*.

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed wi th the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-out put-pad timing as fast as 3.8 ns, even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops, requiring instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pinto-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design ti me. All unused I/Os are configured as tristate outputs by the Actel Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A I/Os should be driven by high-speed push-pull devices with a low-resistance pull-up device when being configured as tristate output buffers. If the I/O is driven by a voltage level greater than V <sub>CCI</sub> and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A lo gic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5 V to provide the logic '1' input, and V <sub>CCI</sub> is set to 3.3 V on the SX-A device, the input signal may be pulled down by the SX-A input. Each I/O module has an available power-up resistor of approximately 50 k : that can configure the I/O in a known state during power-up. For nominal pull-up and pull-down resistor values, refer to Table 1-4 on page 1-8 of the application note Actel eX, SX-A, and RTSX-S I/Os. Just slightly before V <sub>CCA</sub> reaches 2.5 V, the resistors are disabled, so the I/Os will be c ontrolled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerni ng available I/O features.



### Figure 1-9 • SX-A QCLK Architecture





## **Clock Resources**

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexor (MUX) in eac h R-cell. HCLK cannot be connected to combinatorial lo gic. This provides a fast propagation path for the clock signal. If not used, this pin must be set as Low or High on the board. It must not be left floating. Figure 1-7 describes the clock circuit used for the constant lo ad HCLK and the macros supported.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible sl ow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, these pins must be set as Low or High on the board. They must not be left floating. Figure 1-8 describes the CLKA and CLKB circuit used and the macros supported in SX-A devices with the exception of A54SX72A.

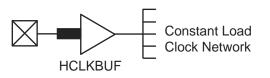
In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, and QCLKD—corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to an en tire quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 1-9 on page 1-6). QCLK pins can function as user I/O pins. If not used, the QCLK pins must be tied Low or High on the board and must not be left floating.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

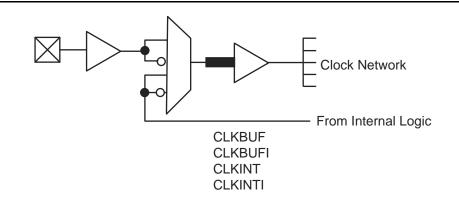
The CLKA, CLKB, and QCLK circuits for A54SX72A as well as the macros supported are shown in Figure 1-10 on page 1-6. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" section on page 1-15 .

Table 1-1 • SX-A Clock Resources

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD	) 0	0	0	4



#### Figure 1-7 • SX-A HCLK Clock Buffer



#### Figure 1-8 • SX-A Routed Clock Buffer